



DS89C420 Ultra-High-Speed Flash Microcontroller

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REVISION B5 ERRATA

The errata listed below describe situations where DS89C420 revision B5 components perform differently than expected or differently than described in the data sheet. Dallas Semiconductor intends to correct these errata in subsequent die revisions.

This errata sheet only applies to DS89C420 revision B5 components. Revision B5 components are branded on the top side of the package with a six-digit code in the form yywwB5, where yy and ww are two-digit numbers representing the year and workweek of manufacture, respectively. To obtain an errata sheet on another DS89C420 die revision, visit our website at www.maxim-ic.com/errata.

Note: Revision Ax and earlier DS89C420 devices were constructed with special silicon that required a unique parallel programming algorithm. Revision B4 and later use the standard parallel programming algorithm used by all other members of the ultra-high-speed flash microcontroller family. This transition will be transparent as the manufacturers of dedicated device programmers are the only users of the parallel programming interface. Any user who encounters difficulties programming new revision devices should contact their programmer manufacturer for a software update.

1. LOCK BIT SECURITY LEVELS 1, 2, AND 3 DO NOT FUNCTION PROPERLY

Description:

Security levels 1, 2, and 3 do not function properly and may not prevent access to internal flash memory if external program memory is used.

Work Around:

Use security level 4 if internal flash memory protection is required.