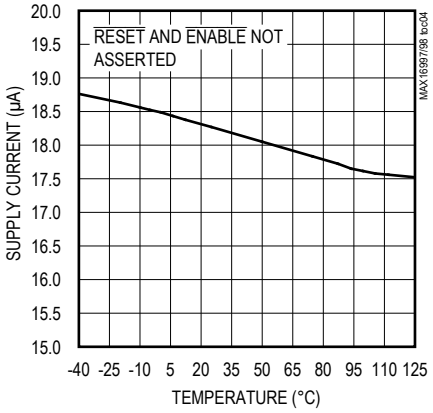
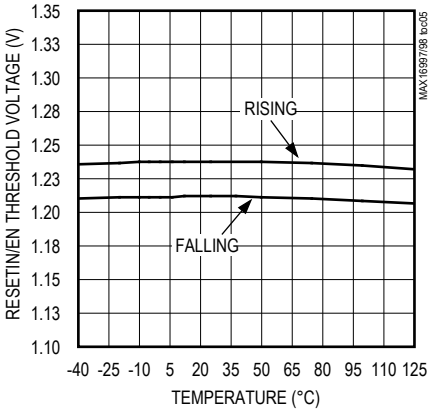
Typical Operating Characteristics (continued)

(C_{SWT} = C_{SRT} = 1500pF, T_A = +25°C, unless otherwise noted.)

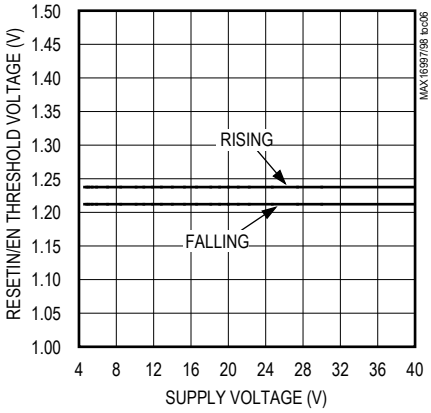
SUPPLY CURRENT vs. TEMPERATURE



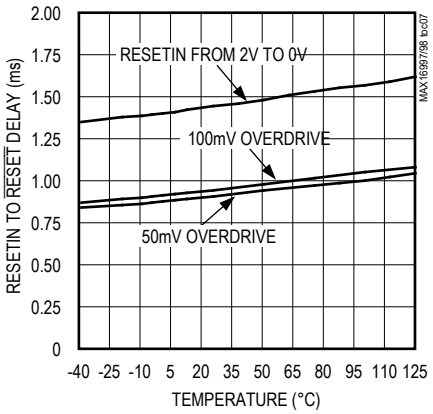
RESETIN/EN THRESHOLD VOLTAGE vs. TEMPERATURE



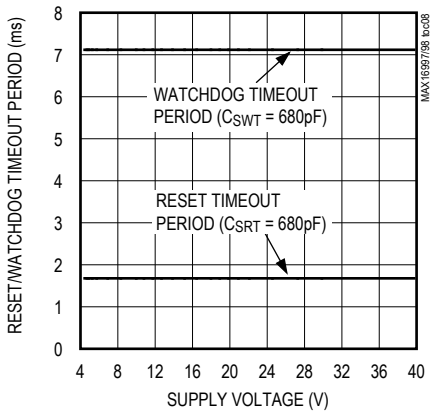
RESETIN/EN THRESHOLD VOLTAGE vs. SUPPLY VOLTAGE



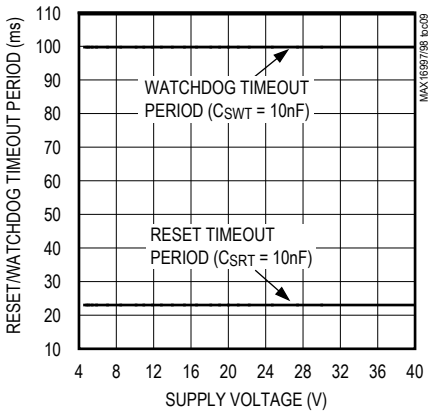
RESETIN TO $\overline{\text{RESET}}$ DELAY vs. TEMPERATURE



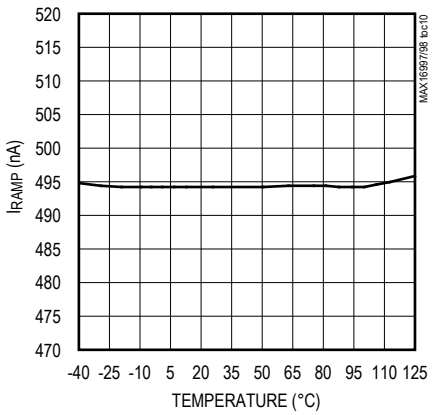
RESETIN/WATCHDOG PERIOD vs. SUPPLY VOLTAGE



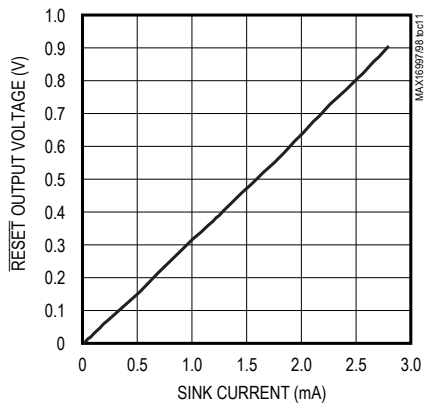
RESETIN/WATCHDOG PERIOD vs. SUPPLY VOLTAGE



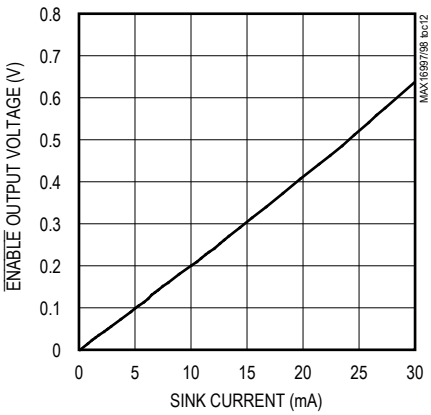
I_{RAMP} vs. TEMPERATURE



$\overline{\text{RESET}}$ OUTPUT VOLTAGE vs. SINK CURRENT



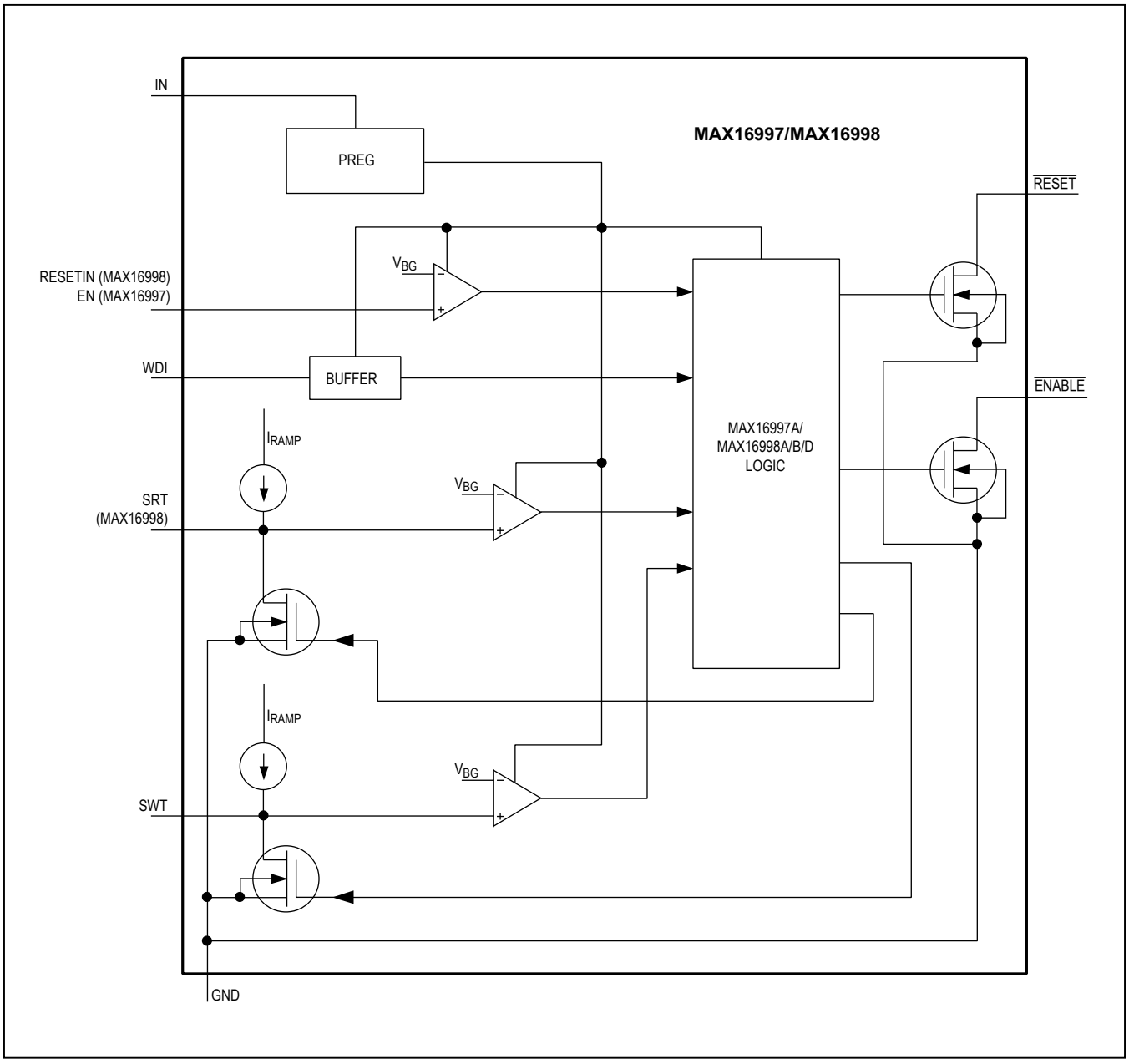
$\overline{\text{ENABLE}}$ OUTPUT VOLTAGE vs. SINK CURRENT



Pin Configuration

PIN		NAME	FUNCTION
MAX16997A	MAX16998A/B/D		
1	1	IN	Power-Supply Input. Bypass IN to GND with a 0.1µF capacitor.
2	—	EN	High-Impedance Input to the Enable Comparator. Depending on the voltage level at EN, the internal watchdog timer is turned on or off (see the *EN Input* section).
3, 7	—	N.C.	No Connection. Not internally connected.
4	4	SWT	Watchdog Timeout Adjustment Input. Connect a capacitor between SWT and GND to set the basic watchdog timeout period. Connect SWT to ground to disable the watchdog timer function. See the *Selecting the Watchdog Timeout Capacitor* section.
5	5	GND	Ground
6	6	WDI	Watchdog Input. **MAX16997A/MAX16998A (Timeout Watchdog):** Two consecutive WDI falling edges must occur at WDI within the watchdog timeout period or $\overline{\text{RESET}}$ asserts. The watchdog timer clears when a falling edge occurs on WDI or whenever $\overline{\text{RESET}}$ is asserted. $\overline{\text{ENABLE}}$ asserts if three consecutive watchdog timeout periods have expired without a falling edge at WDI. WDI is a high-impedance input. Leaving WDI unconnected will cause improper operation of the watchdog timer. **MAX16998B/D (Window Watchdog):** WDI falling transitions within periods shorter than the closed window width or longer than the basic watchdog timeout period force $\overline{\text{RESET}}$ to assert low for the reset timeout period. The watchdog timer begins to count after $\overline{\text{RESET}}$ is deasserted. The watchdog timer clears when a WDI falling edge occurs or whenever $\overline{\text{RESET}}$ is asserted. $\overline{\text{ENABLE}}$ asserts if three consecutive watchdog timeout periods have expired without a falling edge at WDI. WDI is a high-impedance input. Leaving WDI unconnected will cause improper operation of the watchdog timer.
8	8	$\overline{\text{ENABLE}}$	Open-Drain Enable Output. $\overline{\text{ENABLE}}$ asserts when three consecutive WDI faults occur. $\overline{\text{ENABLE}}$ remains low until three consecutive good WDI falling edges occur. $\overline{\text{ENABLE}}$ does not assert if the voltage at RESETIN (EN) is below its threshold. These devices are guaranteed to be in correct $\overline{\text{ENABLE}}$ output logic state when V_{IN} remains greater than 1.1V.
—	2	RESETIN	Reset Input. High-impedance input to the reset comparator. When $V_{RESETIN}$ falls below 1.235V, $\overline{\text{RESET}}$ asserts. $\overline{\text{RESET}}$ remains asserted as long as $V_{RESETIN}$ is low and for the reset timeout period after RESETIN goes high. Connect $V_{RESETIN}$ to the center point of an external resistive divider to set the threshold for the externally monitored voltage. Connect RESETIN to a defined voltage logic-level.
—	3	SRT	Reset Timeout Adjustment Input. Connect a capacitor between SRT and GND to set the reset timeout period. See the *Selecting the Reset Timeout Capacitor* section.
—	7	$\overline{\text{RESET}}$	Open-Drain Reset Output. $\overline{\text{RESET}}$ asserts whenever RESETIN drops below the selected reset threshold voltage (V_{PON}). $\overline{\text{RESET}}$ remains low for the reset timeout period after all reset conditions are removed, and then goes high. $\overline{\text{RESET}}$ asserts for a period of t_{RESET} whenever a WDI fault occurs. Connect $\overline{\text{RESET}}$ to a pullup resistor connected to a voltage higher than 2.5V (typ).

Functional Diagram



Timing Diagrams

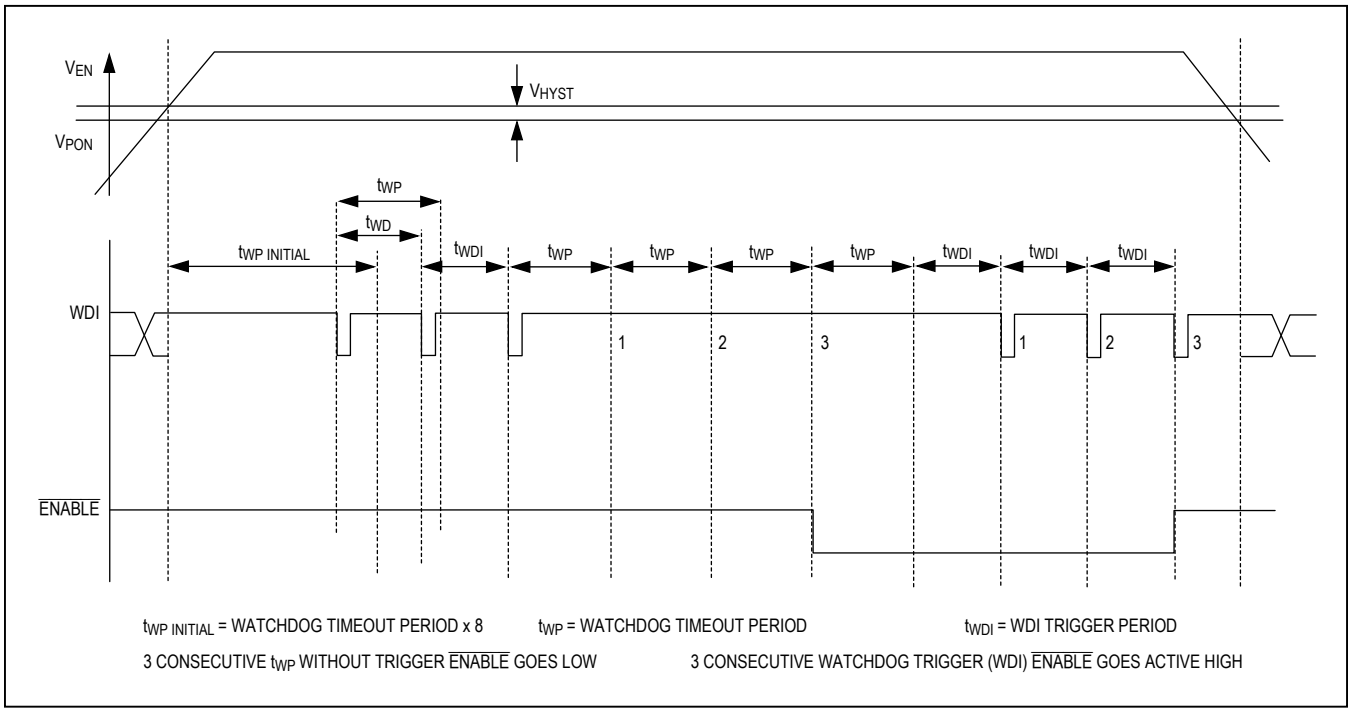


Figure 1. MAX16997A Timing Diagram

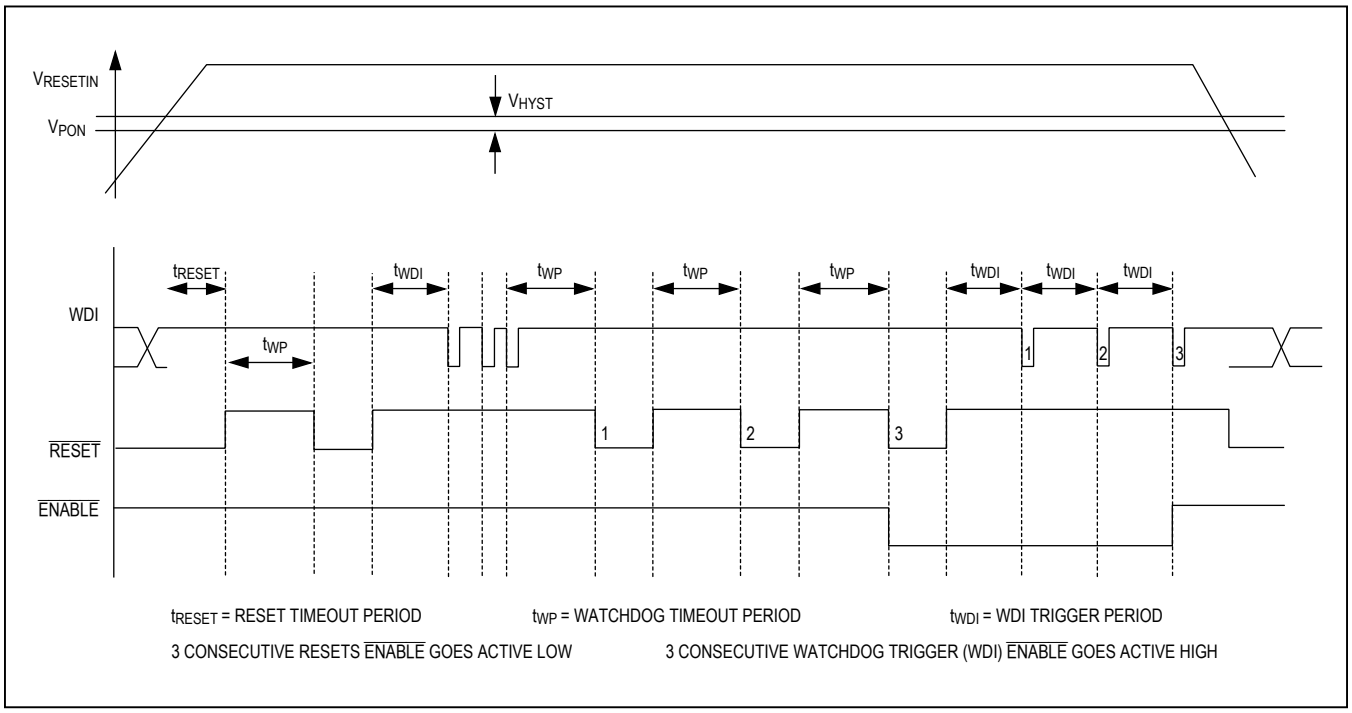


Figure 2. MAX16998A Timing Diagram

Timing Diagrams (continued)

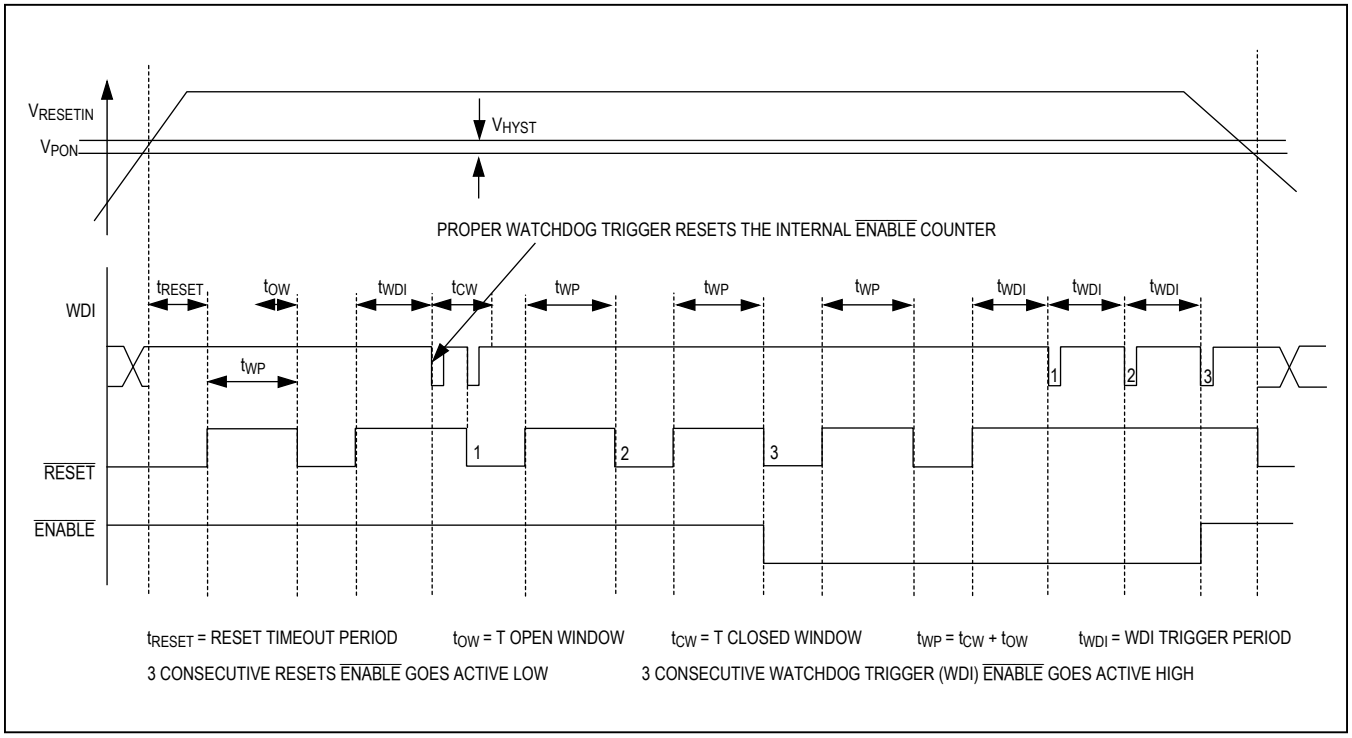


Figure 3. MAX16998B/D Timing Diagram

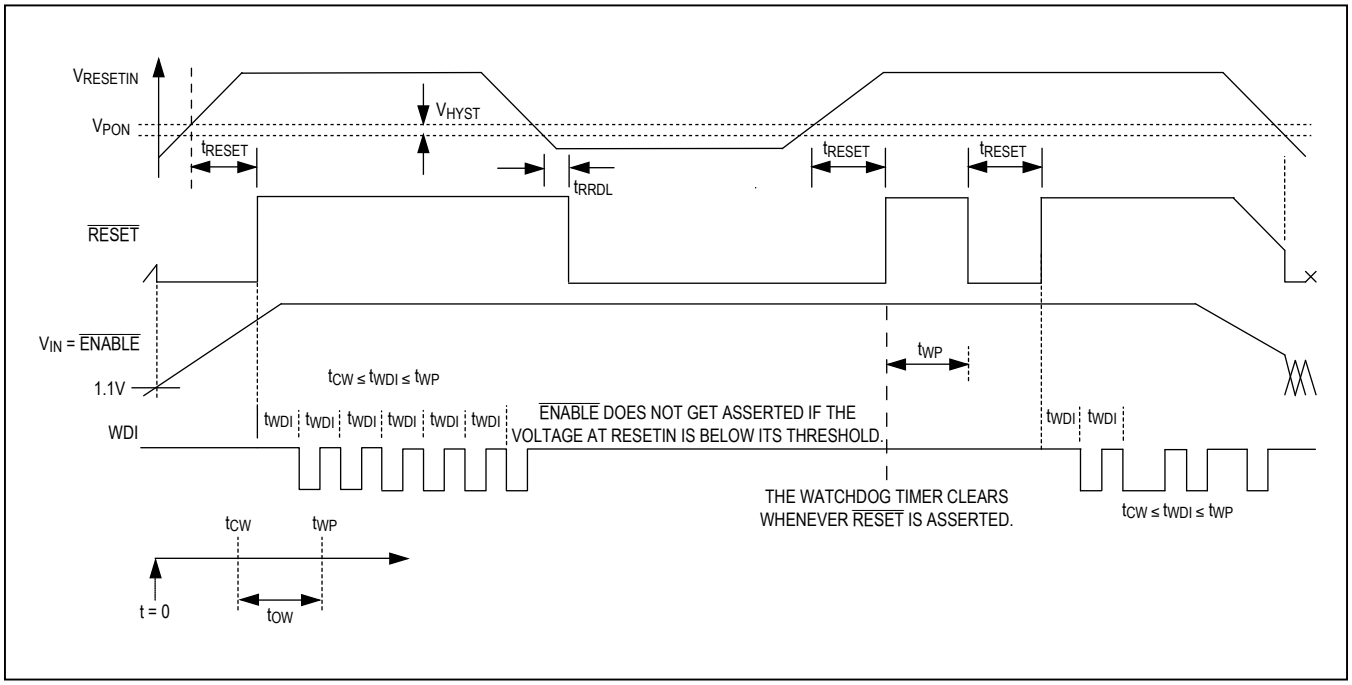


Figure 4. RESETIN, $\overline{RESET}$, V_{IN}, $\overline{ENABLE}$, and WDI Voltage Monitoring

Detailed Description

The MAX16997/MAX16998 are µP supervisory circuits for high-input-voltage and low-quiescent-current applications. These devices improve system reliability by monitoring the sub-system for software code execution errors. The MAX16997A/MAX16998A/B/D detect downstream circuit failures, and provide switchover to redundant circuitry. These devices provide complete adjustability for reset and watchdog functions.

The MAX16998A/B/D generate two output signals, $\overline{\text{RESET}}$ and $\overline{\text{ENABLE}}$, that depend on the voltage level at RESETIN and the signal at WDI. $\overline{\text{RESET}}$ asserts whenever RESETIN drops below the selected reset threshold voltage. $\overline{\text{RESET}}$ remains low for the reset timeout period after all reset conditions are deasserted, and then goes high. $\overline{\text{RESET}}$ also asserts for a period of $t_{\overline{\text{RESET}}}$ whenever a WDI fault occurs. The MAX16997A generates one output signal ($\overline{\text{ENABLE}}$) based on the voltage level at EN and the signal at WDI.

The MAX16997A/MAX16998A provide watchdog timeout adjustability with an external capacitor. The MAX16998A asserts $\overline{\text{RESET}}$ when two consecutive WDI falling edges do not occur within the watchdog timeout period. This device also asserts $\overline{\text{ENABLE}}$ if three consecutive watchdog timeout periods have elapsed without a falling edge at WDI. $\overline{\text{ENABLE}}$ remains low until three consecutive good WDI falling edges occur. $\overline{\text{ENABLE}}$ does not assert if the voltage at RESETIN (EN) is below its threshold. For the MAX16997A, the watchdog timer starts timing if the voltage at EN is higher than a preset threshold level. Each time the voltage at EN rises from below to above the preset threshold voltage, the initial watchdog timeout period is 8 times the normal watchdog timeout period (t_{WP}). Other than described above, the MAX16997A behaves the same as the MAX16998A.

The MAX16998B/MAX16998D contain a window watchdog timer that looks for activity outside an expected window of operation. The window size is factory-set to 50% (MAX16998B) or 75% (MAX16998D) of the adjusted watchdog timeout period.

Reset Output ($\overline{\text{RESET}}$) (MAX16998A/B/D)

The reset output is typically connected to the reset input of the µC to start or restart it in a known state. The MAX16998A/B/D provide an active-low open-drain reset logic to prevent code execution errors.

For the MAX16998A/B/D, $\overline{\text{RESET}}$ asserts whenever RESETIN drops below the selected reset threshold voltage (V_{PON}). $\overline{\text{RESET}}$ remains low for the reset timeout period after RESETIN exceeds the selected threshold voltage, and then goes high.

The MAX16998A asserts $\overline{\text{RESET}}$ for a period of $t_{\overline{\text{RESET}}}$ when two consecutive WDI falling edges do not occur within the adjusted watchdog timeout period. The MAX16998B/D also assert $\overline{\text{RESET}}$ for a period of $t_{\overline{\text{RESET}}}$ when a WDI falling edge does not occur within the open window period.

Anytime reset asserts, the watchdog timer clears. At the end of the reset timeout period, $\overline{\text{RESET}}$ goes high, and the watchdog timer is restarted from zero (see the *Selecting the Watchdog Timeout Capacitor* section).

Enable Output ($\overline{\text{ENABLE}}$)

If the µC fails to operate correctly (e.g., the software execution is stuck in a loop), WDI does not trigger any more and $\overline{\text{RESET}}$ pulls low, resetting the µC. If the µC does not work properly in the next loop either, the device asserts $\overline{\text{RESET}}$ again. After three watchdog timeout periods elapse with no falling edges at WDI, $\overline{\text{ENABLE}}$ asserts and flags a backup circuit that can take over the operation.

$\overline{\text{ENABLE}}$ remains low until three consecutive WDI falling edges with periods shorter than the watchdog timeout occur. $\overline{\text{ENABLE}}$ does not assert if the voltage at RESETIN (EN) is below its threshold. These devices are guaranteed to be in correct $\overline{\text{ENABLE}}$ output logic state when V_{IN} remains greater than 1.1V.

Power-On/Power-Off Sequence

Figure 5 shows the power-up and power-down sequence for $\overline{\text{RESET}}$ and $\overline{\text{ENABLE}}$ for the MAX16998A/B/D.

On power-up, once V_{IN} reaches 1.1V, $\overline{\text{RESET}}$ goes logic-low. As RESETIN rises, $\overline{\text{RESET}}$ remains low. When RESETIN rises above V_{PON}, the reset timer starts and $\overline{\text{RESET}}$ remains low. When the reset timeout period ends, $\overline{\text{RESET}}$ goes high.

For proper $\overline{\text{RESET}}$ operation, V_{IN} must rise above the minimum operating voltage of 5V for longer than 270µs before the RESETIN signal crosses the V_{PON} rising threshold of 1.135V (minimum). See Figure 6 for details.

On power-down, once RESETIN goes below V_{PON}, $\overline{\text{RESET}}$ goes low and remains low until V_{IN} drops below 1.1V. Figure 6 shows the detailed power-up sequence for the MAX16998A/B/D.

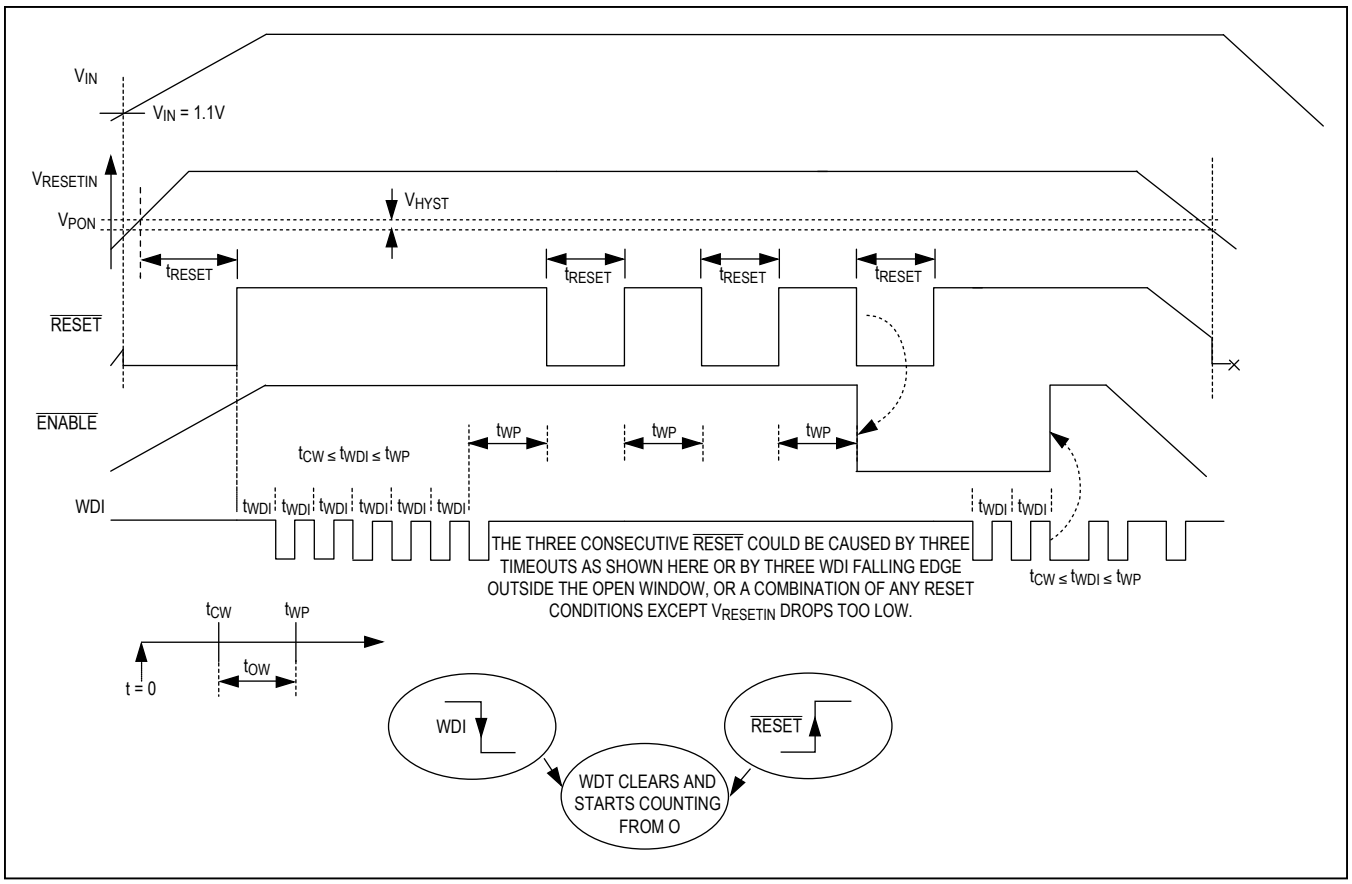


Figure 5. Power-On Reset and Power-Down Reset for the MAX16998A/B/D

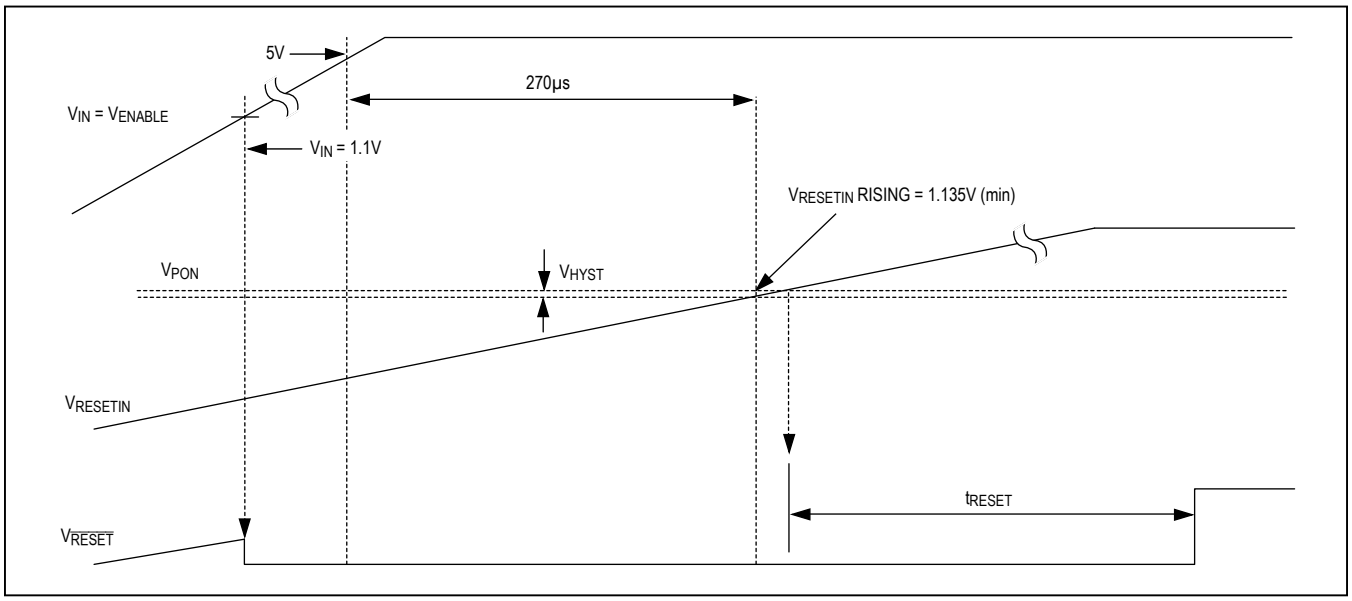


Figure 6. Detailed Power-Up Sequence for the MAX16998A/B/D

RESETIN Input (MAX16998A/B/D)

The MAX16998A/B/D monitor the voltage at RESETIN using an adjustable reset threshold, set with an external resistive divider (see Figure 7). $\overline{RESET}$ asserts when $V_{RESETIN}$ is below 1.235V.

Use the following equations to calculate the externally monitored voltage (V_{CC}).

$$V_{TH} = V_{PON}\left[\frac{R_1}{R_2}+1\right]$$

where V_{TH} is the desired reset threshold voltage, and V_{PON} = 1.235V. To simplify the resistor selection, choose a value for R_2 (< than 1MΩ) and calculate R_1.

$$R_1 = R_2\left[\frac{V_{TH}}{V_{PON}}-1\right]$$

EN Input

The MAX16997A provides a high-impedance input (EN) to the enable comparator. Based on the voltage level at EN, the watchdog timer is turned on or off. The watchdog timer starts timing if the voltage level at EN is higher than a preset threshold voltage (V_{PON}). Each time the voltage at EN rises from below to above the preset threshold voltage, the initial watchdog timeout period is 8 times the normal watchdog timeout period (t_{WP}).

Watchdog Timer

MAX16997A

The watchdog circuit monitors the µC's activity. For the MAX16997A, the watchdog timer starts timing once the voltage at EN is higher than a preset threshold voltage. $\overline{ENABLE}$ asserts if three consecutive watchdog timeout periods have elapsed without a falling edge at WDI. $\overline{ENABLE}$ remains low until three consecutive WDI falling edges with periods shorter than the watchdog timeout period occur.

Each time the voltage at EN rises from below to above the preset threshold voltage, the first watchdog timeout period extends by a factor of 8 (8 x t_{WP}). If a WDI falling edge occurs during that time, then the watchdog timeout period is immediately switched over to a single t_{WP}. If no watchdog falling edge occurs during this prolonged watchdog timeout period, $\overline{ENABLE}$ goes low at the end of this period and stays low. After this, the first falling edge at WDI switches the watchdog timeout period to a single t_{WP}. See Figure 1. The MAX16997A watchdog timeout period (t_{WP}) is adjustable by a single capacitor at SWT.

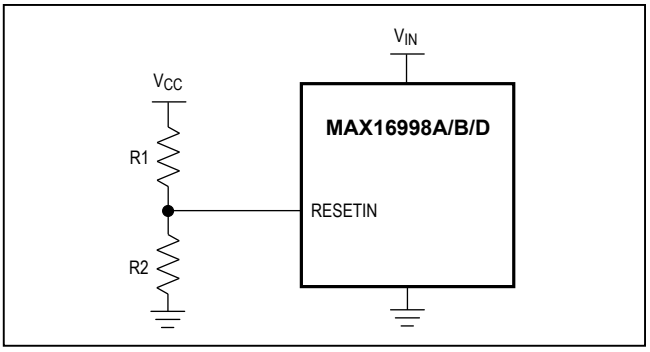


Figure 7. Setting RESETIN Voltage for the MAX16998A/B/D

MAX16998A

The MAX16998A asserts $\overline{RESET}$ when two consecutive WDI falling edges do not occur within the adjusted watchdog timeout period (t_{WP}). $\overline{RESET}$ remains asserted for the reset timeout period ($t_{\overline{RESET}}$) and then goes high. This device also asserts $\overline{ENABLE}$ if three consecutive watchdog timeout periods have elapsed without a falling edge at WDI. $\overline{ENABLE}$ remains low until three consecutive WDI falling edges with periods shorter than the watchdog timeout period occur (see Figure 2).

The internal watchdog timer is cleared by a $\overline{RESET}$ rising edge or by a falling edge at WDI. The watchdog timer remains cleared while $\overline{RESET}$ is asserted; as soon as $\overline{RESET}$ is released, the timer starts counting. WDI falling edges are ignored when $\overline{RESET}$ is low. If no WDI falling edge occurs within the watchdog timeout period, $\overline{RESET}$ immediately goes low and stays low for the adjusted reset timeout period.

MAX16998B/D

The MAX16998B/D have a windowed watchdog timer. The watchdog timeout period (t_{WP}) is the sum of a closed window period (t_{CW}) and an open window period (t_{OW}). If the µC issues a WDI falling edge within the open window period, $\overline{RESET}$ stays high. Once a WDI falling edge occurs within the closed window period, $\overline{RESET}$ immediately goes low and stays low for the adjusted reset timeout period (see Figure 3). If no WDI falling edge occurs within the watchdog timeout period, $\overline{RESET}$ immediately goes low and stays low for the adjusted reset timeout period. The open window size is factory-set to 50% of the watchdog timeout period for the MAX16998B and 75% for the MAX16998D.

Figure 8 shows a WDI falling edge identified as a *good* or a *bad* WDI signal edge. In case 1, the WDI falling edge occurs within the closed window period and is considered a *bad* WDI falling edge (early fault); therefore, it asserts $\overline{RESET}$. Case 2 also shows another fault. In this case,

no WDI falling edge occurs within the watchdog timeout period (t_{WP}) and is considered a late fault that asserts $\overline{RESET}$. In case 3, the WDI falling edge occurs within the open window period and is considered a *good* WDI signal falling edge. In this case, $\overline{RESET}$ stays high. In case 4, the WDI falling edge occurs within the indeterminate region. In this case, the $\overline{RESET}$ state is indeterminate.

These devices assert $\overline{ENABLE}$ after three consecutive bad WDI falling edges. $\overline{ENABLE}$ returns high after three consecutive good WDI signal falling edges (see Figure 3).

Either a rising edge at $\overline{RESET}$ or a falling edge at WDI clears the internal watchdog timer. The watchdog timer remains cleared while $\overline{RESET}$ is asserted. The watchdog timer begins counting when $\overline{RESET}$ goes high. WDI falling edges are ignored when $\overline{RESET}$ is low.

Applications Information

Selecting the Reset Timeout Capacitor

The reset timeout period is adjustable to accommodate a variety of µP applications. Adjust the reset timeout period ($t_{\overline{RESET}}$) by connecting a capacitor (C_{SRT}) between SRT and ground. See the Reset Timeout Period vs. C_{SRT} graph in the *Typical Operating Characteristics section*. Calculate the reset timeout capacitance using the equation below:

$$C_{SRT} = t_{RESET} \times \frac{I_{RAMP}}{V_{RAMP}}$$

where V_{RAMP} is in volts, $t_{\overline{RESET}}$ is in seconds, I_{RAMP} is in nA, and C_{SRT} is in nF.

Leakage currents and stray capacitance (e.g., a scope probe, which induces both) at SRT may cause errors in the reset timeout period. If precise time control is required, use capacitors with low leakage current and high stability.

Selecting the Watchdog Timeout Capacitor

The watchdog timeout period is adjustable to accommodate a variety of µP applications. With this feature, the watchdog timeout can be optimized for software execution. The programmer determines how often the watchdog timer should be serviced. Adjust the watchdog timeout period (t_{WP}) by connecting a capacitor (C_{SWT}) between SWT and GND. For normal mode operation, calculate the watchdog timeout capacitance using the following equation:

$$C_{SWT} = t_{WP} \times \frac{I_{RAMP}}{4 \times V_{RAMP}}$$

where V_{RAMP} is in volts, t_{WP} is in seconds, I_{RAMP} is in nA, and C_{SWT} is in nF. See the Watchdog Timeout Period vs. C_{SWT} graph in the *Typical Operating Characteristics section*.

For the MAX16998B/MAX16998D, the open window size is factory-set to 50% (MAX16998B) or 75% (MAX16998D) of the watchdog period. Leakage currents and stray capacitance (e.g., a scope probe, which induces both) at SWT may cause errors in the watchdog timeout period. If precise time control is required, use capacitors with low leakage current and high stability. To disable the watchdog timer function, connect SWT to ground and connect WDI to either the high- or low-logic state.

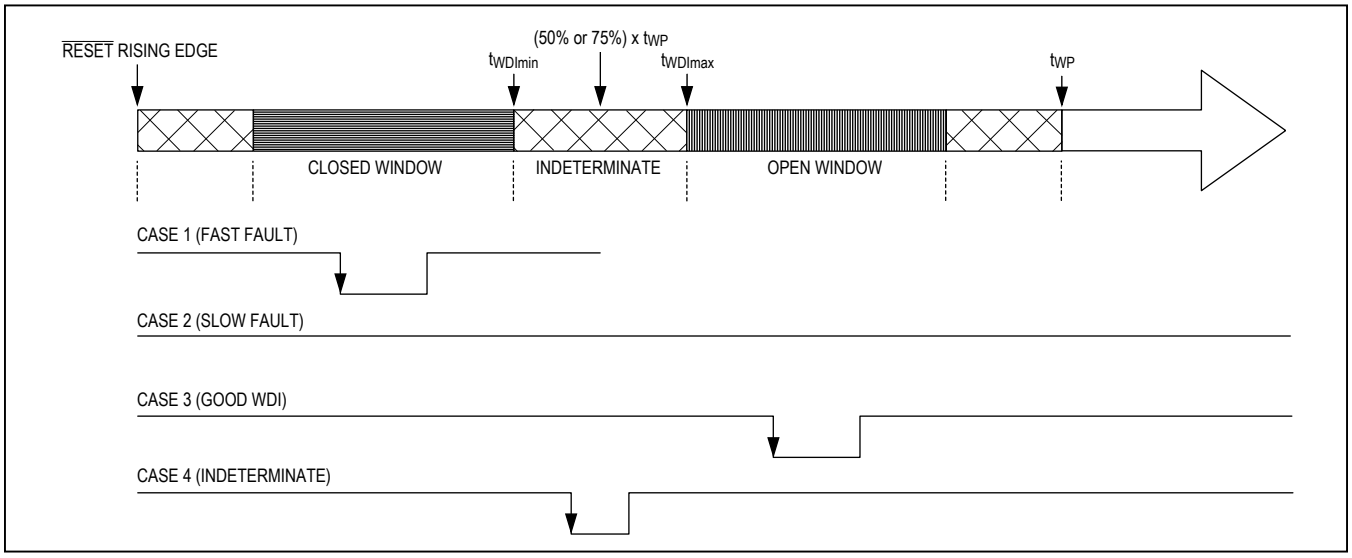


Figure 8. The MAX16998B/D Window Watchdog Diagram

Interfacing to Other Voltages for Logic Compatibility

As shown in Figure 9, the open-drain $\overline{\text{RESET}}$ output can operate in the 2.5V to 18V range. This allows the device to interface a µP with other logic levels.

WDI Glitch Immunity

For additional glitch immunity, connect an RC lowpass filter as close as possible to WDI (see Figure 10).

For example, for glitches with duration of 1µs, a 12kΩ resistor and a 47pF capacitor will provide immunity.

Layout Considerations

SRT and SWT are connected to internal precision current sources. When developing the layout for the application, minimize stray capacitance attached to SRT and SWT as well as leakage currents that can reach those nodes. SRT and SWT traces should be as short as possible. Route traces carrying high-speed digital signals and traces with large voltage potentials as far from SRT and SWT as possible. Leakage currents and stray capacitance (e.g., a scope probe, which induces both) at these pins may cause errors in the reset and/or watchdog timeout period. When evaluating these parts, use clean prototype boards to ensure accurate reset and watchdog timeout periods.

RESETIN is a high-impedance input and a high-impedance resistive divider (e.g., 100kΩ to 1MΩ) sets the threshold level. Minimize coupling to transient signals by keeping the connections to this input short. Any DC leakage current at RESETIN (e.g., a scope probe) causes errors in the programmed reset threshold.

Typical Operating Circuits

$\overline{\text{RESET}}$ remains asserted as long as RESETIN is below the regulated voltage and for the reset timeout period after RESETIN goes high to assure that the monitored LDO voltage is settled. Then, the µC starts operating and triggers WDI.

If the µC fails to operate correctly (e.g., the software execution is stuck in a loop), the WDI signal does not trigger the watchdog timer any more, and $\overline{\text{RESET}}$ is pulled low, resetting the µC. If the µC does not work properly in the next loop either, the device asserts $\overline{\text{RESET}}$ again. After three watchdog timeout periods with no WDI falling edges, $\overline{\text{ENABLE}}$ asserts and flags backup or safety circuits that take over the operation.

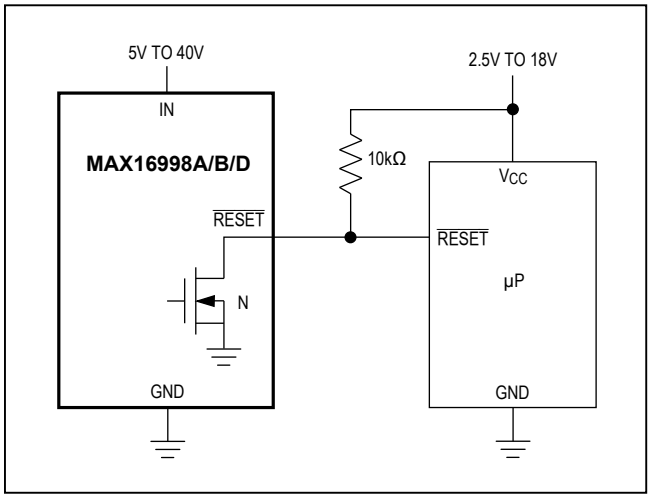


Figure 9. Interfacing to Other Voltage Levels

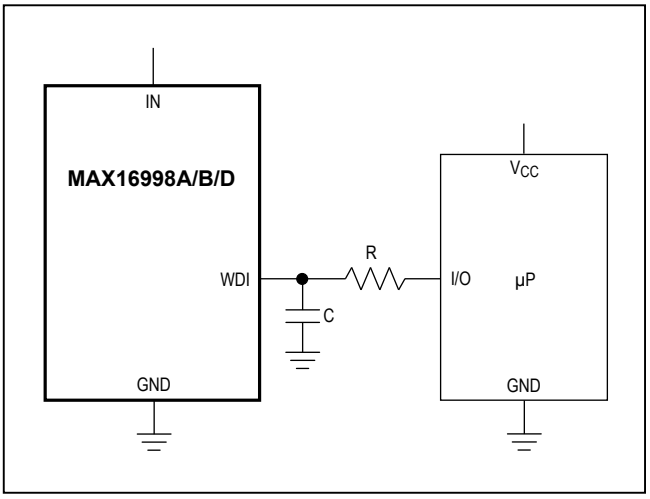


Figure 10. Additional WDI Glitch Immunity Circuit

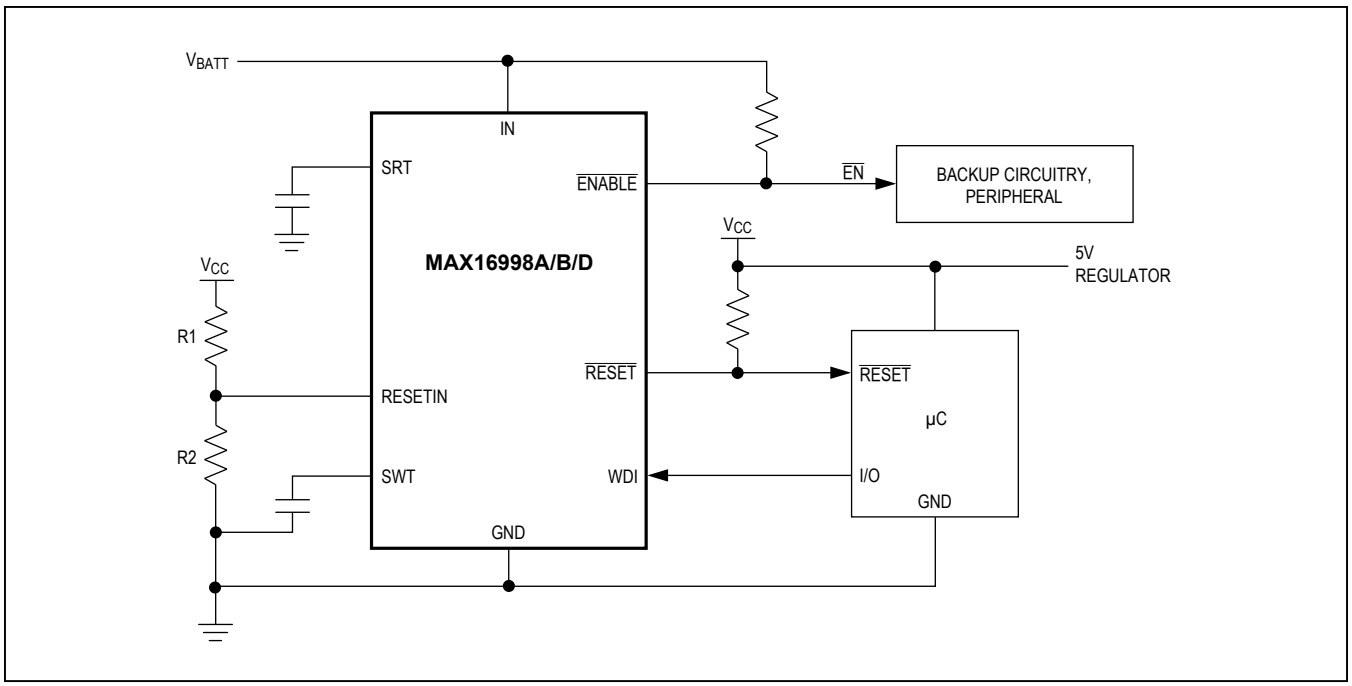


Figure 11. MAX16998A/B/D Switch Over to Backup Circuitry

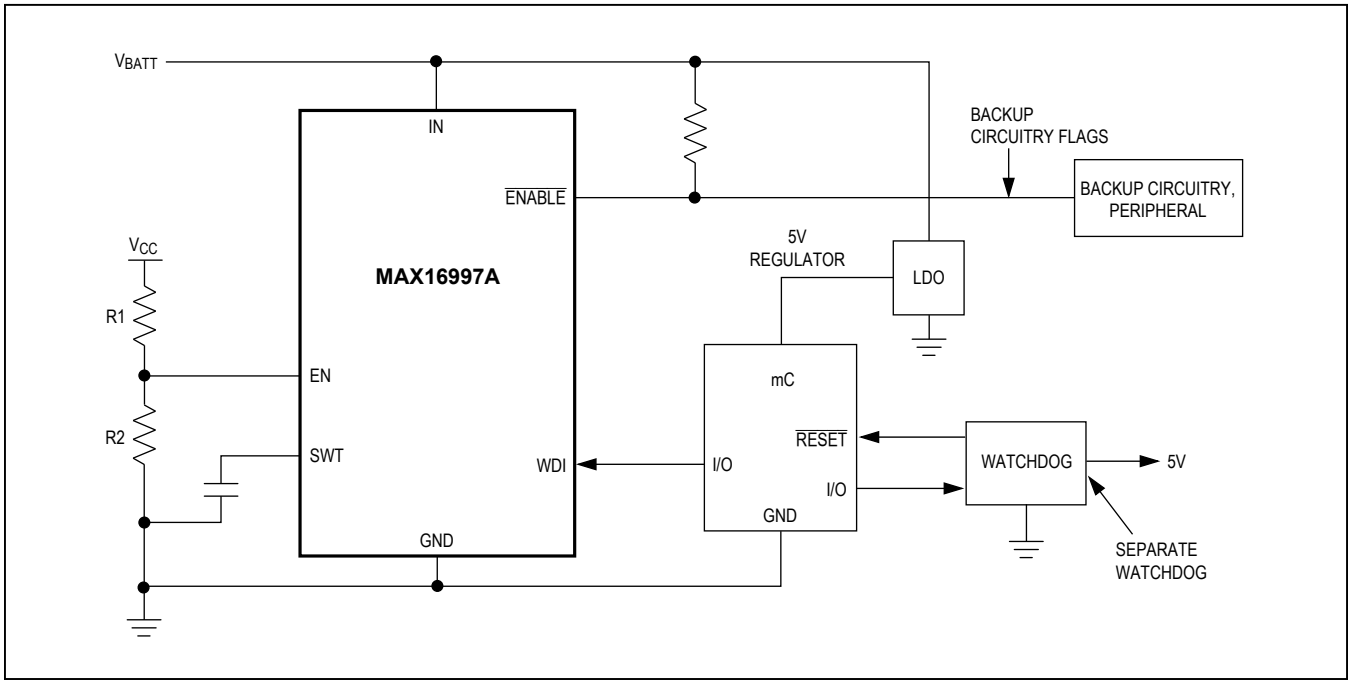
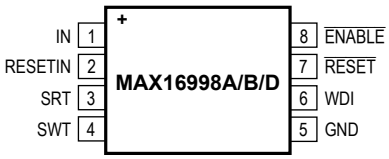


Figure 12. MAX16997A Application Diagram

Pin Configurations

TOP VIEW

µMAX



µMAX

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
8 µMAX	U8+1, U8+4	21-0036	90-0092

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	2/08	Initial release	—
1	4/09	Added bullet to *Features* section, revised *Electrical Characteristics* table	1, 2, 3
2	8/09	Added automotive qualified parts	1
3	11/15	Updated package code and rebranded data sheet	15
4	3/16	Deleted MAX16997AAUA/V+ variant from *Ordering Information*	1
5	4/19	Changes to Power-on/Power-off Sequence section and updated Figure 6	9, 10

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