High Precision Analog Front End

ADI Confidential

AD1018

FEATURES

- **Analog input/output**
  - **Multichannel, 16-bit, 1 MSPS SAR ADC**
    - **17 external voltage input channels**
    - **4 TIA input channels**
    - **Internal channels**
      - **11 IDAC monitor channels**
      - **9 VDAC monitor channels**
      - **3 power monitor channels**
    - **Single-ended mode**
  - **IDACs**
    - **11 low noise, 16-bit, IDAC outputs**
      - **Four channels either 0 mA to 150 mA or 0 mA to 200 mA**
      - **Seven channels 0 to 20 mA or, 0 to 50 mA channels**
  - **VDACs: Nine 16-bit output VDAC channels**
    - **Channel 0, Channel 1, Channel 3, and**
      - **Channel 4: 0 V to 5 V, 150 Ω**
    - **Channel 2: 0 V to 5 V, 1 kΩ**
    - **Channel 5 to Channel 8: 0 V to 2.5 V, 500 Ω**
  - **On-chip voltage reference, 2.5 V**
- **SPI interface up to 40 MHz**
- **Power**
  - **Multiple supplies**
    - **AVDDx for VDACs and ADC to 5 V**
    - **1.65 V to AVDDx – 0.5 V for PVDD_IDACx**
- **Packages and temperature range**
  - **4.5 mm × 4.6 mm, 100-ball WLCSP**
  - **Fully specified for –40°C to +120°C (T_{JA} operation)**

APPLICATIONS

- **Optical communication modules**

GENERAL DESCRIPTION

The AD1018 is an analog front end (AFE) that has a high precision analog-to-digital converter (ADC), voltage output digital-to-analog converters (VDACs), and current output digital-to-analog converters (IDACs).

The ADC signal chain contains four transimpedance amplifier inputs (TIAs), 17 external voltage inputs, nine VDAC monitor channels, 11 IDAC monitor channels, a precharge buffer, and a 1 MSPS successive approximation register (SAR) ADC.

The TIAs convert an input current to voltage and use an internal 2.5 V ADC reference for the positive terminal.

The input multiplexer selects and configures either one of the channels (TIAx_OUT, AINx, IDACx, or VDACx) or one of the internal power monitor signals (AVDDx × 3/8, IOVDD × 3/8, PVDD_IDACx, or AGNDx) as an output to the SAR ADC input. These inputs are single-ended. AGNDx is used as the reference signal. An ADC sequencer option is also available to program an automatic channel measurement sequence (see the AD1018 Hardware Reference Manual for more information).

The AD1018 provides 11 channels of low noise, low drift IDAC outputs with a full-scale range (0 mA to 20 mA or 0 mA to 50 mA for IDAC0 to IDAC6, and 0 mA to 150 mA or 0 mA to 200 mA for IDAC7 to IDAC10). Each IDAC channel has 16-bit resolution.

The AD1018 has nine VDAC channels with 16-bit resolution. Each channel has a voltage output buffer.

A 2.5 V on-chip reference buffer can drive a 100 nF capacitive load and maximum load current of 10 mA. This buffer is designed to bias an external thermal resistor.

Use the 4-wire serial port interface (SPI) at up to 40 MHz to configure each block and to gather ADC data.

FUNCTIONAL BLOCK DIAGRAM

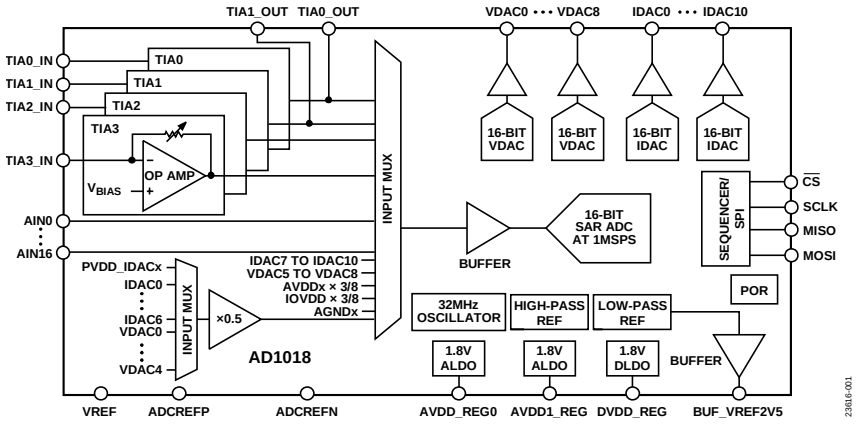

Figure 1.

Rev. Sp0 **Document Feedback**

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700

Technical Support **www.analog.com**

NOTES

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