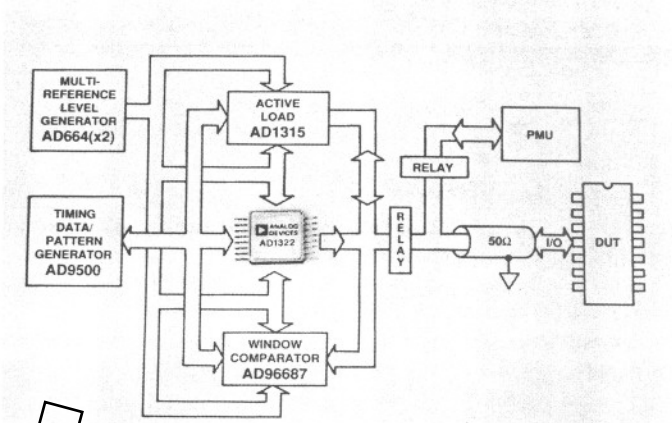
Ultrahigh Speed Pin Driver with Inhibit Mode

AD1322

FEATURES
- 200 MHz Driver Operation
- Driver Inhibit Function
- 200 ps Edge Matching
- Guaranteed Industry Specifications
  - 50 Ω Output Impedance
  - 2 V/ns Slew Rate
  - Variable Output Voltages for ECL, TTL and CMOS
- High Speed Differential Inputs for Maximum Flexibility
- Hermetically Sealed Small Gull Wing Package

APPLICATIONS
- Automatic Test Equipment
  - Semiconductor Test Systems
  - Board Test Systems
- Instrumentation & Characterization Equipment



PRODUCT DESCRIPTION

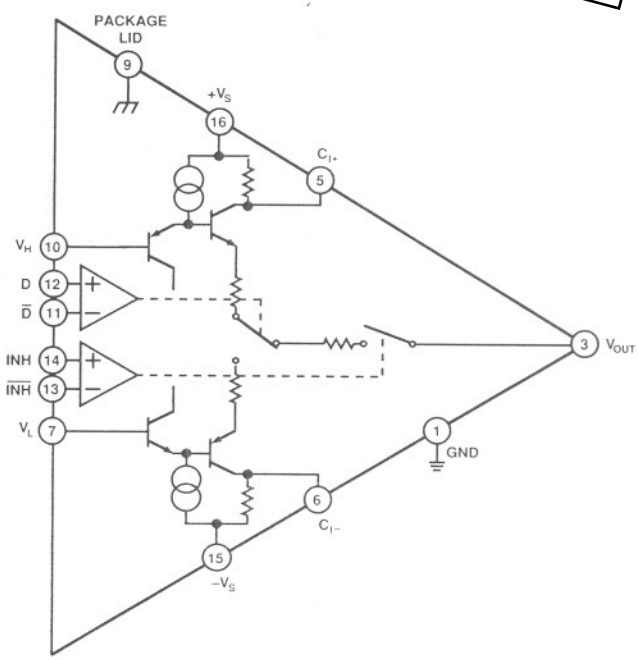
The AD1322 is a complete high speed pin driver designed for use in digital or mixed signal test systems. By combining a high speed monolithic process with a unique surface mount package, this product attains superb electrical performance while preserving optimum packaging densities and long term reliability in an ultrasmall 16-lead, hermetically sealed (gull wing) package.

Featuring unity gain programmable output levels of −2 V to +7 V with output swing capability of less than 100 mV to 9 V, the AD1322 is designed to stimulate ECL, TTL and CMOS logic families. The 200 MHz (2.5 ns pulsewidth) data rate capacity, 2 V/ns slew rate, and matched output impedance allows for real-time stimulation of these digital logic families. To test I/O devices, the pin driver can be switched into a high impedance state (inhibit mode) electrically removing the driver from the path, through the inhibit mode feature. The pin driver leakage current in inhibit is typically 50 nA, and output charge transfer entering inhibit is typically less than 15 pC.

The AD1322 transition from HI/LO or to inhibit is controlled through the data and inhibit inputs. The input circuitry is implemented utilizing high speed differential inputs with a common-mode range of 3 volts. This allows for direct interface to the precision of differential ECL timing or the simplicity of stimulating the pin driver from a single ended TTL or CMOS logic source. The analog logic HI/LO inputs are equally easy to interface. Typically requiring 350 μA of bias current, the AD1322 can be directly coupled to the output of a digital-to-analog converter.

The 200 MHz analog bandwidth of the logic HI/LO inputs allows for four quadrant multiplying providing maximum flexibility as a standard pin driver and a waveform generator all in one package.

The AD1322 is available in a 16-lead, hermetically sealed gull wing package and is specified to operate over the ambient commercial temperature range from 0 to +70°C.



Functional Block Diagram

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SPECIFICATIONS (All measurements made in free air at +25°C. Output load 10 kΩ/6 pF with $+V_S = +10$ V, $-V_S = -5.2$ V unless otherwise specified)

Parameter	AD1322KZ Min	Typ	Max	Units	Comments
DIFFERENTIAL INPUT CHARACTERISTICS					
D to $\overline{D}$, INH to $\overline{INH}$					
Input Voltage	−2.0		+7.0	Volts	
Differential Input Range	0.4	ECL	3.0	Volts	
Bias Current		175	300	μA	
REFERENCE INPUTS					See Note 1
V_{HIGH} Range (V_H)	−2.5		+7.5	Volts	
V_{LOW} Range (V_L)	−2.5		+7.5	Volts	
V_{HIGH} Bias Currents (V_H)		0.5	1.2	mA	
V_{LOW} Bias Currents (V_L)		0.3	0.5	mA	
Input Bandwidth		200		MHz	See Figure 9
OUTPUT CHARACTERISTICS					See Notes 1, 2
Logic High Range	−2.0		+7.0	Volts	
Logic Low Range	−2.0		+7.0	Volts	
Amplitude [$V_H - V_L$]	0.1		+9.0	Volts	
Accuracy					See Figure 1
Initial Offset					See Note 3
V_H	+320	+350	+380	mV	
V_L	−180	−150	−120	mV	
Gain Error	−4.5	−2.5	−0.5	% of Set Level	See Note 4
Linearity Error					
0 V to +5.5 V	−0.5		+0.5	% of Set Level	
−2 V to +7 V	−1.0		+1.0	% of Set Level	
Output Voltage TC		0.5		mV/°C	See Figures 7 & 8
Current Drive					
Static	30.0			mA	
Dynamic	100.0			mA	See Note 5
Current Limit			85	mA	
Output Impedance	48.5	50.0	51.5	ohms	See Note 6
DYNAMIC PERFORMANCE					
Driver Mode					See Note 7
Delay Time	0.9	1.2	1.5	ns	See Figure 2
Prop Delay TC		2.0		ps/°C	See Figure 4
Delay Time Matching					
Edge-to-Edge	−200	±50	+200	ps	See Figure 5
Rise & Fall Times					See Figure 10
1 V Swing		0.5	0.9	ns	Measurement 20%–80%
3 V Swing		1.8	2.2	ns	Measurement 10%–90%
5 V Swing		3.1	3.5	ns	Measurement 10%–90%
Large Signal Slew	1.5	1.7		V/ns	
Toggle Rate	200			MHz	ECL output
Minimum PW, $V_{OUT} = 2$ V		2.0		ns	See Figure 12
Overshoot & Preshoot					
Settling Time					See Figure 3
to ±3% V_O ±50 mV			15	ns	
to ±1% V_O			500	ns	
Delay Time vs. PW		100		ps	See Note 8, See Figure 6

Parameter	AD1322KZ Min	Typ	Max	Units	Comments
DYNAMIC PERFORMANCE					
Inhibit Mode					See Figure 2
Delay Time	1.3	1.6	1.9	ns	See Note 9
Delay Time Matching					
Edge-to-Edge	−200	±50	+200	ps	
Overshoot & Preshoot		40	80	mV	See Figure 3
Output Capacitance		8	10	pF	
Output Charge Going into Inhibit Mode		15		pC	See Figure 13
Leakage Current in Inhibit Mode					
−2 V to +5 V		50	200	nA	
+5 V to +7 V			1.0	μA	
POWER SUPPLIES					
$-V_S$ to $+V_S$ Range			15.2	Volts	
Supply Range					See Note 10
Positive Supply	+8.0	+10.0	+12.0	Volts	
Negative Supply	−7.2	−5.2	−3.2	Volts	
Current					
Positive Supply	4.2	60	78	mA	
Negative Supply	−78	−60	−42	mA	
+PSRR V_{OH} = +7 V	0.5		0.5	%/%V_{OUT}	+V = ±2.5%
−PSRR V_{OL} = −2 V	0.5		0.5	%/%V_{OUT}	−V = ±2.5%

NOTES

[1]The output voltage range is specified for −2 V to +7 V for typical power supply values of −5.2 V and +10.0 V but can be offset for different values of V_{OUT} such as 0 V to +9 V as long as the required headroom of 3 V is maintained between both V_H and $+V_S$ and V_L and $-V_S$.

[2]V_H can be set to be as much as 4 volts below V_L without any harm to the driver with the restriction that neither level can go below −2 V with the typical power supply setting. In this condition the rise and fall times will approximately double.

[3]All pin drivers are pretrimmed at the factory to incorporate an offset error of +350 mV, ±30 mV for V_H and −150 mV, ±30 mV for V_L. For V_H and V_L the offset error remains constant within the specified range.

[4]The gain error of the driver is always in the negative direction with respect to the voltage set level.

[5]Transient output current can easily exceed the AD1322's steady-state current limit when driving capacitive loads. The transient output current capability can be increased by connecting 0.039 μF capacitors between Pin 5 and ground and Pin 6 and ground. This will prevent the driver from current limiting by providing the "edge" current necessary when driving capacitive loads. These capacitors will not affect the driver's dc current limit.

[6]Driver output impedance is 50 ohms, ±1.5 ohms for a 3 V swing into a 50 ohm cable.

[7]Delay times are measured from the crossing of differential ECL outputs at the inputs to the driver to the 50% point of a ±400 mV driver output.

[8]Delay matching vs. PW is defined as the amount of change in propagation, with respect to the leading edge, due to change in pulsewidth of the input signal. The AD1322 is characterized over the pulsewidth range of 2 ns to 100 ns.

[9]Inhibit mode delay times are measured from the crossing of differential (ECL) INH inputs to a 200 mV transition at the pin driver output. V_{OUT} is connected to a 100 ohm/15 pF load terminated to ground. V_{OH} is set at +1 V and V_{OL} is set at −1 V for this test.

[10]A supply range of 15.2 V must be maintained to guarantee a 9 V output swing.

ABSOLUTE MAXIMUM RATINGS*

Power Supply Voltage
- +Vs to GND . . . . . +13 V
- $-V_S$ to GND . . . . . −8.2 V
- Difference from $+V_S$ to $-V_S$ . . . . . 16 V

Inputs
- Difference from D to $\overline{D}$ . . . . . 5 V
- Difference from INH to $\overline{INH}$ . . . . . 5 V
- D, $\overline{D}$, INH, $\overline{INH}$ . . . . . $+V_S$ −12 V, $-V_S$ +11.5 V
- V_H to V_L . . . . . −4 V, +9 V
- V_H, V_L . . . . . $+V_S$ −13.0 V, $-V_S$ +13.2 V

Driver Output
- Voltage . . . . . $+V_S$ −13.0 V, $-V_S$ +13.2 V
- Short Circuit to GND . . . . . Indefinite

Operating Temperature Range . . . . . 0 to +70°C

Storage Temperature Range . . . . . −65°C to +125°C

Lead Temperature Range (Soldering 20 sec)† . . . . . +300°C

NOTES

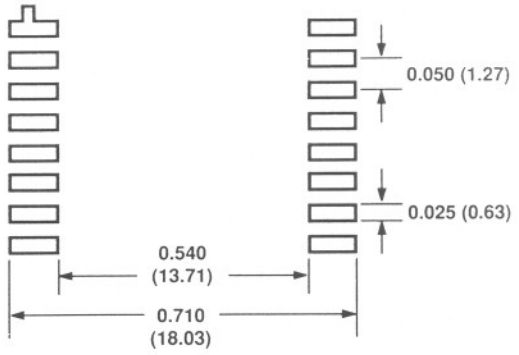
*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

†To ensure lead coplanarity (±0.002 inches) and solderability handling with bare hands should be avoided and the device should be stored in an environment at 24°C, ±5°C (75°F, ±10°F) with relative humidity not to exceed 65%.

CONNECTION DIAGRAMS

Dimensions shown in inches and (mm).

SUGGESTED LANDING PADS LOCATION



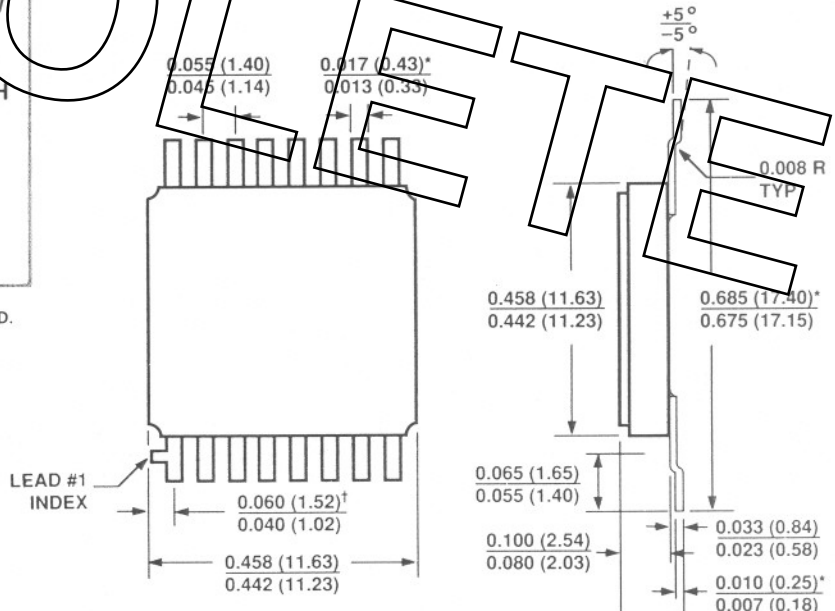
PIN CONFIGURATION

PIN NO.	SYMBOL	FUNCTION
1	GND	CIRCUIT GROUND
2	N/C	NO CONNECTION
3	V_{OUT}	DRIVER OUTPUT
4	N/C	NO CONNECTION
5	C_{1+}	POSITIVE DECOUPLE
6	C_{1-}	NEGATIVE DECOUPLE
7	V_L	VOLTAGE LOGIC LOW
8	N/C	NO CONNECTION
9	LID	LID CONNECTION*
10	V_H	VOLTAGE LOGIC HIGH
11	$\overline{D}$	DRIVER INPUT
12	D	DRIVER INPUT
13	$\overline{INH}$	INHIBIT INPUT
14	INH	INHIBIT INPUT
15	$-V_S$	NEGATIVE SUPPLY
16	$+V_S$	POSITIVE SUPPLY

*IT IS RECOMMENDED TO CONNECT PIN 9 TO CIRCUIT GROUND.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



* ADD AN ADDITIONAL 0.003 INCHES (0.08mm) TO MAX LIMITS, TO ALLOW FOR SOLDER THICKNESS.

† APPLIES TO ALL FOUR CORNERS

ORDERING GUIDE

Model	Temperature Range	Package	Quantity	Price
AD1322KZ	0 to +70°C	16-Lead Gull Wing	1–24	$169.00
			25–99	$124.00
			100+	$ 89.00

OFFSET ERROR

The offset error for logic high is determined by holding the output of the driver at logic high, and applying zero volts to the logic high reference input. The driver output value represents the offset "high" error. The same approach is used to identify offset "low" error. Refer to the Specification Table, Note 3.

$$V_{HIGH\ OFFSET} = V_{OUT}$$

where:

V_H = 0 V
D = HIGH
$\overline{D}$ = LOW
INH = LOW
$\overline{INH}$ = HIGH

GAIN ERROR

Defined as the ratio of the driver's output voltage to its logic set level voltage and is expressed in terms of percent of set level. The gain error is typically seen as 2.5% and is always in the negative direction with respect to the logic set level.

$$V_{HIGH\ GAIN}\ (\%) = \frac{V_{OUT} - V_H - V_{HIGH\ OFFSET}}{V_H} \times 100$$

where:

V_H = 5.0 V+$V_{HIGH\ OFFSET}$
D = HIGH
$\overline{D}$ = LOW
INH = LOW
$\overline{INH}$ = HIGH

LINEARITY ERROR

The deviation of the transfer function from a reference line. For the AD1322, the linearity error is calculated by subtracting the worst case gain error from the best case gain error (for the specified range) and divide the result by two. This method guarantees that the maximum linearity error for any set level within the specified range will be within the specified limits.

$$V_{HIGH\ LINEARITY}\ (\%) = \frac{V_{HIGH\ GAIN}\ (max) - V_{HIGH\ GAIN}\ (min)}{2} \times 100$$

DELAY TIME

The amount of time it takes the input signal to propagate through the driver and be converted to the desired logic levels. The measurement technique is defined in the notes and is shown in Figure 2.

EDGE-TO-EDGE MATCHING

Edge-to-edge matching is the difference, in time, between the delay time of the rising edge and the falling edge.

MINIMUM PULSEWIDTH

Defined as the smallest pulse applied to the input of the driver which can maintain an output signal amplitude of 2 V. The minimum pulsewidth is measured at the 50% point of the waveform.

OVERSHOOT AND PRESHOOT

The amount by which the driver's output voltage exceeds the desired set voltage. Preshoot is similar to overshoot but is the amount by which the driver's output goes below the initial voltage when driving to the new set level (or inhibit mode). See Figure 3.

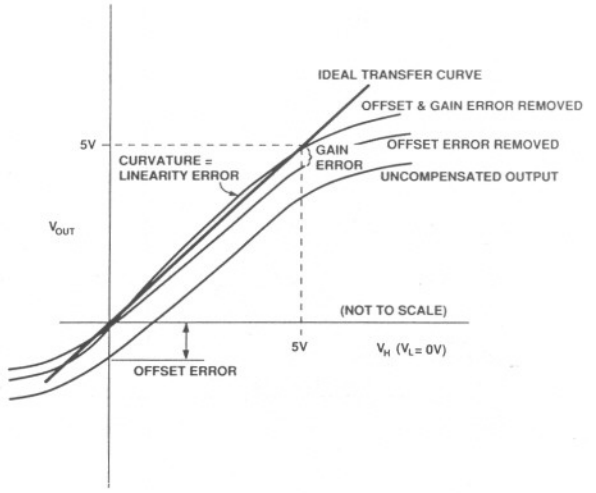


Figure 1. Definition of Terms

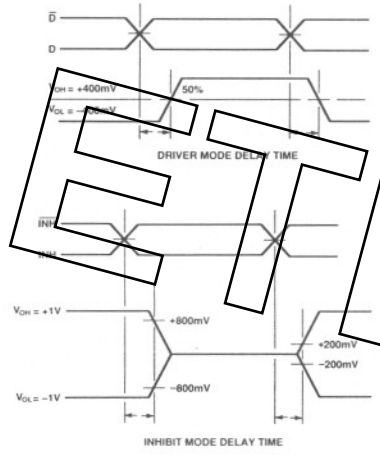


Figure 2. Timing Diagram for Driver and Inhibit Propagation Delay

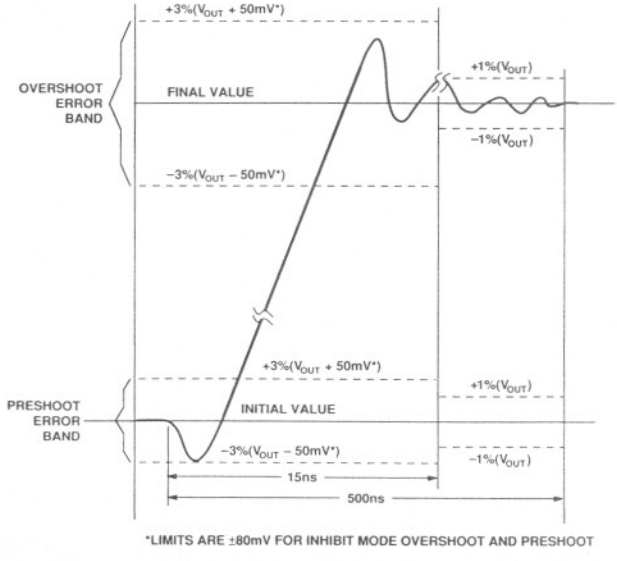


Figure 3. Definition of Waveform Abberations

Typical Performance Characteristics

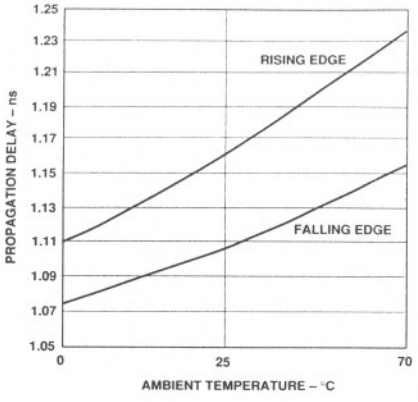


Figure 4. Driver Propagation Delay vs. Temperature

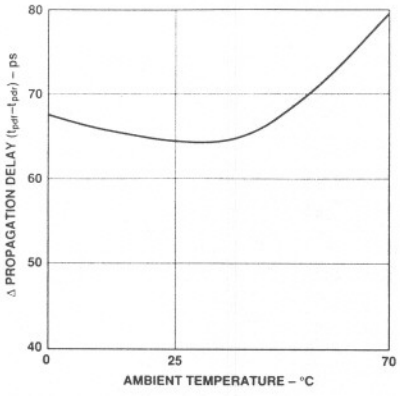


Figure 5. Propagation Delay Edge Matching vs. Temperature

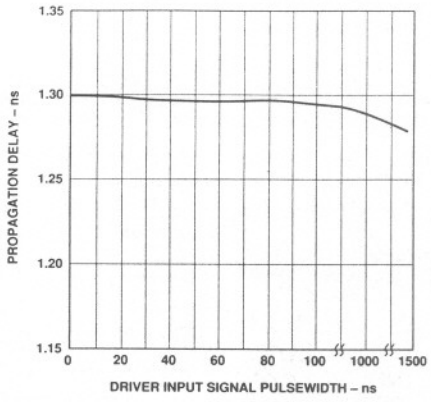


Figure 6. Propagation Delay vs. Input Signal Pulsewidth

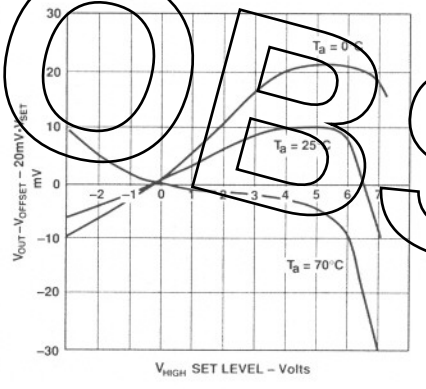


Figure 7. Change in V_{HIGH} over Temperature

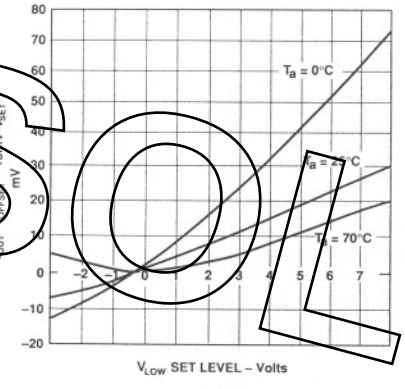


Figure 8. Change in V_{LOW} over Temperature

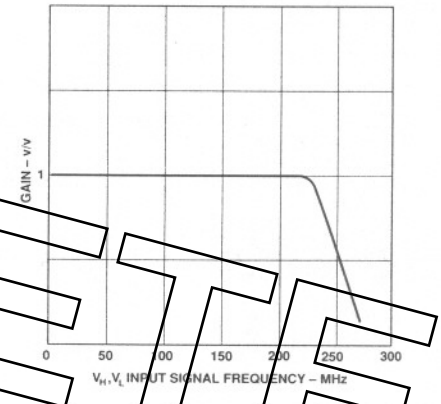


Figure 9. V_{HIGH}, V_{LOW} Input Bandwidth

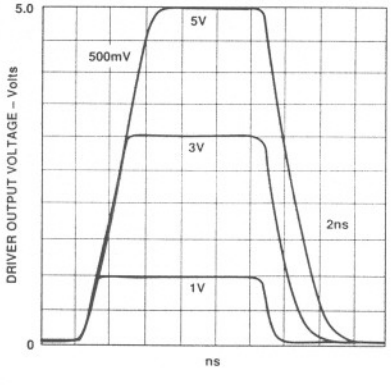


Figure 10. 10 ns Output Pulse at 1 V, 3 V and 5 V

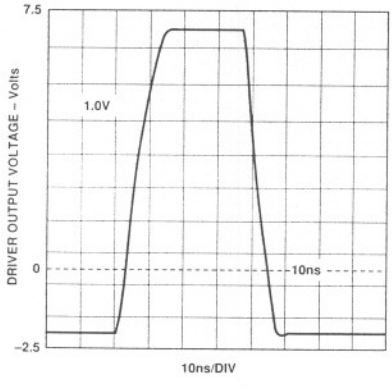


Figure 11. V_{OUT} = 9 V as Seen at the End of a 28", 50 Ω Cable

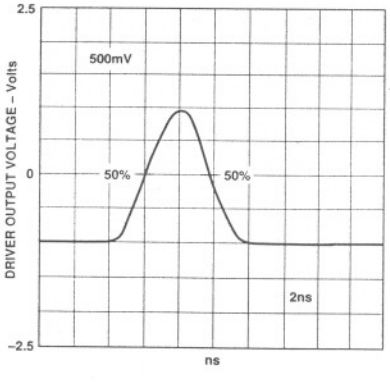


Figure 12. Minimum (Data) Pulsewidth as Defined by V_{OUT} = 2 V, 50% Crossing ≤ 2 ns

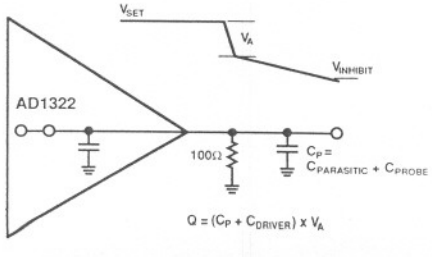


Figure 13. Charge into Inhibit Test Setup

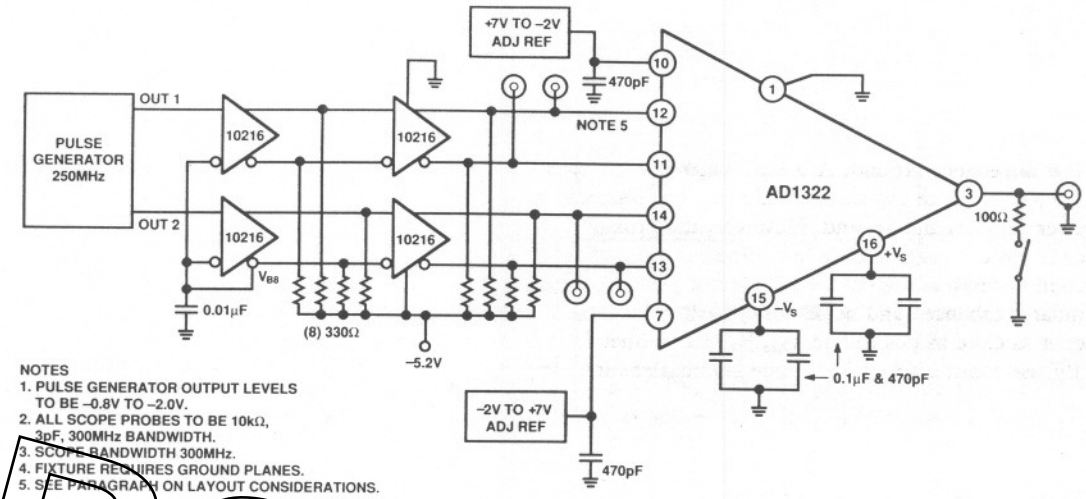


Figure 14. AD1322 Test Setup

FUNCTIONAL DESCRIPTION

The AD1322 is a complete high speed pin driver designed for use in general purpose instrumentation and digital functional test equipment. The purpose of a pin driver is to accept digital, analog and timing information from a system source and combine these to drive the device to be tested.

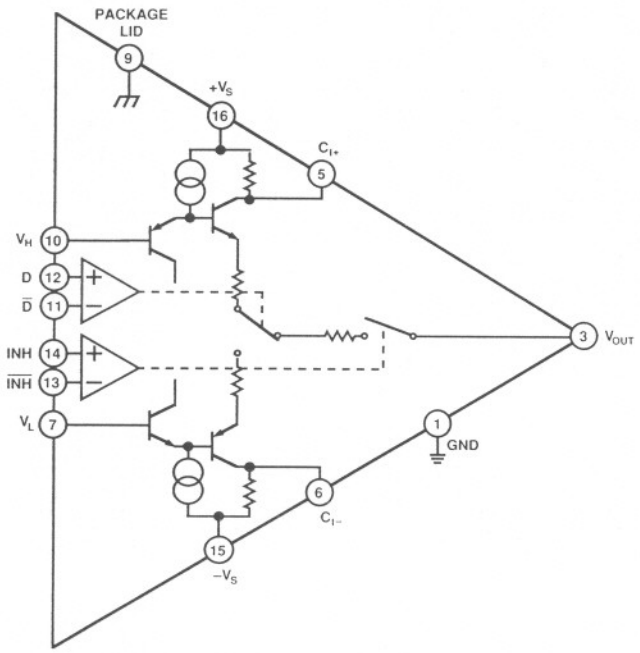


Figure 15. AD1322 Block Diagram

The circuit configuration for the AD1322 is outlined in Figure 15. Simply stated, a pin driver performs the function of a precise, high speed level translator with an output which can be disabled. The AD1322 accepts differential digital information utilizing a high speed differential design on the D and INH inputs providing precise timing at logic crossover and high noise immunity. The wide input voltage range allows for ECL operation with power supplies at 0 to −5.2 V, +2 V to −3.2 V or +5 V to 0 V. Where timing is less critical TTL or CMOS logic levels may be used to toggle the AD1322. By biasing the D and INH inputs to approximately +1.3 V for TTL and 1/2 V_{CC} for CMOS, the D and INH inputs can be directly driven from these single-ended output sources. The output of the pin driver will follow the logic state of the D input providing the INH input is low. When inhibit is asserted the output is disconnected and any activity on the input does not affect the output.

Analog information is provided to the pin driver through the V_H and V_L terminals as reference voltages. These analog voltages are buffered internally using unity gain followers. The resulting gain and linearity errors are provided in the specification table. System timing requirements are achieved through a specified 1.2 ns, ±200 ps driver propagation delay, 2.0 V/ns slew rate, defined preshoot and overshoot, and a dynamically trimmed 50 Ω output impedance.

LAYOUT CONSIDERATIONS

While it is generally considered good engineering practice to capacitively decouple the power supplies of an active device, it is absolutely essential for a high power, high speed device such as the AD1322. The engineer merely has to consider the current pulse demand from the power supply when a dynamic current change of −100 mA to +100 mA is required in only a few nanoseconds. Therefore, a 470 pF high frequency decoupling capacitor must be located within 0.25 inches of the $+V_S$ and $-V_S$ terminals to a low impedance ground. A 0.1 μF capacitor in parallel with a 10 μF tantalum capacitor should also be situated between the power supplies and ground. However, the proximity to the device is less critical assuming low impedance power supply distribution techniques are employed. Circuit performance will be similarly enhanced and noise minimized by locating a 470 pF capacitor as close as possible to V_H, V_L and connected to ground. Bypass considerations have been summarized in Figure 16.

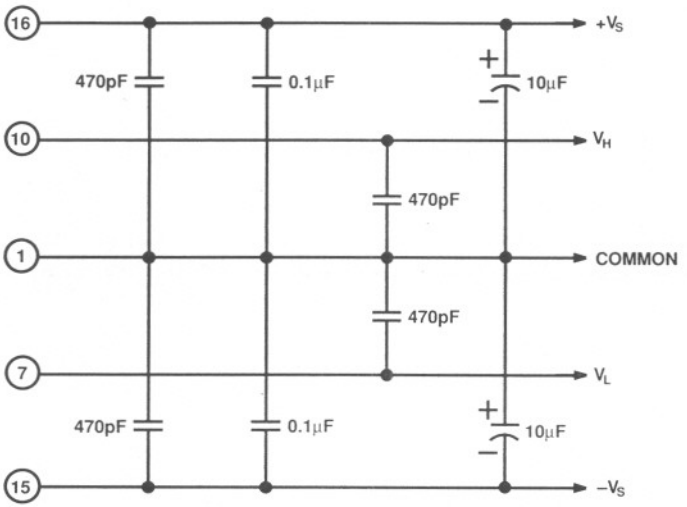


Figure 16. Basic Circuit Decoupling

An equally important consideration is the use of microwave stripline techniques on the output of the AD1322. Failure to preserve the 50 Ω output impedance of the pin driver will result in unwanted reflections, ringing and general corruption of the wave shape. Care should be exercised when selecting etch widths and routing, wire and cable to the device to be tested, and in choosing relays if they are required.

THERMAL CONSIDERATIONS

The AD1322 is provided in a 0.450″ × 0.450″, 16 lead (bottom brazed) gull wing, surface mount package with a typical junction-to-case thermal resistance of 5.6°C/W. Thermal resistance θ_{CA} (case to ambient) vs. air flow for the AD1322 in this package is shown in Figure 17. The improvement in thermal resistance vs. air flow begins to flatten out just above 400 lfm[1, 2].

NOTES

[1]lfm is air flow in Linear Feet/Minute.

[2]For convection cooled systems, the minimum recommended airflow is 400 lfm.

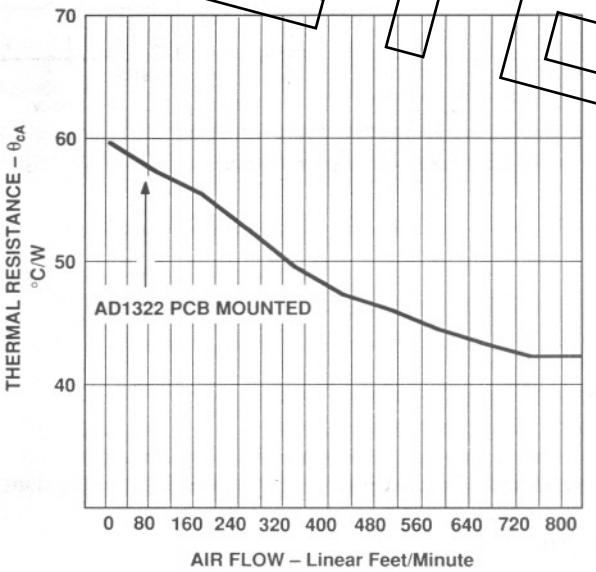


Figure 17. Case-to-Ambient Thermal Resistance vs. Air Flow

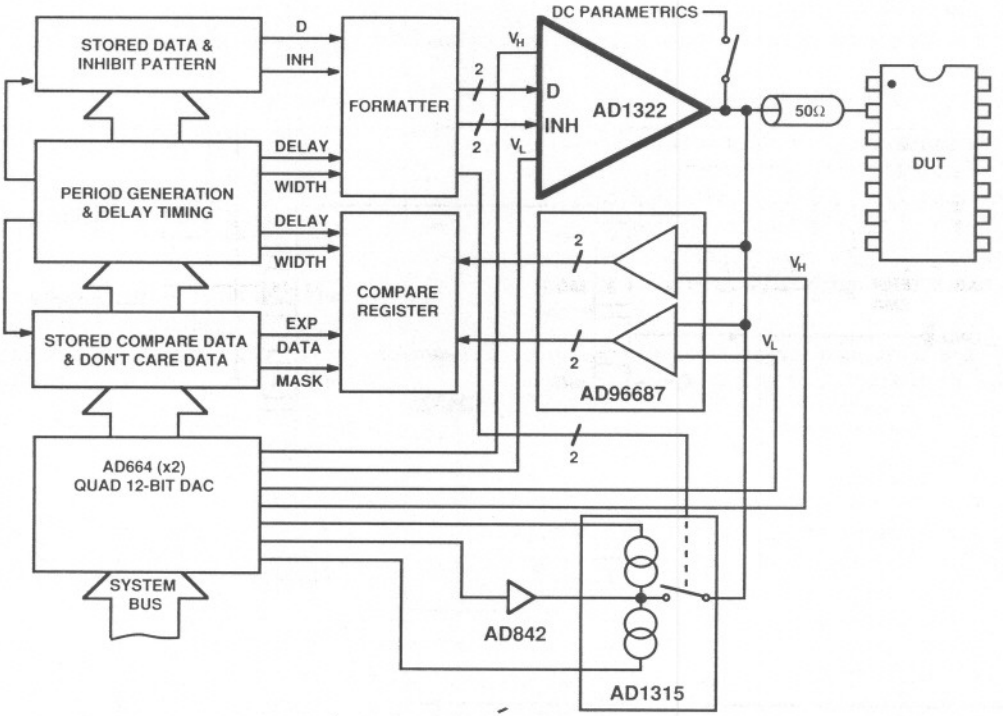
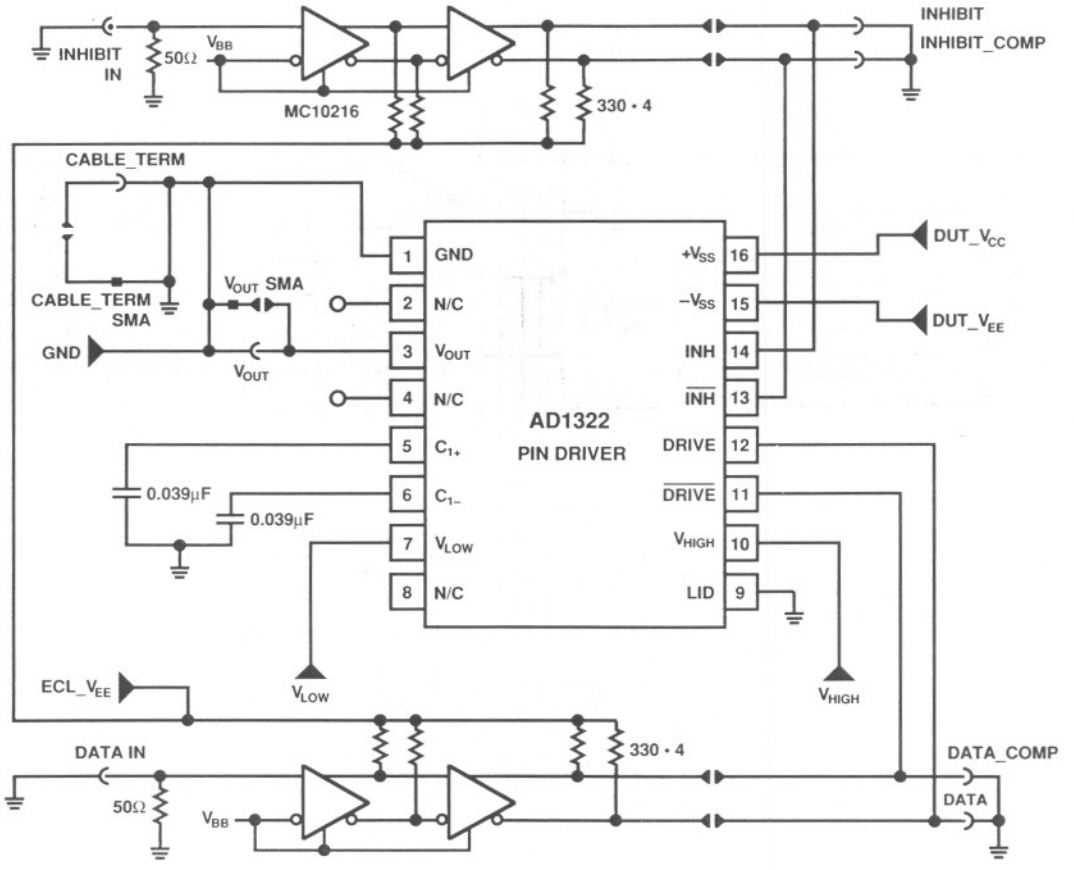


Figure 18. High Speed Digital Test System Block Diagram

APPLICATIONS

The AD1322 has been optimized to function as a pin driver in an ATE test system. Shown in Figure 18 is a block diagram illustrating the electronics behind a single pin of a high speed digital functional test system with the ability to test I/O pins on logic devices. The AD1322 pin driver, AD96687 high speed dual comparator, AD1315 active load, and the AD664 quad 12-bit voltage DAC would comprise the pin electronic portion of the test system. Such a system could operate at 200 MHz in a data mode or 100 MHz in the I/O mode, yet fit into a neat trim package.



NOTES:
"HALF-MOON" CONNECTORS CAN BE CONNECTED OR DISCONNECTED AS REQUIRED . . . ◀▶
DECOUPLING CAPS ARE NOT SHOWN ON THIS SCHEMATIC, BUT THE BOARD USES 0.1μF AND 470pF CAPS TO DECOUPLE THE V_{CC}, V_{EE}, V_{LOW} AND V_{HIGH} SUPPLIES.
SMA CONNECTORS ■
PROBE JACKS)
BNC CONNECTORS (●

Figure 19. AD1322EB Evaluation Board Schematic

AD1322 EVALUATION BOARD

Introduction

The AD1322EB evaluation board was developed to aid the customer in quickly evaluating the performance of the AD1322. Included is complete documentation of the evaluation board along with suggestions on equipment to use and measurement limitations.

Overview

The AD1322 is a high speed pin driver used in automatic test equipment

The device has true differential inputs for both the drive and inhibit which can be driven from either TTL or ECL logic levels (ECL is recommended). Standard ECL design and layout techniques should be used.

The device runs from dual power supplies +10 V and −5.2 V. It is very important that these power supplies are decoupled properly at the device pin. (High frequency oscillations will couple through to the device output.)

The reference input pins are dc inputs; therefore they also should be decoupled properly. The reference input range is −2 V to +7 V.

The output slew rate is 1 V/ns for large signals and has a rep rate for an ECL level of 100 MHz minimum.

Equipment

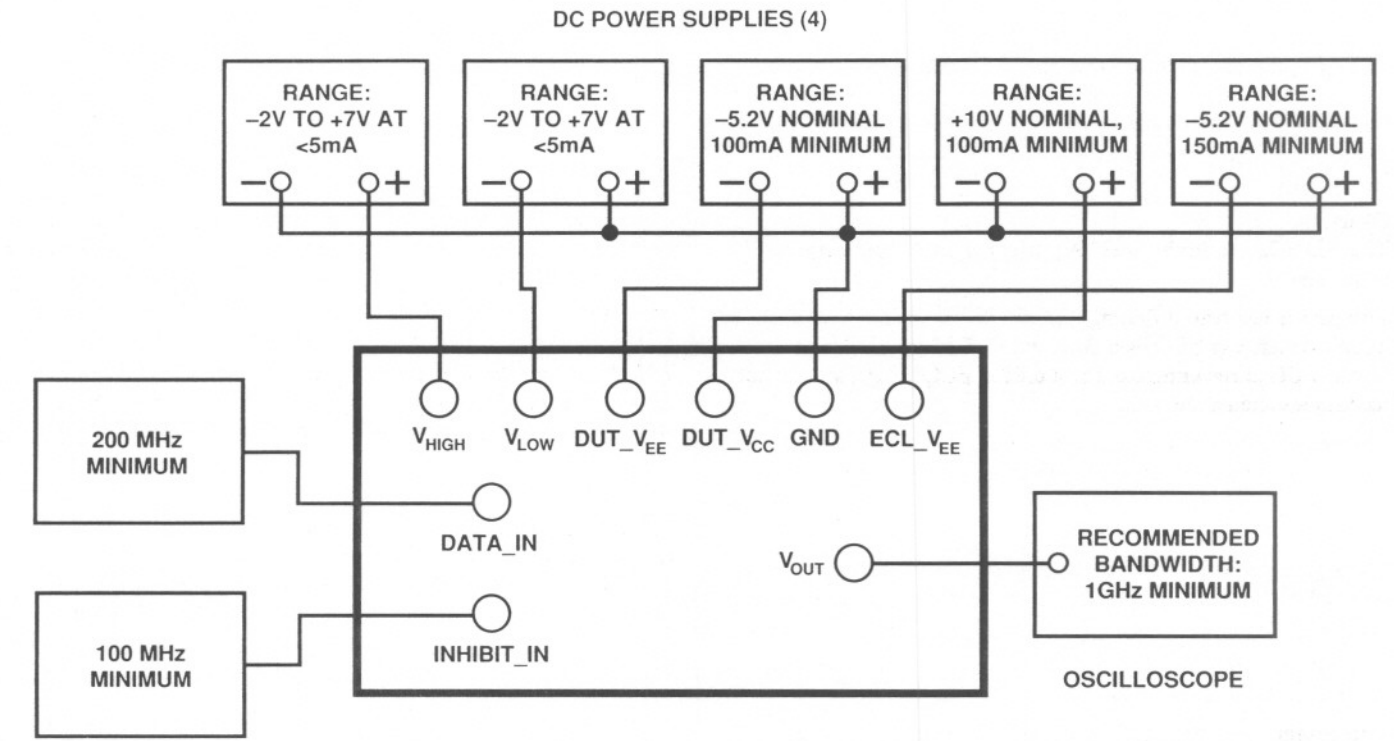
The Drive and Inhibit inputs should be driven with standard ECL levels. If the full performance of the AD1322 needs to be evaluated, the generator must be able to supply an ECL level at frequencies greater than 200 MHz. Motorola's MC10216 is used on the evaluation board to simulate the actual application. V_{BB} is used on the MC10216 as the logic reference and the outputs have 330 ohm pulldowns to V_{EE}.

Five power supplies are required: DUT_V_{CC}, DUT_V_{EE}, V_{HIGH}, V_{LOW} and ECL_V_{EE}. DUT_V_{CC} requires +10 V at 100 mA minimum; DUT_V_{EE} requires −5.2 V at 100 mA minimum; ECL_V_{EE} requires −5.2 V at 150 mA minimum. V_{HIGH} and V_{LOW} require −2 V to +7 V at 5 mA (each).

The output performance of the pin driver can only be measured properly with a scope which has the proper bandwidth for the required application. The input impedance and the bandwidth of the scope probe should be taken into consideration when evaluating the performance of the device. The resultant bandwidth of the system is the RMS value of the components in the system.

The characterizations performed by Analog Devices were performed using the following equipment: the scope equipment consists of the Tektronix 11402 mainframe (1 GHz BW), P6203 FET probe (1 GHz, 1.2 pF, 1 M ohm) and the 11A71 plug-in (1 GHz BW, 50 ohm).

The Hewlett-Packard 54120 and 54110 were also evaluated with the 500 ohm, 1.2 pF passive probes and the Data Precision 6100 with their model 640 FET probe (50 kΩ, 4 pF). When measuring the performance of waveforms close to or exceeding the bandwidth of a scope, it is not uncommon for the results between scopes to be different because of aberrations and slew rates.



CONNECTORS ON AD1322 EVALUATION BOARD:

1. DC POWER SUPPLIES: FEMALE BANANA JACKS
2. PULSE GENERATORS: FEMALE BNC CONNECTORS
3. OSCILLOSCOPE: FEMALE PROBE SOCKET (TEKTRONIX p/n: 131–0258–00)

Figure 20. AD1322 Evaluation Board Connections