Four-Channel 12-Bit Sampling A/D Converter for Digital Signal Processing

AD1334

FEATURES

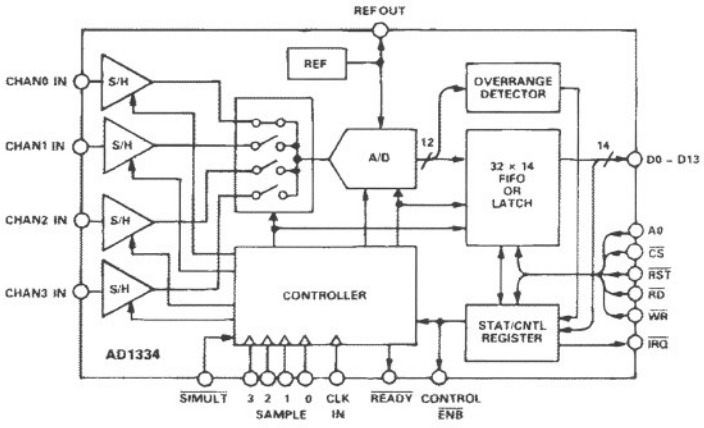
Four-Channel A/D Converter for DSP Includes:
- Simultaneous or Independent Sampling Capability
- 12-Bit Accurate A/D Converter
- 2-Bit Channel ID Tags Each Conversion Result
- 32-Word FIFO Memory
- Fully Asynchronous, High Speed Digital Interface

Single-Channel Sample Rate Up to 67 kHz
Four-Channel Simultaneous Sample Rate Up to 28 kHz
Entire System Dynamically Characterized
Minimal Effective Aperture Delay Mismatch from Channel-to-Channel & Device-to-Device
15 ns Data Access Time Allows "No Wait State" Interface to: ADSP-2100 (A), TMS320C25 DSP56000, NECμPD77230
Low Power, 250 mW/Channel

APPLICATIONS

Sonar Signal Processing
Robotics/Machine Control
Disk-Drive Head Positioning
Vibration Analysis

BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD1334 is a four-channel, 12-bit, sampling A/D converter system optimized for use in multichannel digital signal processing (DSP) applications. The device consists of four independent sample-and-hold amplifiers, a multiplexer, an A/D converter, a controller, a 32-word FIFO memory and a fully asynchronous high speed digital interface. The product is packaged in a 40-pin hermetic DIP.

The channel controller enables the AD1334 to appear as four independent channels of analog input by generating all of the timing necessary to ensure that the sampled channel is digitized to 12-bit accuracy. Upon receipt of a sample command, the controller will immediately place the sample-and-hold amplifier into hold mode and then prioritize and schedule the held value for A/D conversion. At the appropriate time, the sampled input is gated through the multiplexer and, after settling, is digitized by the A/D converter. The sample-and-hold amplifier is then returned to sample mode so that it can acquire the next sample.

For effective use in simultaneous sampling applications, the sample-and-hold amplifiers are designed to provide a minimum amount of aperture delay time mismatch from channel-to-channel and device-to-device.

The 12-bit A/D converter can convert ±5 V full scale signals at sample rates up to 67 kHz for single-channel operation. In the simultaneous mode, the AD1334 has a four-channel sample rate up to 28 kHz. The entire converter system is specified and tested for signal-to-noise ratio, total harmonic distortion and channel-to-channel isolation.

The digital interface provides a true asynchronous link between the A/D and a high speed microprocessor. Data transfer is controlled by generating an interrupt signal when data is available. Interrupts can be generated when the FIFO is full (32 words), half-full (16 words), or when a single word of data is ready (FIFO bypassed). The AD1334 can also generate an interrupt when the A/D conversion results are overrange.

The AD1334 provides a completely specified and tested system that bridges the interface and specification gap between A/D converters and high speed DSP.

REV. A

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 617/329-4700 Fax: 617/326-8703 Twx: 710/394-6577
Telex: 924491 Cable: ANALOG NORWOODMASS

AD1334—SPECIFICATIONS (T_A = +25°C, V_S = ±15 V, V_{DD} = +5 V and f_{CLK} = 2.5 MHz unless noted)

	AD1334BD			AD1334TD			
	Min	Typ	Max	Min	Typ	Max	Units
S/H, MUX & A/D CONVERTER[1]							
Input Impedance	2	2.5		2	2.5		kΩ
Voltage Range		−5 to +5			−5 to +5		V
Output Coding		Offset Binary			Offset Binary		
CLK IN Frequency, (f_{CLK})	1.0		2.5	1.0		2.5	MHz
High Time	200			200			ns
Low Time	200			200			ns
Sampling Rate Per Channel (f_S)							
Simultaneous Mode ($\overline{SIMULT}$ = LOW)							
1 Channel			67			67	kHz
2 Channels			46			46	kHz
3 Channels			35			35	kHz
4 Channels			28			28	kHz
Independent Mode ($\overline{SIMULT}$ = HIGH)							
1 Channel			67			67	kHz
2 Channels			67			67	kHz
3 Channels			44			44	kHz
4 Channels			33			33	kHz
S/H							
Acquisition Time to 0.01%		6.5	7.5		6.5	7.5	µs
Droop Rate		0.2	1.0		0.2	1.0	mV/ms
Over Temperature		Doubles Every 10°C			Doubles Every 10°C		
−3 dB Small Signal Bandwidth		200			200		kHz
Group Delay[2] (f_{IN}<10 kHz)		785			785		ns
Aperture Delay[3]	0	10	15	0	10	15	ns
Effective Aperture Delay[4] (f_{IN}<10 kHz)	−700	−775	−850	−700	−775	−850	ns
Static Characteristics							
Integral Linearity Error		±1/2	±1		±1/2	±1	LSB
Over Temperature			±1			±1 1/2	LSB
Differential Linearity Error			±1			±1	LSB
Over Temperature			±1			±2	LSB
−Full-Scale Error		±2	±4		±2	±4	LSB
Over Temperature		±4	±8		±4	±13	LSB
+Full-Scale Error		±2	±4		±2	±4	LSB
Over Temperature		±4	±8		±4	±13	LSB
PSRR, $\pm V_S$		±1/2			±1/2		LSB/V
Dynamic Characteristics[5, 6]							
Signal-to-Noise Ratio, f_{IN} = 13.6 kHz	70	72		70	72		dB
Total Harmonic Distortion, f_{IN} = 13.6 kHz		−86	−76		−86	−76	dB
Intermodulation Distortion, f_{IN1} = 13.1 kHz & f_{IN2} = 13.6 kHz		−86	−76		−86	−76	dB
Channel-to-Channel Isolation[7], f_{IN} = 8.009 kHz							
$\overline{SIMULT}$ = LOW	70	78		70	78		dB
$\overline{SIMULT}$ = HIGH		74			74		dB
Reference Voltage	−5.05		−4.95	−5.05		−4.95	V
Output Current	±1	±2		±1	±2		mA
Drift		±10	±30		±10	±30	ppm/°C

	AD1334BD			AD1334TD			
	Min	Typ	Max	Min	Typ	Max	Units
DIGITAL INPUTS[6]							
Voltage Input, LOW			+0.8			+0.8	V
HIGH	+2.0			+2.25			V
Input Current			±250			±250	μA
Input Capacitance		5			5		pF
$\overline{RST}$ LOW Pulse Width	10			10			ns
DIGITAL OUTPUTS[6]							
D0–D13, $\overline{READY}$							
Output Voltage, Logic LOW[8]			+0.4			+0.4	V
Output Voltage, Logic HIGH[8]	+2.4			+2.4			V
3-State Leakage Current			±250			±250	μA
$\overline{IRQ}$, CONTROL $\overline{ENB}$							
Output Voltage, Logic LOW[8]			+0.4			+0.4	V
$\overline{IRQ}$ Off-State Leakage			±10			±10	μA
Output Capacitance		5			5		pF
FIFO Fall-Thru Time		400	800		400	800	ns
$\overline{IRQ}$ LOW to D0–D13 Valid[9]			0			0	ns
POWER REQUIREMENTS							
Operating Range							
$\pm V_S$	±11.4		±15.75	±11.4		±15.75	V
V_{DD}	+4.75		+5.25	+4.75		+5.25	V
Supply Current							
$+V_S$		47	60		47	60	mA
$-V_S$		39	50		39	50	mA
$+V_{DD}$		7	15		7	15	mA
Consumption							
$\pm V_S = \pm 12$ V		1.0	1.2		1.0	1.2	W
$\pm V_S = \pm 15$ V		1.25	1.5		1.25	1.5	W
TEMPERATURE RANGE							
Operating and Specified	−40		+85	−55		+125	°C
Storage	−65		+150	−65		+150	°C

NOTES

[1]Specifications are per channel in 4 Channel Simultaneous Mode (SAMPLE 0–3 connected together and $\overline{SIMULT}$ & CONTROL $\overline{ENB}$ = LOW), at f_S = 28 kHz, and with SAMPLE 0–3 having an 80% duty cycle unless noted.

[2]Group delay is the negative of the 1st derivative of phase with respect to frequency and is a measure of the analog time delay through the S/H.

[3]Aperture delay is the time delay from the SAMPLE input to S/H switch opening and is a measure of the digital time delay through the S/H.

[4]Effective aperture delay is the difference between analog and digital time delays described in (2) and (3).

[5]THD of harmonics 2–7 of the fundamental. SNR of fundamental less harmonics 2–7.

[6]Guaranteed over operating temperature and power supply voltage range.

[7]Isolation of any one channel from remaining three channels which have near maximum amplitude ac signals at their inputs.

[8]I_{OL} = 4 mA for AD1334BD, I_{OL} = 3.2 mA for AD1334TD; I_{OH} = −4 mA for AD1334BD, I_{OH} = −3.2 mA for AD1334TD.

[9]$\overline{RD}$, $\overline{CS}$, A0 = LOW; $\overline{WR}$, $\overline{RST}$ = HIGH.

Specifications subject to change without notice.

ORDERING GUIDE

Model	Temperature Range	Package Option*
AD1334BD	−40°C to +85°C	DH-40A
AD1334TD/883B	−55°C to +125°C	DH-40A

*D = Hermetic Ceramic DIP.

AD1334

SWITCHING CHARACTERISTICS (over operating temperature and power supply voltage range, with C_{OUT} = 30 pF or 100 pF except where noted)

Parameter	Description	Conditions	Min	Max	Units
READ CYCLE					
t_{RC}	Read Cycle Time	C_{OUT} = 30 pF	25		ns
		C_{OUT} = 100 pF	35		ns
t_A	Data Access Time	C_{OUT} = 30 pF		15	ns
		C_{OUT} = 100 pF		25	ns
t_{LZ}	Output Low Z Time		2		ns
t_{HZ}	Output High Z Time	C_{OUT} = 30 pF		15	ns
		C_{OUT} = 100 pF		25	ns
t_{OH}	Output Hold Time		2		ns
t_{A0RD}	A0 Valid to $\overline{RD}$ LOW		3		ns
t_{RDA0}	$\overline{RD}$ HIGH to A0 Invalid		3		ns
t_{A0CS}	A0 Valid to $\overline{CS}$ LOW		3		ns
t_{CSA0}	$\overline{CS}$ HIGH to A0 Invalid		3		ns
WRITE CYCLE					
t_{WC}	Write Cycle Time		15		ns
t_{WP}	Write Pulse Width		5		ns
t_{SU}	Data Setup Time		2		ns
t_H	Input Hold Time		4		ns
t_{A0WR}	A0 Valid to $\overline{WR}$ LOW		3		ns
t_{WRA0}	$\overline{WR}$ HIGH to A0 Invalid		3		ns
t_{A0CS}	A0 Valid to $\overline{CS}$ LOW		3		ns
t_{CSA0}	$\overline{CS}$ HIGH to A0 Invalid		3		ns

Specifications subject to change without notice.
All specifications are guaranteed but not tested.

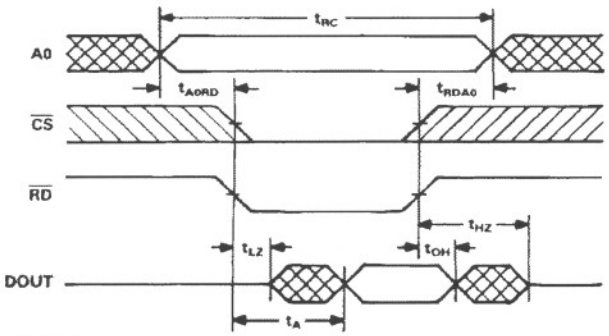
ABSOLUTE MAXIMUM RATINGS*

$+V_S$ to APWR/ASIG GND . . . . . +18 V
$-V_S$ to APWR/ASIG GND . . . . . −18 V
V_{DD} to DGND . . . . . +7 V
APWR/ASIG GND to DGND . . . . . −0.3 V to +0.3 V
Analog Input to APWR/ASIG GND . . . . . $-V_S$ to $+V_S$
Digital Input to APWR GND
SAMPLE0–SAMPLE3, CLK IN, $\overline{SIMULT}$, CONTROL $\overline{ENB}$ . . . . . −0.3 V to +7 V
Digital Input to DGND
D0–D13, $\overline{RD}$, $\overline{WR}$, $\overline{CS}$, A0, $\overline{RST}$ . . −0.3 V to V_{DD}+0.3 V
Output Short Circuit Duration
REF OUT, TP . . . . . Indefinite
Digital Output . . . . . 1 Output for 1 sec
Lead Temperature Range,
Soldering for 10 sec . . . . . +300°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum conditions for extended periods may affect device reliability.

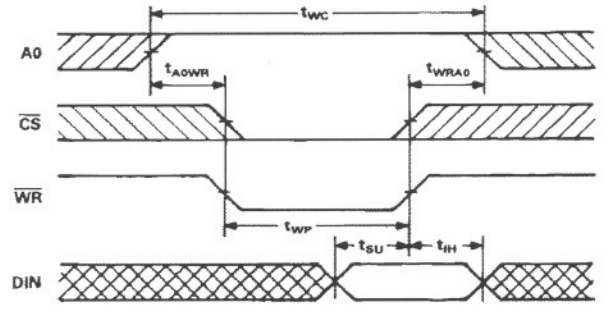
CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.



NOTES
CS IS VALID BEFORE OR COINCIDENT WITH RD HIGH-TO-LOW TRANSITION.
CS IS INVALID AFTER OR COINCIDENT WITH RD LOW-TO-HIGH TRANSITION.
WR IS NOT ACTIVE DURING READ CYCLE.

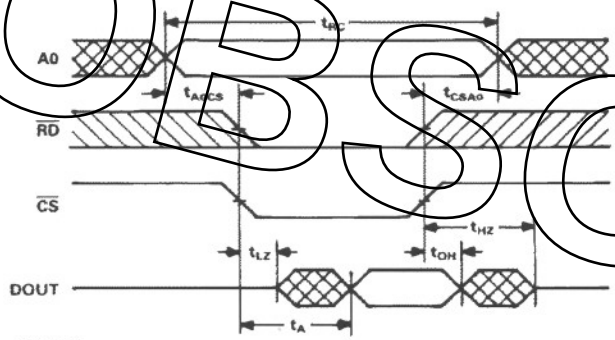
Timing Waveform for Read Cycle No. 1 (RD Controlled)



NOTES
CS IS VALID BEFORE OR COINCIDENT WITH WR HIGH-TO-LOW TRANSITION.
CS IS INVALID AFTER OR COINCIDENT WITH WR LOW-TO-HIGH TRANSITION.
RD IS NOT ACTIVE DURING WRITE CYCLE.

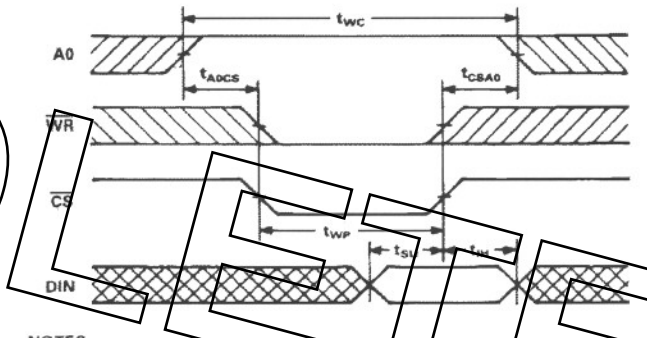
Timing Waveform for Write Cycle No. 1 (WR Controlled)

Figure 1.



NOTES
RD IS VALID BEFORE OR COINCIDENT WITH CS HIGH-TO-LOW TRANSITION.
RD IS INVALID AFTER OR COINCIDENT WITH CS LOW-TO-HIGH TRANSITION.
WR IS NOT ACTIVE DURING READ CYCLE.

Timing Waveform for Read Cycle No. 2 (CS Controlled)



NOTES
WR IS VALID BEFORE OR COINCIDENT WITH CS HIGH-TO-LOW TRANSITION.
WR IS INVALID AFTER OR COINCIDENT WITH CS LOW-TO-HIGH TRANSITION.
RD IS NOT ACTIVE DURING WRITE CYCLE.

Timing Waveform for Write Cycle No. 2 (CS Controlled)

Figure 2.

AC TEST CONDITIONS

Input Pulse Levels	DGND to +3.0 V
Input Rise/Fall Times	<5 ns
Timing Reference Levels	
Inputs	1.5 V
Outputs	
LOW	0.4 V
HIGH	2.4 V
Enabled to LOW	V_T − 0.1 V
Enabled to HIGH	V_T + 0.1 V
Disabled from LOW	V_{OL} + 0.5 V
Disabled from HIGH	V_{OH} − 0.5 V

V_T = 1.5 V, the voltage to which 3-stated outputs are forced.

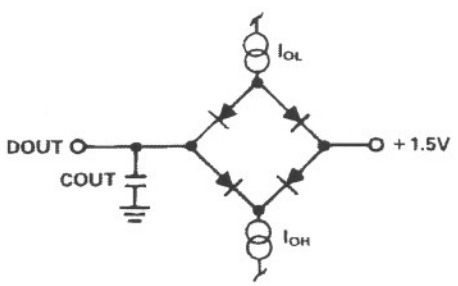


Figure 3. Output Load

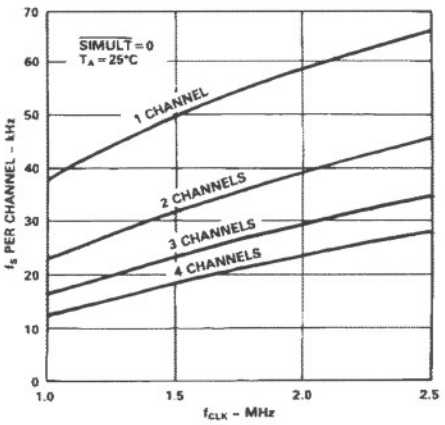


Figure 4. Maximum Sample Rate vs. Clock Frequency (Simultaneous Mode)

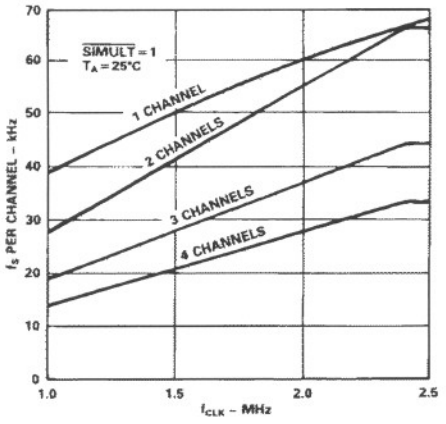


Figure 5. Maximum Sample Rate vs. Clock Frequency (Independent Mode)

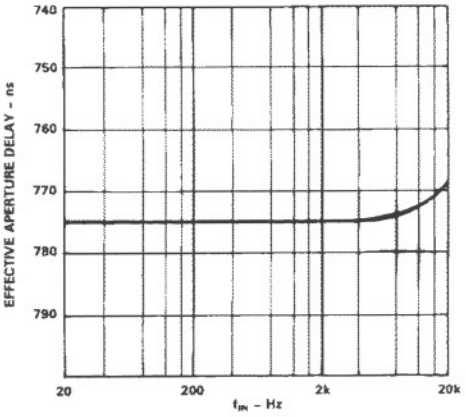


Figure 6. Effective Aperture Delay vs. Frequency

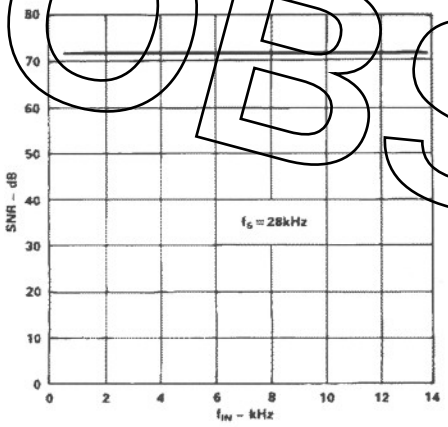


Figure 7. A/D SNR vs. Frequency (Average of Four Channels, Simultaneous Mode)

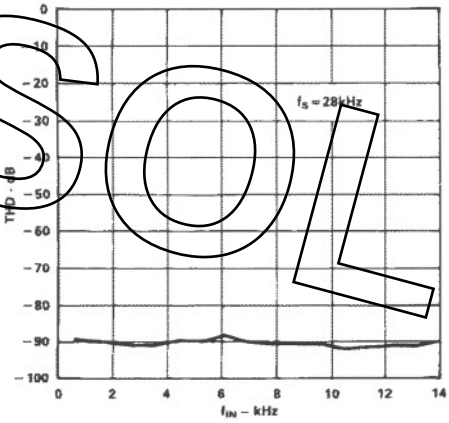


Figure 8. A/D THD vs. Frequency (Average of Four Channels, Simultaneous Mode)

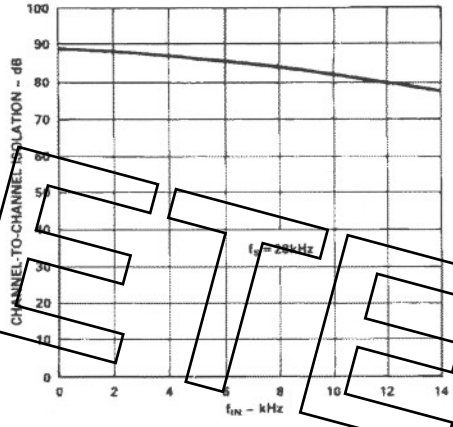


Figure 9. Channel-to-Channel Isolation vs. Frequency

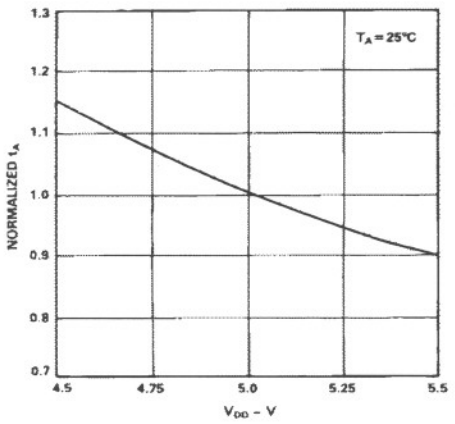


Figure 10. Normalized Data Access Time vs. V_{DD}

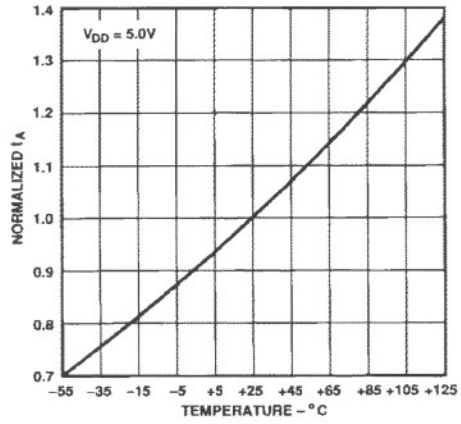


Figure 11. Normalized Data Access Time vs. Temperature

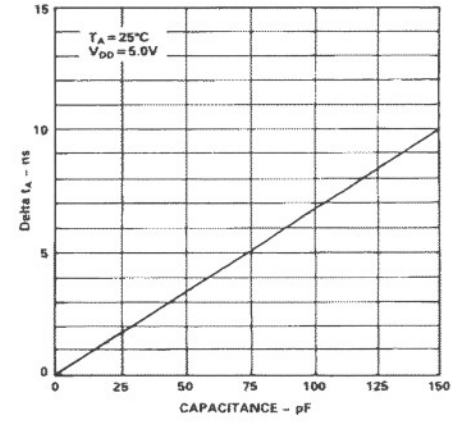
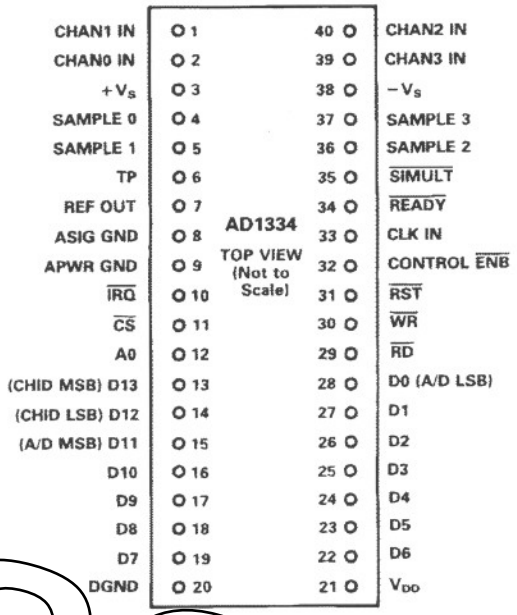


Figure 12. Change in Data Access Time vs. Loading

PIN CONFIGURATION



PIN DESCRIPTIONS

Pin	Mnemonic	Function
2	CHAN 0 IN	Channel 0 analog input.
1	CHAN 1 IN	Channel 1 analog input.
40	CHAN 2 IN	Channel 2 analog input.
39	CHAN 3 IN	Channel 3 analog input.
6	TP	Test Point (no connect).
32	CONTROL $\overline{ENB}$	Input and (open drain) output used to enable controller externally or through µP interface.
34	$\overline{READY}$	Output that, in simultaneous mode, indicates all channels have been successfully converted and device is ready to sample.
35	$\overline{SIMULT}$	Input that when LOW sets controller to simultaneous mode which keeps S/Hs in hold mode until all channels have been converted.
8	ASIG GND	Analog signal ground.
7	REF OUT	−5V reference output.
3, 38	$+V_S$, $-V_S$	Analog power supplies.
9	APWR GND	Analog power ground.
33	CLK IN	External clock input to the A/D converter and channel controller.
4	SAMPLE 0	Channel 0 S/H control input.
5	SAMPLE 1	Channel 1 S/H control input.
36	SAMPLE 2	Channel 2 S/H control input.
37	SAMPLE 3	Channel 3 S/H control input.
10	$\overline{IRQ}$	Open drain interrupt request. User programmable to become active on any of the following conditions: One A/D Conversion Result Available; FIF0 Half Full or Full; A/D Conversion Results Over range.
11	$\overline{CS}$	Chip select input.
12	A0	Address bit zero. Selects data path from FIFO/latch (low) or from/to Status/Control register (high).
28–22	D0–D6	Bidirectional 3-state data lines. D11 is A/D converter MSB when D0–D13 are outputs. D7 is Status/
19–13	D7–D13	Control register MSB. D12 and D13 carry channel ID number.
29	$\overline{RD}$	Read control input (D0–D13).
30	$\overline{WR}$	Write control input (D0–D7).
31	$\overline{RST}$	Reset. In reset state, FIFO is transparent & overrange detector is disabled.
20, 21	DGND, V_{DD}	Digital power supply.

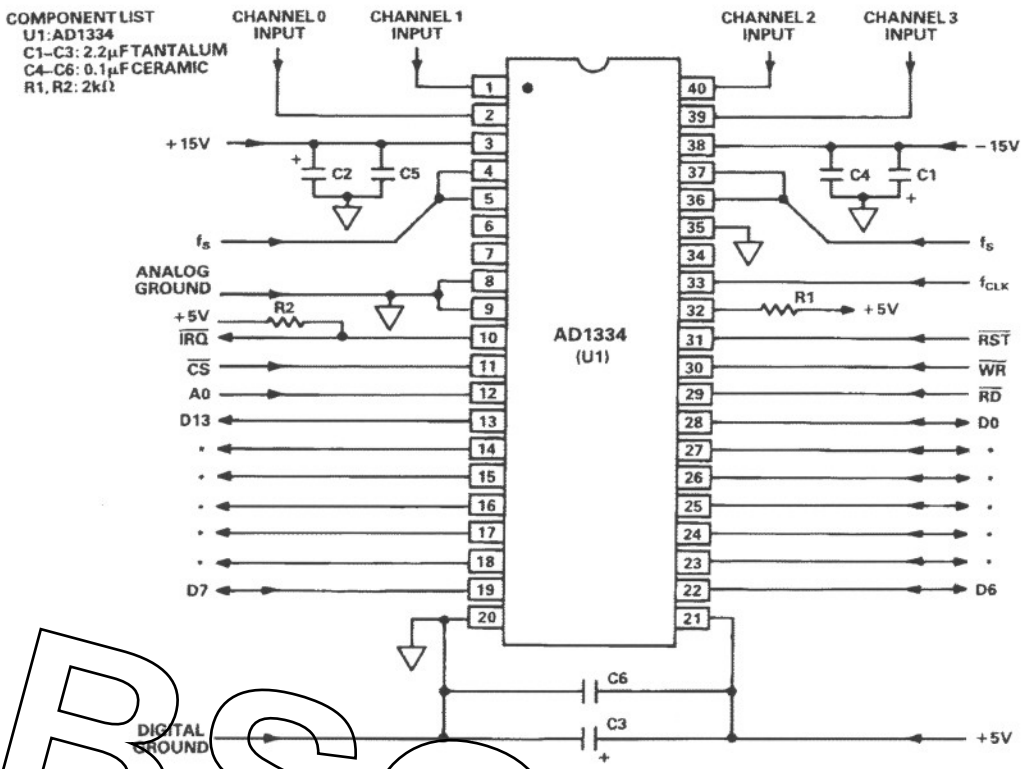


Figure 13. Typical Interface Circuit (Simultaneous Mode)

CONTROL AND STATUS REGISTER DESCRIPTIONS

Control

Bit →	7	6	5	4	3	2	1	0
	CTLEN	$\overline{L}$/F	$\overline{HF}$/F	ORNG	X	X	X	X

Bit	Mnemonic	Function
7	CTLEN	A "0" in this bit position will disable the controller. A "1" in this bit position will enable the controller.
6	$\overline{L}$/F	A "0" in this bit position will reset the FIFO and enable the transparent latch. $\overline{IRQ}$ will become active on the completion of an A/D conversion cycle. $\overline{IRQ}$ will become inactive on the start of the next A/D conversion cycle or at the start of a read cycle, whichever happens first. A "1" in this bit position will enable the FIFO and activate $\overline{IRQ}$ when the FIFO is half full or full (depending on CBIT 5). $\overline{IRQ}$ will become inactive on the start of the next A/D conversion cycle or when the FIFO is read from.
5	$\overline{HF}$/F	A "0" in this bit position will cause $\overline{IRQ}$ to become active when the 16th word is shifted into the FIFO (if the FIFO is enabled). A "1" in this bit position will cause $\overline{IRQ}$ to become active when the 32nd word is shifted into the FIFO (if the FIFO is enabled).
4	ORNG	A "0" in this bit position will disable the overrange interrupt capability. A "1" in this bit position will activate $\overline{IRQ}$ if overranged (all "0"s or all "1"s) data is shifted into the FIFO. $\overline{IRQ}$ will become inactive when this bit is reset to "0."
3-0	X	Not defined.

Status

Bit →	7	6	5	4	3	2	1	0
	FLAG	DATA	ORUN	ORNG	X	X	X	X

Bit	Mnemonic	Function
7	FLAG	Logical OR of status Bits 4 & 6.
6	DATA	Set if $\overline{IRQ}$ becomes active because data is available. Reset when FIFO is read from if FIFO used. Reset when $\overline{IRQ}$ becomes inactive if latch is used.
5	ORUN	Set when FIFO has overrun. Reset by control Bit 6.
4	ORNG	Set if $\overline{IRQ}$ became active because of overrange condition. Reset by control Bit 4.
3-0	X	Not defined.

SAMPLE-AND-HOLD AMPLIFIERS

The four sample-and-hold amplifiers internal to the AD1334 combine precision high speed amplifiers and switches together with laser trimmed thin-film resistors to offer a performance and power efficient front end for multichannel applications. Each sample-and-hold amplifier is designed to minimize the effects of dc and ac error sources in simultaneous as well as independent sampling applications.

Operational Description

The sample-and-hold amplifier architecture is based on an integrator which results in a relatively low input impedance (2.5 kΩ) and an acquisition time of 7.5 μs (maximum). DC error sources are specified and controlled through the use of precision amplifiers, low leakage switches and package-level laser trimming of thin-film resistors.

Group delay is specified and controlled through the use of trimmed thin-film resistors, tight-tolerance hold capacitors and high speed amplifiers. Aperture delay is specified and controlled through the use of high speed CMOS logic and DMOS switches. The effective aperture delay, which is the delay seen by the user, is therefore controlled from channel to channel and from device to device. The effective aperture delay is negative because the held value corresponds to a value of input voltage that occurred before the amplifier was put into hold mode.

In applications where endpoint (+FS and −FS) accuracy is critical, the source impedance should be minimized because each ohm will typically change the gain of the sample-and-hold amplifier by 0.04%. This should not be a problem in most cases because the low impedance output of either a programmable gain amplifier or antialiasing filter will be connected to each of the AD1334's analog inputs.

CHANNEL CONTROLLER

The AD1334 Channel Controller enables the AD1334 to appear as four independent channels of analog input by generating all of the timing necessary to ensure that the sampled channel is digitized to 12-bit accuracy. Upon receipt of a sample command, the controller will immediately place the sample-and-hold amplifier into hold mode and then prioritize and schedule the held value for A/D conversion. At the appropriate time, the sampled input is gated through the multiplexer and, after settling, is digitized by the A/D converter. The sample-and-hold amplifier is then returned to sample mode so that it can acquire the next sample.

Operational Description

Timing is initiated on the rising edge of SAMPLE 0–3 control inputs. To minimize the effects of digital feedthrough from the control inputs, it is recommended that the falling edge occur before sample-and-hold acquisition (sample-and-holds have a maximum 7.5 μs acquisition time) but after the A/D conversion is complete. Refer to Figures 15 and 16.

CONTROL $\overline{\text{ENB}}$ functions as an "on/off" switch for the controller and is both an input and an open drain output. The controller can therefore be activated either through the microprocessor interface (via control register Bit 7) or externally by an open drain driver (such as the 74HC03). The controller can also be permanently enabled by grounding CONTROL $\overline{\text{ENB}}$. The timing for enabling and disabling the controller as described above is shown in Figure 14. Controller operation is described in greater detail in the application note "Using Multiple AD1334s in Many-Channel Synchronous Sampling Applications."

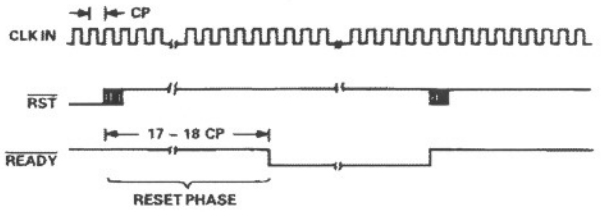


Figure 14a. Timing Diagram for Resetting Controller (CONTROL $\overline{\text{ENB}}$ = 0)

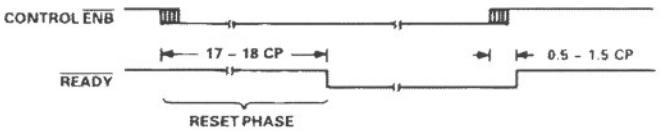


Figure 14b. Timing Diagram for Disabling and Enabling Controller Using CONTROL $\overline{\text{ENB}}$ ($\overline{\text{RST}}$ = 1)

The channel controller also adds 2 bits (D12 and D13) of data to each A/D conversion result for channel identification. Table I summarizes this relationship.

D13	D12	A/D Conversion Results From
0	0	Channel 0
0	1	1
1	0	2
1	1	3

Table I.

Two timing modes are available for sampling and converting each or all of the analog inputs. (Note - The timing diagrams shown refer to Channels "A,B,C,D" rather than "0,1,2,3." This is done because each channel is completely independent of the other three channels and, in fact, Channel A can be any of Channels 0, 1, 2 or 3, Channel B can be any of the remaining channels, etc.)

Simultaneous Mode

Simultaneous mode is selected by connecting the $\overline{\text{SIMULT}}$ pin to logic low. This mode should be used when any 2, 3 or all 4 channels are to be sampled simultaneously (i.e., at the same instant in time). This mode keeps the sample-and-hold amplifiers on the sampled channels in hold mode until all the sampled inputs have been digitized and will normally result in better channel-to-channel isolation relative to independent mode. The timing diagram for this mode is shown in Figure 15. Note that $\overline{\text{IRQ}}$ becomes active on the completion of every A/D conversion since the FIFO is not being used in this example.

Prioritizing logic internal to the channel controller can be used to ensure that the channels are converted in a predetermined sequence. Synchronizing the sample control signal (rising edge of SAMPLE 0-3) to either the rising or falling edge of the clock will result in Channel 0 being converted before Channel 1, Channel 1 before Channel 2, and Channel 2 before Channel 3. An obvious advantage to this is that the user can choose to ignore data Bits 12 and 13 (D12 and D13) which carry the channel identification.

AD1334

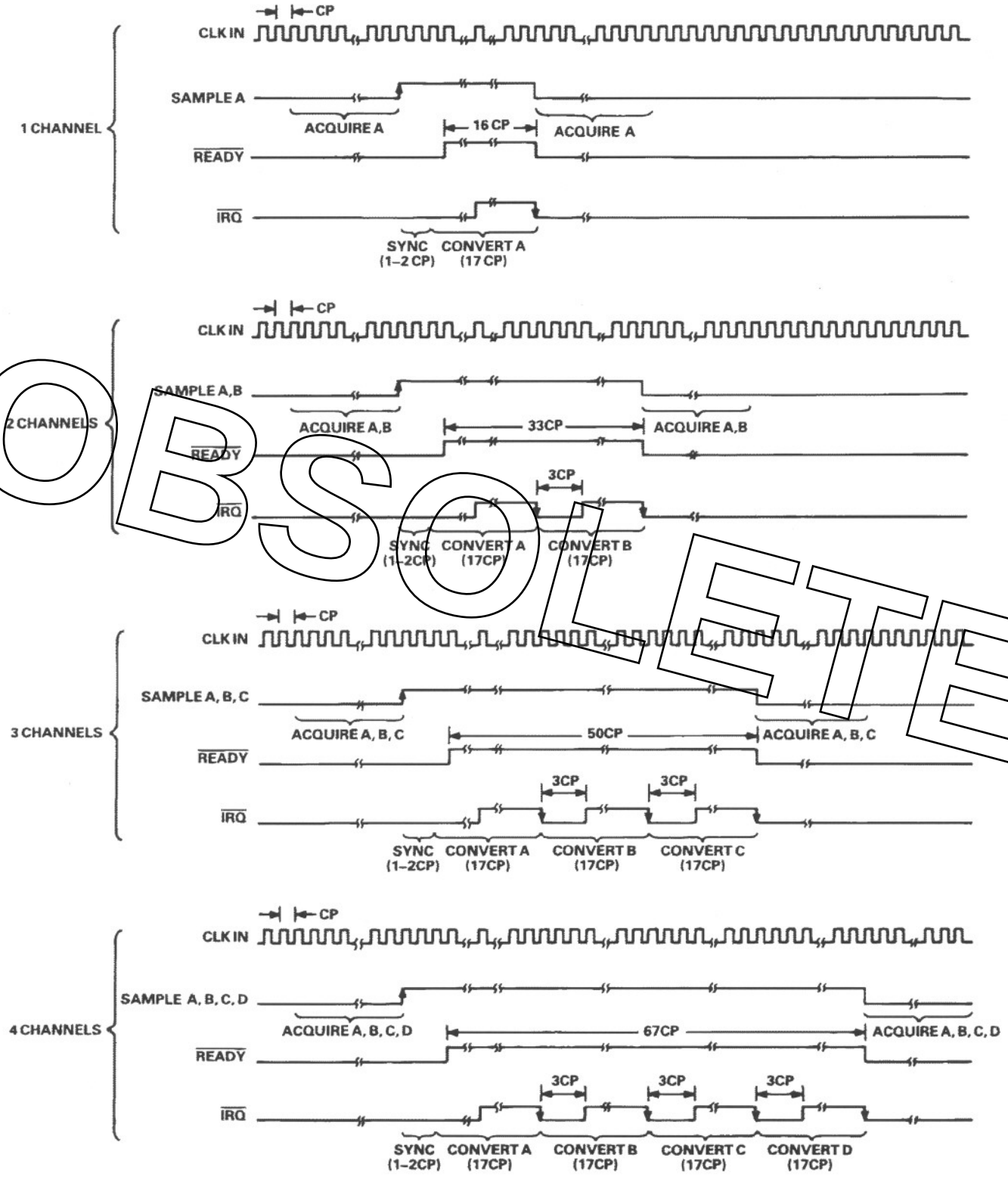


Figure 15. Timing Simultaneous Sampling ($\overline{SIMULT}$ = Low, FIFO Not Used)

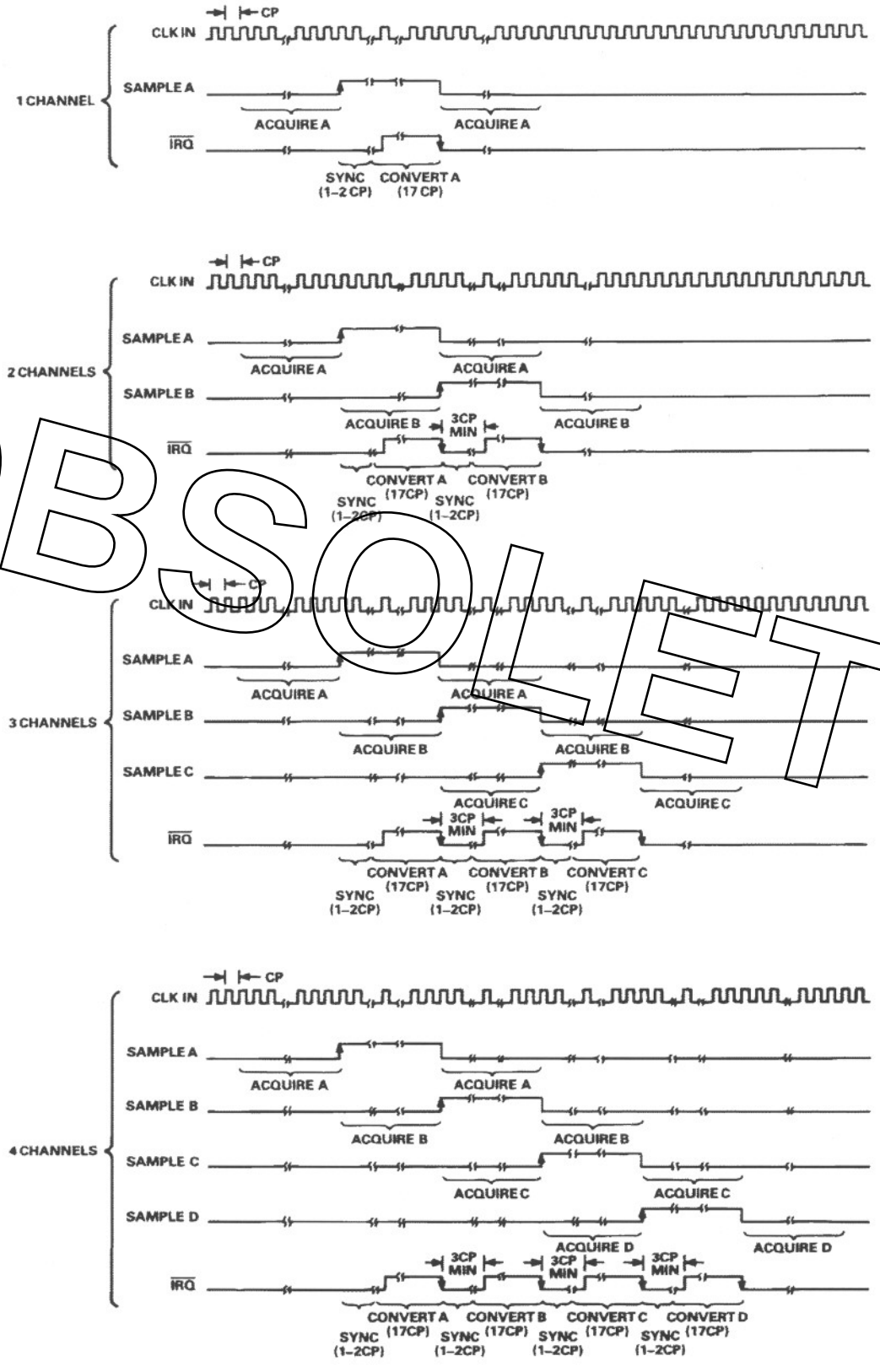


Figure 16. Timing for Independent Sampling ($\overline{SIMULT}$ = High, FIFO Not Used) w/Worst Case Skew of SAMPLE Control Inputs

If the FIFO is used, the falling edge of the $\overline{READY}$ signal, can be used as an interrupt signal to notify a processor that the 1, 2, 3 or 4 channels have been successfully converted and have been shifted into the FIFO. All conversion results can be read from the FIFO with the exception of the last one, which must fall through to the output (fall-through time is typically 400 ns). $\overline{READY}$ can also be used as a signal to the device generating the sample command that the previous group of samples have been converted and that the next group of samples are being acquired.

The application note "Simultaneous and Independent Sampling of Analog Signals with the AD1334" describes this operating mode in greater detail.

Independent Mode

Independent mode is selected by connecting the $\overline{SIMULT}$ pin to logic high. This mode should be used when any number of channels are sampled independently. In contrast to simultaneous mode, this mode returns the sample-and-hold amplifier on the sampled channel to sample mode when the channel input has been digitized. This mode allows the AD1334 to emulate up to four independent sampling A/D converters, each of which can accommodate different sample rates and hence different signal bandwidths. The timing diagram for this mode is shown in Figure 16. Note that $\overline{IRQ}$ becomes active on the completion of every A/D conversion since the FIFO is not being used.

The $\overline{READY}$ signal has no implicit definition in this mode, other than the falling edge indicating that the controller has no conversions pending.

The application note "Simultaneous and Independent Sampling of Analog Signals with the AD1334" describes this operating mode in greater detail.

A/D CONVERTER

The analog input voltage range goes from −5 V to +5 V and the digital output coding is Offset Binary (see Table II). Twos complement coding can be obtained by inverting the MSB (D11).

Center of Code Voltage (V)	Output Code
−5.000000	000 . . . 000
−0.002441	011 . . . 111
0.000000	100 . . . 000
+4.997559	111 . . . 111

Table II. A/D Conversion Relationship

Operational Description

Analog signal information is converted to a 12-bit digital word by sampling the waveform and digitizing it using the successive-approximation conversion technique. Since the clock does not define the amount of time between samples, it need not be crystal controlled. Best performance will be obtained by operating the clock at the maximum 2.5 MHz clock frequency.

HIGH SPEED DIGITAL INTERFACE

The AD1334 completes the solution for A/D conversion in DSP applications by providing the system's designer a direct, high speed parallel digital interface. The prime feature of this interface architecture is that it operates completely asynchronously from the A/D converter and therefore allows the AD1334 to appear as "memory" to a microprocessor.

The combination of fully asynchronous operation with respect to the A/D conversion process and fast data access time allows the AD1334 user to upgrade to faster versions, or even different vendors, of DSP hardware without having to add synchronization or wait state logic. In addition, by virtue of hybrid circuit technology, the user is not required to add external circuitry to prevent digital feedthrough into the analog section.

The AD1334 data transfer is accomplished by employing an interrupt driven architecture. Interrupts can be programmed by the microprocessor to be generated when the FIFO is full (32 conversion results), half-full (16 conversion results) or after every conversion (FIFO is bypassed). The AD1334 digital interface also includes an overrange detect circuit, which can generate an interrupt if the sampled analog input signal exceeds positive or negative full scale, to alert the system that a conversion result has been generated that will result in a nonlinearity in the subsequent signal processing.

Operational Description

The AD1334 can interface directly to a microprocessor via standard data (D0–D13), address (A0) and control lines read ($\overline{RD}$, $\overline{WR}$, $\overline{CS}$, $\overline{IRQ}$ and $\overline{RST}$).

Data Transfer

The data lines D0–D13 are bidirectional I/O that are TTL compatible and have 4mA drive capability. The data lines are used to transfer control information into, and A/D conversion results with status information and channel identification out of the AD1334. Address line A0 is an input that is used to select as the data path either A/D conversion results with channel ID (A0=0) or the Control/Status Registers (A0=1) and would typically be the least significant address bit in the system if the AD1334 is "mapped" to adjacent memory locations. Chip Select ($\overline{CS}$) is used to define a unique location in memory for the AD1334 and should be formed by decoding the upper address bits. Read ($\overline{RD}$) and Write ($\overline{WR}$) define the type of data transfer.

Figures 17–22 illustrate how the AD1334 interfaces to a number of popular single chip digital signal processors.

Interrupts

Interrupt Request ($\overline{IRQ}$) is an open drain output that can be used to interrupt the processor on any of the conditions programmed in the control register. $\overline{READY}$ can be used in simultaneous applications as an alternative processor interrupt signal as described above. In either case, the processor should be programmed to interrupt on the falling edge of its Interrupt Request input.

FIFO

The AD1334 contains a high speed 32-word asynchronous fall-through FIFO which may be enabled under user control when data buffering is required. The FIFO may be programmed to produce interrupts on either the half-full or full condition as well as on certain errors. Its boundary condition behavior is designed to minimize the possibility of lost data. This behavior is described in detail in the application note "FIFO Operation and Boundary Conditions in the AD1332 and AD1334."

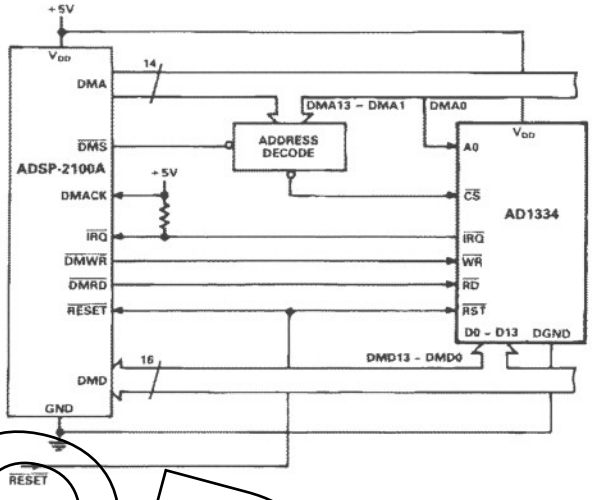


Figure 17. ADSP-2100A to AD1334 Interface

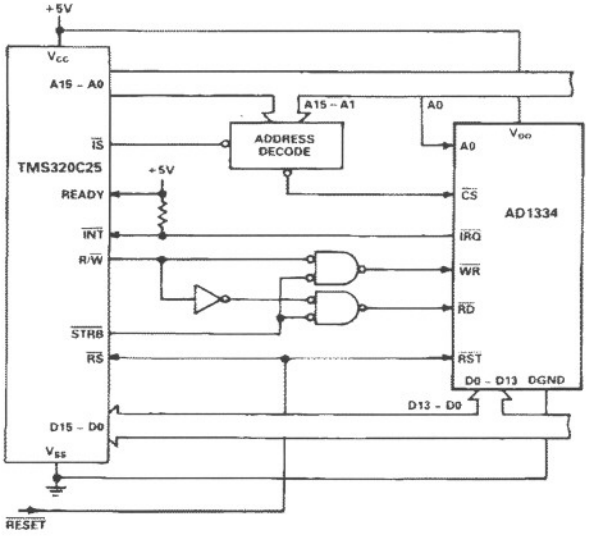


Figure 18. TMS320C25 to AD1334 Interface

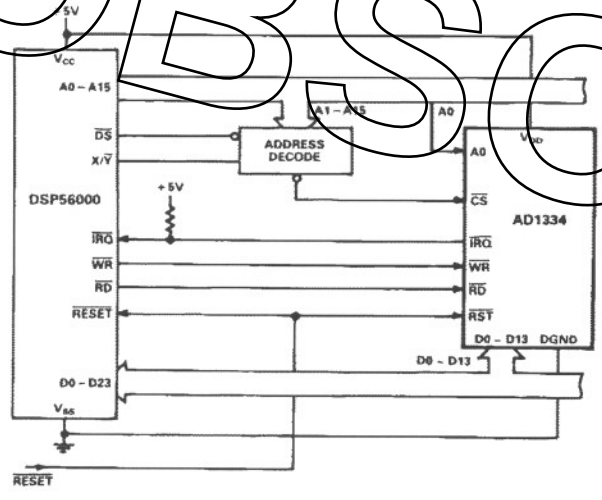


Figure 19. DSP56000 to AD1334 Interface

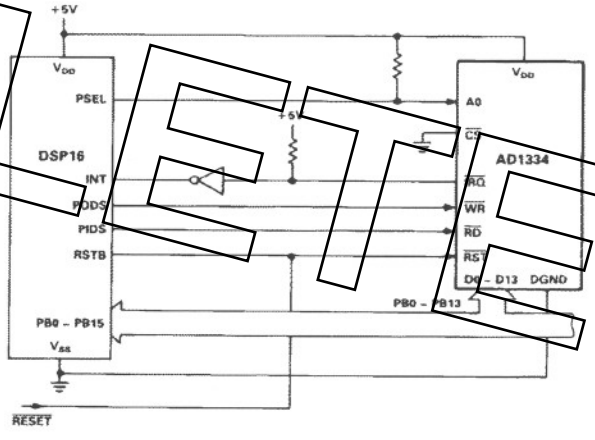


Figure 20. DSP16 to AD1334 Interface

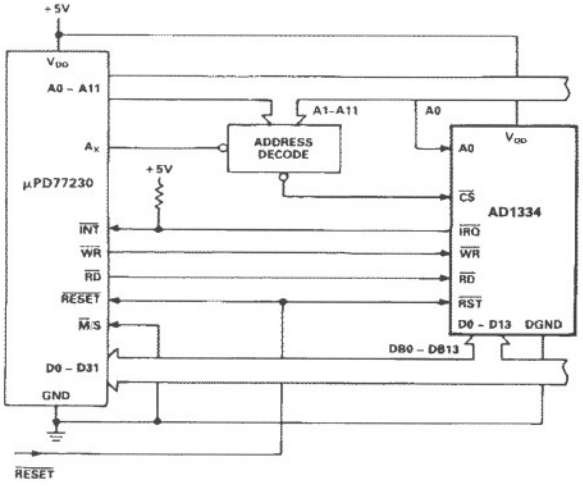


Figure 21. μPD77230 to AD1334 Interface

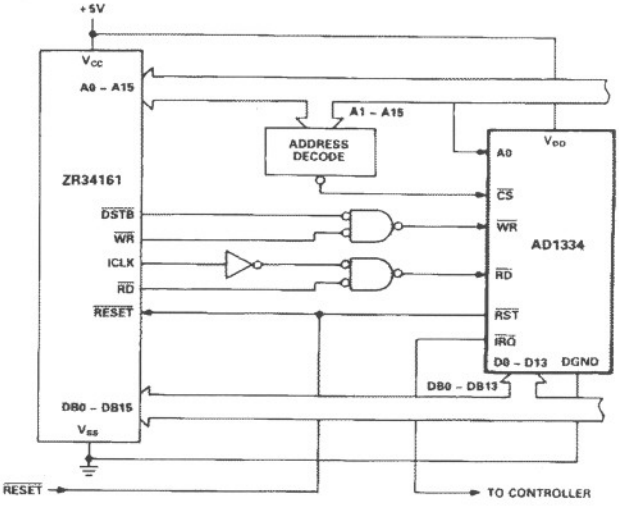


Figure 22. ZR34161 to AD1334 Interface

AD1334

FIFO Half-Full Interrupt

The timing for interrupts that are generated when the FIFO is half-full is shown in Figures 23a and 23b. In both figures, $\overline{IRQ}$ becomes active when the 16th A/D conversion result is shifted into the FIFO. In Figure 23a, the processor responds immediately and a read cycle takes place before the next conversion cycle begins. Here, the completion of the read cycle shifts the 1st conversion result (which was just read by the processor) out of the FIFO, replaces it with the second conversion result and causes $\overline{IRQ}$ to become inactive since there are now 15 conversion results in the FIFO.

In Figure 23b, the processor does not respond before the next conversion cycle begins and $\overline{IRQ}$ becomes inactive. The FIFO continues to accept conversion results and the processor can read from the FIFO at any time so long as the FIFO has not overrun.

This mode allows the AD1334 to have a low interrupting priority since the processor has up to 17 additional A/D conversions before the FIFO overruns. Therefore, the processor will have up to 260µs to respond at the maximum sample rate of 65kHz.

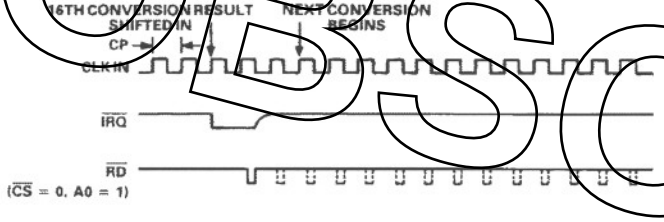


Figure 23a. Timing Diagram for Half-Full Interrupt (Read Before 17th Conversion Started)

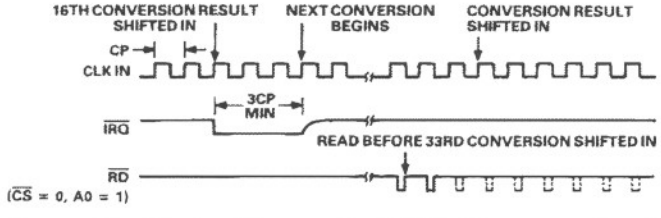


Figure 23b. Timing Diagram for Half-Full Interrupt (Read After 17th Conversion Started)

FIFO Full Interrupt

The timing for interrupts that are generated when the FIFO is full is shown in Figures 24a and 24b. In both figures, $\overline{IRQ}$ becomes active when the 32nd A/D conversion result is shifted into the FIFO. In Figure 24a, the processor responds immediately and a read cycle takes place before the next conversion cycle begins. Here, the completion of the read cycle shifts the first conversion result (which was just read by the processor) out of the FIFO, replaces it with the second conversion result and causes $\overline{IRQ}$ to become inactive because there are now 31 conversion results in the FIFO.

In Figure 24b, the processor does not respond before the next conversion cycle begins and $\overline{IRQ}$ becomes inactive. The processor must read from the FIFO before the completion of the current conversion cycle or the FIFO will overrun. This mode maximizes the memory capability of the AD1334 but requires a fairly high interrupting priority in the processor since the processor has only one A/D conversion before the FIFO overruns. Therefore, the processor will have only 15µs to respond at the maximum sample rate of 65kHz.

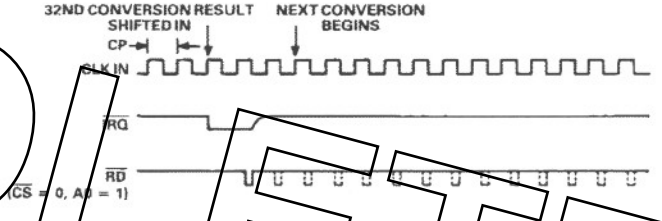


Figure 24a. Timing Diagram for Full Interrupt (Read Before 33rd Conversion Started)

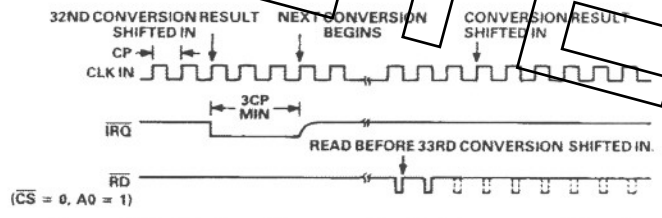


Figure 24b.Timing Diagram for Full Interrupt (Read After 33rd Conversion Started)

Conversion Results Overrange Interrupt

If the FIFO is used, the AD1334 can be programmed to generate interrupts when overranged conversion results are shifted into the FIFO. If $\overline{IRQ}$ became active as a result of an overrange condition, the only way it can become inactive is to clear Bit 4 of the control register. Typically, the user should clear the entire control register which will, in effect, remove the interrupt, reset the FIFO and disable the controller.

Should the overrange interrupt capability be used, Status Register Bits 4 and 6 can be used to identify whether the interrupt occurred as a result of an overrange condition or FIFO half-full (or full).

Single Conversion Interrupt (FIFO Bypassed)

The timing for interrupts that are generated when the FIFO is bypassed is shown in Figures 15 and 16. Here, $\overline{IRQ}$ becomes active at the completion of each A/D conversion cycle. $\overline{IRQ}$ remains active, independent of the read cycle, until the next conversion cycle begins, which is a minimum of three clock periods (1.2µs with 2.5MHz clock). Data is valid so long as $\overline{IRQ}$ remains active.

This mode makes data available immediately after the conversion process has been completed and is therefore very similar to the operation of a conventional A/D converter if $\overline{IRQ}$ is taken to mean conversion STATUS. This mode is most useful when a single conversion result is necessary to adjust a system parameter, such as the gain of a PGA that may be in front of an AD1334.

Since $\overline{IRQ}$ will only be valid for only three A/D clock periods (1.2µs with a 2.5MHz clock), a high interrupting priority should be assigned by the processor. Should the single conversion result be necessary to adjust a system parameter as described above, it may be more efficient to "poll" the Status Register to determine when the conversion result is available.

Operation Other Than with a Microprocessor

The AD1334 can be used in other than microprocessor environments by grounding pins 11, 12 and 29 ($\overline{CS}$, A0 and $\overline{RD}$), connecting Pin 30 ($\overline{WR}$) to V_{DD} and pulsing $\overline{RST}$ low. This will permanently enable the AD1334 three-state outputs and clear the control register, causing the FIFO to be bypassed.

Multiple AD1334s

The architecture of the AD1334 allows multiple devices to be used in a microprocessor based system. Figure 25 illustrates how four AD1334s can be configured to simultaneously sample their analog inputs and reside in eight sequential locations in a microprocessor's memory address space. The control register of each device should be programmed to interrupt on the same condition so that the same number of conversion results are available from all devices. Further information on controlling and synchronizing multiple devices is contained in the application note "Using Multiple AD1334s in Many-Channel Simultaneous Sampling Applications."

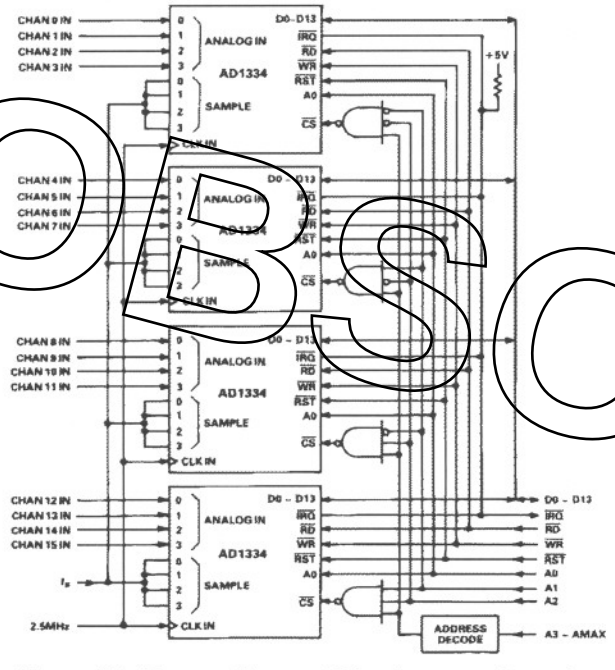


Figure 25. Sixteen-Channel Simultaneous Sampling System

Floating Point Converter

Figure 26 illustrates how to boost the dynamic range of the AD1334 by including it in a floating point A/D converter architecture. The AD526 is a single-ended programmable gain amplifier with gains of 1, 2, 4, 8 and 16. Here, four AD526s are "hardwired" into gains of 1, 2, 4 and 8 to extend the dynamic range of the AD1334 to 15 bits. Fully differential inputs with gains up to 500 can be obtained by substituting the AD365 for the AD526.

The AD1334 is operated in simultaneous mode, with one AD526 per channel. Upon receipt of a sample command, the four channels are sampled and converted. Table III summarizes the input voltage range for each channel.

Channel	Input Voltage Range
0	−5 V to +5 V
1	−2.5 V to +2.5 V
2	−1.25 V to +1.25 V
3	−625 mV to +625 mV

Table III.

For each group of four samples, a processor can be used to discard the three A/D conversion results that were not converted on the optimum range. The system shown can provide results at sample rates up to 28 kHz.

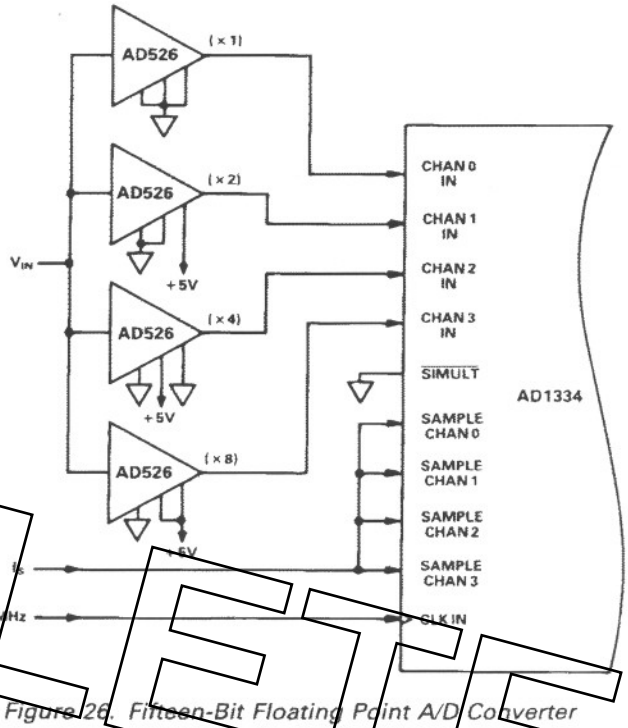


Figure 26. Fifteen-Bit Floating Point A/D Converter

SUCCESSFULLY APPLYING THE AD1334

Grounding

In order to obtain the specified performance of the AD1334, proper grounding and power supply decoupling techniques must be observed. First, it is imperative that a ground plane be used. A ground plane provides a low resistance, low inductance path for currents to flow back to their source. Without a ground plane, currents will return to the source in such a way as to minimize the energy of the system and therefore parasitic inductances will exist in such undesirable locations as power supply lines and signal grounds.

Second, all three ground connections on the AD1334 must be tied together to the ground plane. The AD1334 APWR GND (Pin 9) carries the imbalance current from the analog power supplies ($\pm V_S$). APWR GND is also connected to the package seal ring/lid and therefore can cause coupling between the analog and digital sections if it is not tied directly to the ground plane.

ASIG GND (Pin 8) is the signal ground internal to the AD1334 and is "common" for the −5 V reference, sample-and-hold amplifiers, multiplexer and A/D converter. The current that flows through this pin from the A/D converter is a dynamic current that changes on every clock cycle. Inductance in this trace will therefore cause a reduction in performance in the entire analog section.

DGND (Pin 20) is a separate ground connection for the digital interface chip. It carries a dynamic current every time a digital output changes state, and inductance in the trace that connects to this pin will reduce the noise margin between the A/D converter and the digital interface chip.

Power Supply Decoupling

The power supply decoupling capacitors supply the instantaneous current to the AD1334 and also provide some high frequency filtering. The filtering aspect of the capacitors should not be counted on however, and the user should make every effort to supply quiet, well regulated power supplies to the AD1334. Switching mode power supplies are not recommended for the analog power supplies $\pm V_S$.

Decoupling capacitors should be placed as close to the device as possible to minimize inductances in power supply traces. A 2.2μF (or greater) solid tantalum capacitor in parallel with a 0.1μF ceramic capacitor should be used for decoupling each $+V_S$ and $-V_S$. A 1.0μF (or greater) solid tantalum capacitor should be used for decoupling V_{DD}.

Transmission Line Effects

The digital interface has 10K ECL speed and with 15pF loading exhibits a typical edge rate of 1.4ns. High speed CMOS systems that incorporate the AD1334 must use careful PCB layout and impedance matching techniques to reduce crosstalk and voltage reflections.

Crosstalk

The fast edge rates with large voltage swings of CMOS systems can result in capacitive and inductive coupling (crosstalk) between adjacent PCB signal traces and may compromise signal integrity and reduce noise margins. The effect can be most severe on data lines that are near "clocked" control lines, such as Read, Write and Chip Select lines, when they actually change their logic state as a result of crosstalk.

To reduce crosstalk, the PCB layout should minimize long parallel traces. If this can not be avoided, clock lines should be shielded from data and address lines by running ground traces along side them.

Voltage Reflections

The gross impedance mismatch between high impedance CMOS inputs and low impedance CMOS outputs invites unwanted voltage reflections and "ringing" that can also compromise signal integrity and reduce noise margins. This level of mismatch causes a nearly equal and opposite negative pulse to be reflected back from the load to the source when the round trip delay of the line exceeds the rise or fall time of the driving signal. For a typical line delay of 0.055ns/cm with a 1.4ns edge rate, this translates to only 13cm (5 inches) for the AD1334. Provided the signal lines are over a ground plane, this may never be a problem since the added capacitance will reduce the edge rate.

The effect will be most severe on "clock" lines in synchronous systems such as Read, Write and Chip Select lines. For example, should the AD1334 Read control input ($\overline{RD}$) be double clocked as a result of a reflection while in a read cycle, in most cases the digital interface chip will be fast enough to respond. If the FIFO is being read from, a second shift out will occur and A/D conversion results will be lost.

Since CMOS output stages are not capable of delivering enough current to the load when a transmission line (PCB trace) is terminated in its characteristic impedance, series damping is recommended when reflections must be reduced or eliminated. Here, a small resistor (typically 10Ω to 75Ω) is inserted in series with the transmission line as close to the source as possible. The goal is to match the series resistance plus driver output impedance to the transmission line impedance. This will keep the wave that is reflected back from the load to source from reflecting back to the load.

The primary disadvantage of series termination is that due to the voltage divider formed by the source resistance and line impedance, the voltage at the input to the line is midway between logic levels during the two-way propagation delay time. This means that although any number of device inputs may be attached at the load end, other device inputs cannot be distributed along the transmission line.

REFERENCES

Cypress Semiconductor, CMOS Data Book, Cypress Semiconductor, 1987.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm)

40-Pin Bottom Brazed Ceramic DIP (DH-40A)