

8 Bit Monolithic Multiplying D/A Converter

FEATURES

Improved Replacement for Industry Standard 1408/1508

Improved Settling Time: 250ns typ

Improved Linearity: ±0.1% Accuracy Guaranteed Over

Temperature Range (-9 Grade)

High Output Voltage Compliance: +0.5V to -5.0V

Low Power Consumption: 157mW typ

High Speed 2-Quadrant Multiplying Input: 4.0mA/µs

Slew Rate

Single Chip Monolithic Construction

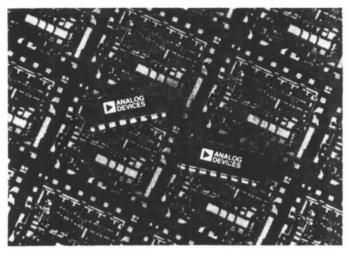
Hermetic 16 Pin Ceramic DIP

Low Cost

The AD1408 and AD1508 are low cost monolithic integrated circuit 8-bit multiplying digital-to-inglog converters, consisting of matched bipolar switches, a precision resistor network and a control amplifier. The single chip is mounted in a hermetically sealed ceramic 16 lead dual-in-line package.

Advanced circuit design and precision processing techniques result in significant performance advantages over older indusrry standard 1408/1508 devices. The maximum linearity error over the specified operating temperature range is guaranteed to be less than ±4LSB (-9 grade) while settling time to ±4LSB is reduced to 250ns typ. The temperature coefficient of gain is typically 20ppm/°C and monotonicity is guaranteed over the entire operating temperature range.

The AD1408/AD1508 is recommended for all low-cost 8-bit DAC requirements; it is also suitable for upgrading overall performance where older, less accurate and slower 1408/1508 devices have been designed in. The AD1408 series is specified for operation over the 0 to +75°C temperature range, the AD1508 series for operation over the entire military temperature range of -55°C to +125°C.



- Monolithic IC construction makes the AD1408/AD1508 an optimum choice for applications where low cost is a major consideration.
- he AD1408/AD1508 directly replaces other devices of
- rsatile design configuration allows voltage or current outputs, variable or fixed reference inputs CMOS or TTL logic compatibility and a wide choice of accuracy and ten perature range specifications.
- 4. Accuracies within ±1/4LSB allow performance improvement of older applications without redesign.
- 5. Faster settling time (250ns typ) permits use in higher speed applications.
- 6. Low power consumption improves stability and reduces warm-up time.
- 7. The AD1408/AD1508 multiplies in two quadrants when a varying reference voltage is applied. When multiplication is not required, a fixed reference is used.
- 8. The AD1408/AD1508 is available in chip form; please consult factory for details.
- 9. The device is packaged in a hermetically-sealed ceramic 16 lead dual-in-line package. Processing to MIL-STD-883 level B is available.

RATING	SYMBOL	V	LUE		UNIT
POWER SUPPLY VOLTAGE	v _{cc}	+5	.5 6.5		V dc V dc
DICITAL DIDITION TACE	V _{EE}		.5. 0		V dc
DIGITAL INPUT VOLTAGE	V ₅ thru V ₁₂				
APPLIED OUTPUT VOLTAGE	v_0		.5, -5.2		V dc
REFERENCE CURRENT	I ₁₄	5.0			mA
REFERENCE AMPLIFIER INPUTS	V_{14}, V_{15}	v _c	C, V _{EE}		V dc
POWER DISSIPATION (Package Limitation) Derate above T _A = +25°C	D	10	00		mW mW/°C
OPERATING TEMPERATURE RANGE	P _D	0.			mw/ C
AD1408 Series	T_A	0 1	0 +75		°C
AD1508 Series	TA		5 to +125	5	°C
STORAGE TEMPERATURE RANGE	T _{STG}	-6	5 to +150)	°c
ADI408 Series: The = 0 to +75°C unless others CHARACZERISTIC	.0mA, AD1508 Series	s: T _A = -55° inputs at hig	C to +12 h logic le	e5°C vel.)	UNIT
(Error Relative to Full Scale I ₂) AD1508-9, AD1408-9 AD1508-8, AD1408-8 AD1408-7 SETTLING TIME) <u>-</u> /	±0.10 ±0.19 ±0.39	% %
to Within 1/2LSB [Includes t _{PLH}] $(T_A = +25^{\circ}C)$	t _S	<u> </u>	250		ns
PROPAGATION DELAY TIME				\mathcal{I}	
$T_A = +25^{\circ}C$	фLH, фHL	-	30	100	ns
OUTPUT FULL SCALE CURRENT DRIFT	TCIO	-	-20	_	ppm/°C
DIGITAL INPUT LOGIC LEVELS (MSB)					9,4400
High Level, Logic "1" Low Level, Logic "0"	v_{IH}	2.0	_	0.8	V dc V dc
DIGITAL INPUT CURRENT (MSB)					
High Level, V _{IN} = 5.0V	I _{IH}	-	0	0.04	mA
Low Level, $V_{IL} = 0.8V$	I _{IL}	-	-0.4	-0.8	mA
REFERENCE INPUT BIAS CURRENT (Pin 15)	I ₁₅	-	-1.0	-3.0	μΑ
OUTPUT CURRENT RANGE					
		0	2.0	2.1	mA
$V_{EE} = -5.0V$	OR				
$V_{EE} = -6.0V \text{ to } -15V$	I _{OR} I _{OR}	o	2.0	4.2	mA
V _{EE} = -6.0V to -15V OUTPUT CURRENT	L _{OR}	0	2.0	4.2	mA
$V_{\text{EE}} = -6.0 \text{V to } -15 \text{V}$ OUTPUT CURRENT $V_{\text{REF}} = 2.000 \text{V}, \text{R14} = 1000 \Omega$	or lor				
$V_{\rm EE}^{}=$ -6.0V to -15V OUTPUT CURRENT $V_{\rm REF}^{}=$ 2.000V, R14 = 1000 Ω OUTPUT CURRENT (All Bits Low)	L _{OR}	0	2.0	4.2	mA
$V_{\rm EE}^{}=$ -6.0V to -15V OUTPUT CURRENT $V_{\rm REF}^{}=$ 2.000V, R14 = 1000 Ω OUTPUT CURRENT (All Bits Low) OUTPUT VOLTAGE COMPLIANCE	I _O	1.9	1.99	2.1	mA mA
$V_{\rm EE}^{\rm r}$ = -6.0V to -15V OUTPUT CURRENT $V_{\rm REF}$ = 2.000V, R14 = 1000Ω OUTPUT CURRENT (All Bits Low) OUTPUT VOLTAGE COMPLIANCE (E ₁ \leq 0.19% at T _A = +25°C)	I _O (min)	1.9	1.99	4.2	mA mA μA
$V_{\rm EE} = -6.0 \text{V to } -15 \text{V}$ $OUTPUT CURRENT$ $V_{\rm REF} = 2.000 \text{V, } R14 = 1000 \Omega$ $OUTPUT CURRENT$ (All Bits Low) $OUTPUT \text{ VOLTAGE COMPLIANCE}$ $(E_1 \le 0.19\% \text{ at } T_A = +25 ^{\circ} \text{C})$ $V_{\rm EE} = -5 \text{V}$	I _O I _O (min) V _O	1.9	1.99	4.2 2.1 4.0 -0.6, +0.5	mA mA μA
$V_{\rm EE} = -6.0 \text{V to } -15 \text{V}$ OUTPUT CURRENT $V_{\rm REF} = 2.000 \text{V}, \text{R14} = 1000 \Omega$ OUTPUT CURRENT (All Bits Low) OUTPUT VOLTAGE COMPLIANCE $\{E_1 \le 0.19\% \text{ at } T_A = +25^{\circ}\text{C}\}$ $V_{\rm EE} = -5 \text{V}$ $V_{\rm EE} \text{ below } -10 \text{V}$	I _O I _O (min) V _O V _O	1.9	2.0 1.99 0	4.2 2.1 4.0 -0.6, +0.5 -5.0, +0.5	mA mA μA V dc V dc
$V_{EE} = -6.0V \text{ to } -15V$ $OUTPUT CURRENT$ $V_{REF} = 2.000V, R14 = 1000\Omega$ $OUTPUT CURRENT$ $(All Bits Low)$ $OUTPUT VOLTAGE COMPLIANCE$ $(E_1 \le 0.19\% \text{ at } T_A = +25^{\circ}\text{C})$ $V_{EE} = -5V$ $V_{EE} \text{ below } -10V$ $REFERENCE CURRENT SLEW RATE$	I _O I _O (min) V _O	1.9	1.99	4.2 2.1 4.0 -0.6, +0.5	mA mA μA
$\begin{split} &V_{EE}^- = -6.0 \text{V to } -15 \text{V} \\ &\text{OUTPUT CURRENT} \\ &V_{REF}^- = 2.000 \text{V}, \text{R14} = 1000 \Omega \\ &\text{OUTPUT CURRENT} \\ &\text{(All Bits Low)} \\ &\text{OUTPUT VOLTAGE COMPLIANCE} \\ &\text{(E}_1 \leq 0.19\% \text{ at } T_A = +25 ^\circ \text{C}) \\ &V_{EE}^- = -5 \text{V} \\ &V_{EE}^- \text{ below } -10 \text{V} \\ &\text{REFERENCE CURRENT SLEW RATE} \\ &\text{OUTPUT CURRENT POWER SUPPLY SENSITIVITY} \end{split}$	I _O I _O (min) V _O V _O	1.9	2.0 1.99 0	4.2 2.1 4.0 -0.6, +0.5 -5.0, +0.5	mA mA μA V dc V dc
$V_{EE}^{-} = -6.0V \text{ to } -15V$ $OUTPUT CURRENT$ $V_{REF} = 2.000V, R14 = 1000\Omega$ $OUTPUT CURRENT$ $(All Bits Low)$ $OUTPUT VOLTAGE COMPLIANCE$ $\{E_1 \le 0.19\% \text{ at } T_A = +25^{\circ}\text{C}\}$ $V_{EE} = -5V$ $V_{EE} \text{ below } -10V$ $REFERENCE CURRENT SLEW RATE$ $OUTPUT CURRENT POWER SUPPLY$ $SENSITIVITY$ $POWER SUPPLY CURRENT$	l _O R l _O (min) V _O V _O SRI _{REF} PSSI _O	0 1.9 - - -	2.0 1.99 0 - - 4.0	4.2 2.1 4.0 -0.6, +0.5 -5.0, +0.5 - 2.7	mA mA V dc V dc mA/μs μA/V
$\begin{split} &V_{EE}^- = -6.0 \text{V to } -15 \text{V} \\ &\text{OUTPUT CURRENT} \\ &V_{REF}^- = 2.000 \text{V}, \text{R14} = 1000 \Omega \\ &\text{OUTPUT CURRENT} \\ &\text{(All Bits Low)} \\ &\text{OUTPUT VOLTAGE COMPLIANCE} \\ &\text{(E}_1 \leq 0.19\% \text{ at } T_A = +25 ^\circ \text{C}) \\ &V_{EE}^- = -5 \text{V} \\ &V_{EE}^- \text{ below } -10 \text{V} \\ &\text{REFERENCE CURRENT SLEW RATE} \\ &\text{OUTPUT CURRENT POWER SUPPLY SENSITIVITY} \end{split}$	l _O R l _O (min) V _O V _O SRI _{REF} PSSI _O l _{CC}	0 1.9 - - -	2.0 1.99 0 	4.2 2.1 4.0 -0.6, +0.5 -5.0, +0.5 - 2.7	mA mA μA V dc V dc mA/μs
$V_{EE} = -6.0V \text{ to } -15V$ $OUTPUT CURRENT$ $V_{REF} = 2.000V, R14 = 1000\Omega$ $OUTPUT CURRENT$ $(All Bits Low)$ $OUTPUT VOLTAGE COMPLIANCE$ $\{E_1 \le 0.19\% \text{ at } T_A = +25^{\circ}\text{C}\}$ $V_{EE} = -5V$ $V_{EE} \text{ below } -10V$ $REFERENCE CURRENT SLEW RATE$ $OUTPUT CURRENT POWER SUPPLY$ $SENSITIVITY$ $POWER SUPPLY CURRENT$ $(All Bits Low)$	l _O R l _O (min) V _O V _O SRI _{REF} PSSI _O	0 1.9 - - -	2.0 1.99 0 - - 4.0	4.2 2.1 4.0 -0.6, +0.5 -5.0, +0.5 - 2.7	mA mA V dc V dc mA/μs μA/V mA
$V_{EE} = -6.0V \text{ to } -15V$ OUTPUT CURRENT $V_{REF} = 2.000V, R14 = 1000\Omega$ OUTPUT CURRENT (All Bits Low) OUTPUT VOLTAGE COMPLIANCE $\{E_1 \le 0.19\% \text{ at } T_A = +25^{\circ}\text{C}\}$ $V_{EE} = -5V$ $V_{EE} \text{ below } -10V$ REFERENCE CURRENT SLEW RATE OUTPUT CURRENT POWER SUPPLY SENSITIVITY POWER SUPPLY CURRENT (All Bits Low) POWER SUPPLY VOLTAGE RANGE	l _O R l _O (min) V _O V _O SRI _{REF} PSSI _O l _{CC} l _{EE}	0 1.9 - - - - -	2.0 1.99 0 	4.2 2.1 4.0 -0.6, +0.5 -5.0, +0.5 - 2.7 +14 -13	mA mA V dc V dc V dc mA/μs μA/V mA mA
$V_{EE} = -6.0V \text{ to } -15V$ $OUTPUT CURRENT$ $V_{REF} = 2.000V, R14 = 1000\Omega$ $OUTPUT CURRENT$ $(All Bits Low)$ $OUTPUT VOLTAGE COMPLIANCE$ $\{E_1 \le 0.19\% \text{ at } T_A = +25^{\circ}\text{C}\}$ $V_{EE} = -5V$ $V_{EE} \text{ below } -10V$ $REFERENCE CURRENT SLEW RATE$ $OUTPUT CURRENT POWER SUPPLY$ $SENSITIVITY$ $POWER SUPPLY CURRENT$ $(All Bits Low)$	loR lo (min) Vo Vo SRIREF PSSIO LCC LEE	0 1.9 - - -	2.0 1.99 0 	4.2 2.1 4.0 -0.6, +0.5 -5.0, +0.5 - 2.7	mA mA V dc V dc mA/μs μA/V mA
$V_{\rm EE} = -6.0 { m V}$ to $-15 { m V}$ OUTPUT CURRENT $V_{\rm REF} = 2.000 { m V}$, $R14 = 1000 { m \Omega}$ OUTPUT CURRENT (All Bits Low) OUTPUT VOLTAGE COMPLIANCE $\{E_1 \le 0.19\% \text{ at } T_A = +25 { m °C}\}$ $V_{\rm EE} = -5 { m V}$ $V_{\rm EE}$ below $-10 { m V}$ REFERENCE CURRENT SLEW RATE OUTPUT CURRENT POWER SUPPLY SENSITIVITY POWER SUPPLY CURRENT (All Bits Low) POWER SUPPLY VOLTAGE RANGE $(T_A = +25 { m °C})$	l _O R l _O (min) V _O V _O SRI _{REF} PSSI _O l _{CC} l _{EE}	0 1.9 - - - - - - +4.5	2.0 1.99 0 	4.2 2.1 4.0 -0.6, +0.5 -5.0, +0.5 - 2.7 +14 -13 +5.5	mA mA μA V dc V dc V dc mA/μs μA/V mA mA V dc
$V_{\rm EE} = -6.0 {\rm V} \; {\rm to} \; -15 {\rm V}$ OUTPUT CURRENT $V_{\rm REF} = 2.000 {\rm V}, \; {\rm R}14 = 1000 {\rm \Omega}$ OUTPUT CURRENT (All Bits Low) OUTPUT VOLTAGE COMPLIANCE $\{E_1 \le 0.19\% \; {\rm at} \; T_A = +25 {\rm ^{\circ}C}\}$ $V_{\rm EE} = -5 {\rm V}$ $V_{\rm EE} \; {\rm below} \; -10 {\rm V}$ REFERENCE CURRENT SLEW RATE OUTPUT CURRENT POWER SUPPLY SENSITIVITY POWER SUPPLY CURRENT (All Bits Low) POWER SUPPLY VOLTAGE RANGE $(T_A = +25 {\rm ^{\circ}C})$ POWER DISSIPATION All Bits Low $V_{\rm EE} = -5.0 {\rm V} \; {\rm dc}$	loR lo (min) Vo Vo SRIREF PSSIO LCC LEE	0 1.9 - - - - - - +4.5	2.0 1.99 0 	4.2 2.1 4.0 -0.6, +0.5 -5.0, +0.5 - 2.7 +14 -13 +5.5	mA mA μA V dc V dc V dc mA/μs μA/V mA mA V dc
$V_{EE} = -6.0V \text{ to } -15V$ OUTPUT CURRENT $V_{REF} = 2.000V, R14 = 1000\Omega$ OUTPUT CURRENT (All Bits Low) OUTPUT VOLTAGE COMPLIANCE $(E_1 \le 0.19\% \text{ at } T_A = +25^{\circ}\text{C})$ $V_{EE} = -5V$ $V_{EE} \text{ below } -10V$ REFERENCE CURRENT SLEW RATE OUTPUT CURRENT POWER SUPPLY SENSITIVITY POWER SUPPLY CURRENT (All Bits Low) POWER SUPPLY VOLTAGE RANGE $(T_A = +25^{\circ}\text{C})$ POWER DISSIPATION All Bits Low $V_{EE} = -5.0V \text{ dc}$ $V_{EE} = -15V \text{ dc}$	LOR LO LO (min) VO VO SRI _{REF} PSSLO LCC LCC LEE VCCR VEER	0 1.9 - - - - - - +4.5	2.0 1.99 0 - - 4.0 0.5 +9 -7.5 +5.0 -15	4.2 2.1 4.0 -0.6, +0.5 -5.0, +0.5 - 2.7 +14 -13 +5.5 -16.5	mA mA V dc V dc mA/μs μA/V mA V dc V dc v dc
$V_{\rm EE} = -6.0 \rm{V} \ to \ -15 \rm{V}$ OUTPUT CURRENT $V_{\rm REF} = 2.000 \rm{V}, \ R14 = 1000 \Omega$ OUTPUT CURRENT (All Bits Low) OUTPUT VOLTAGE COMPLIANCE $\{E_1 \le 0.19\% \ \text{at } T_A = +25 ^{\circ} \text{C}\}$ $V_{\rm EE} = -5 \rm{V}$ $V_{\rm EE} \ below \ -10 \rm{V}$ REFERENCE CURRENT SLEW RATE OUTPUT CURRENT POWER SUPPLY SENSITIVITY POWER SUPPLY CURRENT (All Bits Low) POWER SUPPLY VOLTAGE RANGE $(T_A = +25 ^{\circ} \rm{C})$ POWER DISSIPATION All Bits Low $V_{\rm EE} = -5.0 \rm{V} \ dc$	VO VO SRIREF PSSIO LCC IVEE VCCR VEER	0 1.9 - - - - - - +4.5	2.0 1.99 0 - 4.0 0.5 +9 -7.5 +5.0 -15	4.2 2.1 4.0 -0.6, +0.5 -5.0, +0.5 - 2.7 +14 -13 +5.5 -16.5	mA mA V dc V dc V dc mA/μs μA/V mA v dc V dc mA/ψs

Specifications subject to change without notice.

APLYING THE AD1408/1508 Apply Inc. Amplifier Drive and Compensation reference 2a and 2b are the connection diagrams for using the foures 2a and 2b are the connection diagrams for using the feures 2a and 1508 in basic voltage output modes. In Figure 2a, a place of the property of the AD1408/February 22, 20 Stage output modes. In Figure 2a, 2 positive reference voltage, V_{REF}, is converted to a current by R14. This reference current determines. REF, is converted to a current R14. This reference current determines the scale restor for the output current such that the full scale output iscor (1/256) less than the reference psctof roll scale output (1/256) less than the reference current. R15 provides s ILSB (1/256) less than the reference current. R15 provides s llab current compensation to the reference control amplifier ominimize temperature drift; it is nominally equal to R14 to multiple of the a stable precision resistor. This conithough develops a negative output voltage across R_L and requires a positive VREF.

162 negative V_{REF} is to be used, connections to the reference amplifier must be reversed as shown in Figure 2b. This circuit also delivers a negative output voltage, but presents impedance o the reference source. The negative VREF must be at least 4 volts above the VAE supply

quadrant multiplication may b performed by applying sipolar ac signal as the reference as long as pin 14 is positive relative to pin 15 (reference current must flow into pin 14). I the ac reference is applied to pin 14 through R14, a negative voltage equal to the negative peak of the c reference must be applied through R15 to pin 15; if the ac reference is applied to pin 15 through R15, a positive voltage equal to the positive peak of the ac reference must be applied through R14 to pin 14.

when a dc reference is used, capacitive bypass from reference to ground will improve noise rejection.

The compensation capacitor, C, provides proper phase margin for the reference control amplifier. As R14 is increased, the closed-loop gain of the amplifier is decreased, therefore C must be increased. For R14 = $1.0k\Omega$, $2.5k\Omega$ and $5.0k\Omega$, minimum values of capacitance are 15pF, 37pF and 75pF respectively. C may be tied to either VEE or ground, but tying it to VEE increases negative supply noise rejection. If the reference is driven by a high-impedance current source, heavy compensation of the amplifier is required; this causes a reduction in overall bandwidth.

Output Current Range

The nominal value for output current range is 0 to 1.992mA as determined by a 2mA reference current. If VEE is more negative than -7.0 volts, this range may be increased to a maximum of 0 to 4.2mA. An increase in speed may be realized at increased output current levels, but power consumption will increase, possibly causing small shifts in linearity.

Pin 1, range control, may be grounded or unconnected. Although other older devices of this type require different terminations for various applications, the AD1408/AD1508 compensates automatically. This pin is not connected internally, therefore any previously installed connections will be tolerated.

Output Voltage Range

The voltage on pin 4 is restricted to a +0.5 to -0.6 volt range when $V_{EE} = -5V$. When V_{EE} is more negative than -10 volts, this range is extended to +0.5 to -5.0 volts. If the current into pin 14 is 2mA (full-scale output current = 1.992mA), a 2.5k Ω resistor between the output, pin 4, and ground will provide a 0 to -4.980 volt full-scale. If $R_{\rm I}$ exceeds 500Ω however, the settling time of the device is increased.

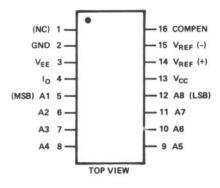
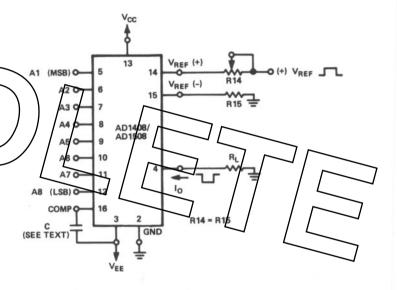
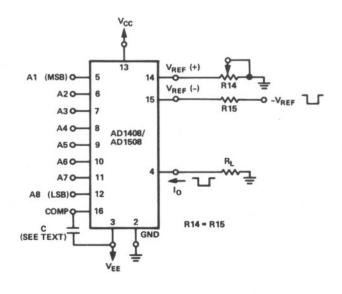


Figure 1. Pin Connections



a. Connections for Use with Positive Reference



b. Connections for Use with Negative Reference

Figure 2. Basic Connections

Voltage Output

A low impedance voltage output may be derived from the output current of the AD1408/AD1508 by using an output amplifier as shown in Figure 3. The output current I_O flows in R_O to create a positive-going voltage range at the output of amplifier A1. R_O may be chosen for the desired range of output voltage; the complete circuit transfer function is given in Figure 3.

If a bipolar output voltage range is desired, R_{BP}, shown dotted, must be installed. Its purpose is to provide an offset equal to one-half of full-scale at the output of A1. The procedure for calibrating the circuit of Figure 3 is as follows:

Calibration for Unipolar Outputs (No RBP)

- 1. With all bits "OFF", adjust the A1 null-pot, R1, for $V_{\rm OUT}$ = 0.00V.
- 2. With all bits "ON", adjust R_{REF} for V_{OUT} = (Nominal Full Scale) 1LSB = +9.961 volts

equired)

With all bits 'OFF'', adjust R_{BP} for V_{OUT} = -F.S. =

-5.000 volts

With Bit 1 (MSB) 'ON', and all other Bits 'OFF'',

3. With all bits "ON", verify that $E_{OUT} = 15.000V - 1LSB = 4.961V$.

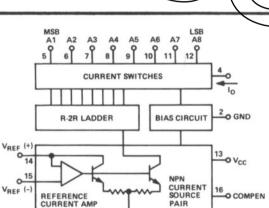
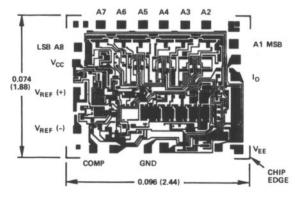
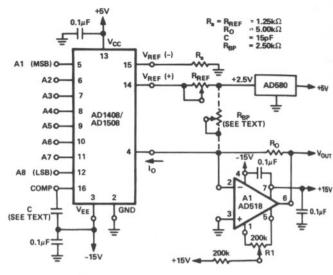


Figure 4. Simplified Block Diagram



THE AD1408/AD1508 IS AVAILABLE IN CHIP FORM GUARANTEED TO -7 LEVEL PERFORMANCE. CONSULT FACTORY FOR APPLICATION AND PRICING DETAILS.

Figure 5. Chip Dimensions and Pad Layout. Dimensions shown in inches and (mm).

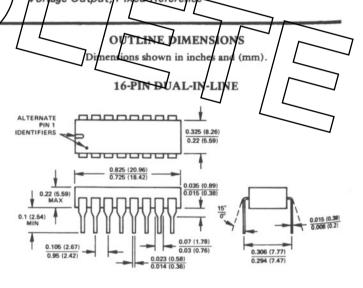


$$V_{OUT} = \frac{V_{REE}}{R_{REF}}(R_O) \left[\frac{A1}{2} + \frac{A2}{4} + \frac{A3}{8} + \frac{A4}{16} + \frac{A5}{32} + \frac{A6}{64} + \frac{A7}{128} + \frac{A8}{256} \right]$$

ADJUST $\rm V_{REF}$, $\rm R_{REF}$ OR $\rm R_{O}$ SO THAT WITH ALL DIGITAL INPUTS AT LOGIC "1", $\rm V_{OUT}$ = 9.961 VOLTS:

$$V_{\text{OUT}} = \frac{2.5}{1.35 \text{k}\Omega} (5 \text{k}\Omega) \left[\frac{1}{2} + \frac{1}{4} + \frac{1}{8} + \frac{1}{16} + \frac{1}{32} + \frac{1}{64} + \frac{1}{128} + \frac{1}{256} \right] = 9.961 \text{ VOLTS}$$

figure 3. Typical Connection Diagram, AD1408/AD1508, Voltage Output, Fixed Reference



AD1408/AD1508 ORDERING GUIDE

MODEL	ACCURACY (±% F.S.)	TEMP. RANGE (°C)	
AD1408-7D	0.39	0 to +75	
AD1408-8D	0.19	0 to +75	
AD1408-9D	0.10	0 to +75	
AD1508-8D	0.19	-55 to +125	
AD1508-9D	0.10	-55 to +125	
AD1508-8D/			
883B	0.19	-55 to +125	
AD1508-9D/			
883B	0.10	-55 to +125	