Notes on using Analog Devices' DSP, audio, & video components from the Computer Products Division
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AD1849K Jitter Requirements and Input Signal Coupling

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Overview

This edition of Engineer's Notes will shed some light on AD1849K jitter requirements listed in the data sheet when using an external clock source to drive the AD1849. Also discussed are AC vs. DC coupling of the input signal. The information is presented in a Q & A format.

Q & As

1. Please provide some specs for jitter requirements for the clock inputs (both SCLK and CLKIN and the relationship between them) of the AD1849k. The AD1849K data sheet mentions a low jitter requirement for external clocks used to drive the part. (I am compelled to use external clocks to synchronize with the rest of the system.) Could you please identify which clock signals in particular are susceptible to clock jitter? I understand that the sampling clock (SCLK) should be a low jitter clock but is this also a requirement for the over-sampling filter clock (MCLK) and the frame sync? Secondly, it would be of assistance if you could quantify the jitter requirements and outline the effects of clock jitter on the distortion and noise specifications for the part. How will the jitter affect THD and IMD. Will -80dB THD still be attainable with a jittery clock signal(s)?

Regarding jitter from an external clock source. Regardless of the clock source for a mixed signal device, the effect of jitter is to raise the noise floor and increase distortion. The effect of such jitter will depend on the sample rate, signal frequency and bandwidth and the amount of noise + THD already present. For most applications using the AD1849, i.e. 80dB S/N 50kHz sample rate and a 10kHz tone, the jitter added noise will be much less than the already present system noise (about -80dB) unless the jitter exceeds about 2ns. For details of jitter effects I would recommend one of the reference texts on digital audio or telecommunications.

2. In order to sync with an existing clock we wish to derive our 1849 clocks via a jittery PLL. The question is: how much jitter is acceptable on each of the SCLK and MCLK inputs?

The clocks most affected by jitter will be the Xtal inputs (if external clocks are used) or the serial bit clock (SCLK) if used as an input. Since usually only one clock source is used at a time, this will normally be the only one you have to worry about. As mentioned in item one above, jitter shouldn't be a problem if it is less than 2ns, which is much higher than obtained from most Xtal oscillators. A well designed PLL should also have a much better jitter performance than this.

3. Crystal data for the CS4215 says that the line inputs should be DC coupled for minimum output offset. The AD data says there is no advantage to DC coupling. Will DC coupling to the AD1849k generate loud pops when switching between the AC coupled mic input and the DC coupled line input as the data sheet suggests? I would have expected no noise as the inputs in both cases would be at the same DC potential. I intend biasing the driving op-amp with the AD1849k CMOUT, so that the only difference in DC levels will be that caused by the op-amp's output offset.

Regarding AC vs. DC input signal coupling. Yes, if you switch between different DC bias voltage levels, you will generate switching noise. The input to the CODEC internal Op-Amps, is biased to the CMOUT voltage, +/- the input offset of the Op-Amps. This input offset is typically less than 5mV and will not cause serious problems, i.e. 'pops & clicks' unless gained-up in subsequent signal processing. If you think your system may generate total input offsets in excess of 10 to 20 mV you may want to determine, by experiment, the maximum tolerable level of switched noise you can tolerate. Wider bandwidth applications where high S/N ratios are expected will be subjectively worse, especially if augmented by ringing in any filters.