Automotive Audio Bus A²B Transceiver

Silicon Anomaly List

AD2426/AD2427/AD2428

ABOUT AD2426/AD2427/AD2428 SILICON ANOMALIES

These anomalies represent the currently known differences between revisions of the A²B® AD2426/AD2427/AD2428 product(s) and the functionality specified in the AD2426/AD2427/AD2428 data sheet(s) and the Technical Reference manual.

SILICON REVISIONS

A silicon revision number with the form "-x.x" is branded on all parts. The silicon revision can be electronically determined by reading the **VERSION** register.

Silicon REVISION	VERSION[7:0]
0.1	0x01
0.0	0x00

ANOMALY LIST REVISION HISTORY

The following revision history lists the anomaly list revisions and major changes for each anomaly list revision.

Date	Anomaly List Revision	Data Sheet Revision	Additions and Changes
12/18/2019	C	Rev.A	Added Anomaly:18000044
07/18/2019	B	Sp0	Added Silicon Revision 0.1 Added Anomaly:18000030
03/22/2018	A	PrC	Initial Version

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SUMMARY OF SILICON ANOMALIES

The following table provides a summary of AD2426/AD2427/AD2428 anomalies and the applicable silicon revision(s) for each anomaly.

No.	ID	Description	Rev 0.0	Rev 0.1
1	18000027	PRBS Test Mode May Erroneously Report Bit Errors	x	x
2	18000028	BMMCFG.BMMRXEN Bit Does Not Behave as Expected	x	x
3	18000030	I2C Signals Clamp When I2C Bus Voltage Is Higher Than IOVDD	x	.
4	18000044	The I2C Clock Low Pulse Width Violates The Minimum Time When Operating In Fast Mode	x	x

Key: x = anomaly exists in revision
. = Not applicable

DETAILED LIST OF SILICON ANOMALIES

The following list details all known silicon anomalies for the AD2426/AD2427/AD2428 including a description, workaround, and identification of applicable silicon revisions.

1. 18000027 - PRBS Test Mode May Erroneously Report Bit Errors:

DESCRIPTION:
The PRBS (pseudorandom binary sequence) test mode may erroneously report bit errors when I2S/TDM transmit is enabled. This can occur on both master and slave transceivers.

WORKAROUND:
Do not run PRBS mode with I2S/TDM transmit enabled. In order to make sure I2S/TDM transmit is disabled, **`I2SCFG.TX0EN`** and **`I2SCFG.TX1EN`** must be cleared on each node before entering PRBS mode.

APPLIES TO REVISION(S):
0.0, 0.1

2. 18000028 - BMMCFG.BMMRXEN Bit Does Not Behave as Expected:

DESCRIPTION:
In bus monitor mode, the A-side LVDS receiver should always be disabled when **`BMMCFG.BMMRXEN`** = 0. Due to this anomaly, this behavior only occurs when the PLL is locked.

WORKAROUND:
Use an external switch to control the LVDS traffic going to the A-side of a transceiver in bus monitor mode.

APPLIES TO REVISION(S):
0.0, 0.1

3. 18000030 - I2C Signals Clamp When I2C Bus Voltage Is Higher Than IOVDD:

DESCRIPTION:
If the I2C Bus Voltage (I2C_VBUS) is greater than IOVDD, the I2C signals may clamp to a voltage level that is lower than I2C_VBUS. This is due to the activation of internal ESD diodes on the transceiver's SCL and SDA pins, and the resulting clamping may result in violation of the VIH spec of other devices on the I2C bus. The following table summarizes the effect of this anomaly for different cases:

I2C_VBUS	IOVDD	Remarks
1.8V	1.8V	No Issue
3.3V	3.3V	No Issue
3.3V	1.8V	I2C signals clamp to an intermediary voltage level. Other devices connected to the I2C bus must have maximum VIH specs that are below the clamped voltage. Low reliability risk. A worst-case circuit analysis must be performed at the system level to verify operation at these voltage levels.
5V	1.8V or 3.3V	Not supported.

WORKAROUND:
Operate both I2C_VBUS and IOVDD at 1.8V or 3.3V only.

A pull-up resistor on the SCL/SDA pins ensures that the internal ESD diodes are not damaged when I2C_VBUS is powered while IOVDD is not:

1. When I2C_VBUS is 1.8V, use at least a 1KOhm pull-up resistor on the I2C pins.
2. When I2C_VBUS is 3.3V, use at least a 2KOhm pull-up resistor on the I2C pins.

APPLIES TO REVISION(S):
0.0

4. 18000044 - The I2C Clock Low Pulse Width Violates The Minimum Time When Operating In Fast Mode:

DESCRIPTION:
When the A^2B transceiver operates as I2C master in Fast Mode (400KHz), the I2C clock low pulse width (t_{LOW}) doesn't meet the minimum duration as per I2C 2.1 specification. The transceiver can assert a minimum of 1.21us instead of 1.3us as per I2C 2.1 specification.

If there is sufficient margin for the data setup(t_{DS}) and data hold time(t_{DH}), the t_{LOW} violation will not lead to functional failures. If the peripheral on I2C bus supports Fast Mode Plus adhering to I2C 2.1 specification, there will not be functional failures due to this anomaly. Fast Mode Plus devices have margin for data setup and data hold with 1.21us t_{LOW}

WORKAROUND:
Use one of the workaround.

1. Operate I2C in Standard Mode (100KHz) of operation
2. Choose an I2C peripheral that supports Fast Mode Plus

APPLIES TO REVISION(S):
0.0, 0.1