ANALOG DEVICES

AN-203
APPLICATION NOTE

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Using the AD2S80A Series Resolver-to-Digital Converters As a Control Transformer

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INTRODUCTION

The AD2S80A, AD2S81A and AD2S82A are monolithic, tracking resolver-to-digital converters, whose important features are: Ratiometric Tracking Conversion, Dynamic Performance Selected by the User, Variable Resolution Up to 16 Bits Selected by the User, Velocity Output, and 8-/16-Bit Bus Interface.

This application note does not discuss the basic operation or specifications of the AD2S80A series converters; detailed information can be found in the relevant data sheets.

The description, basics of operation and circuit implementation are given for a positional servo control system using a resolver and an AD2S80A series resolver-to-digital converter.

CONTROL TRANSFORMER

Traditionally a control transformer (CT), an electromechanical device, would be fed by the output of a control transmitter (CX), thus forming a synchro/resolver control chain.

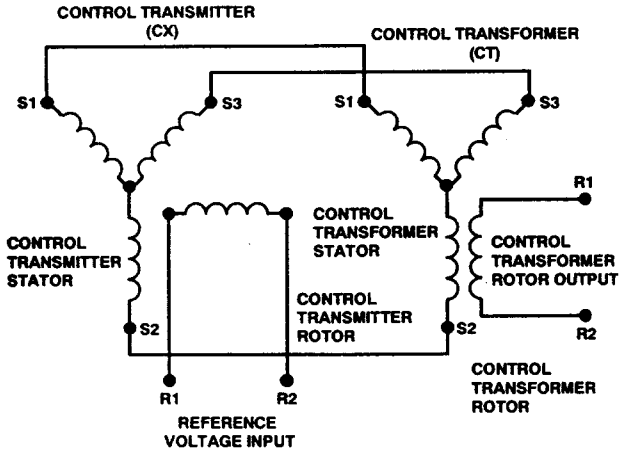

Figure 1. Synchro/Resolver Control Chain

In a control chain, when the shaft angle position of the CX equals the shaft angle position of the CT, a null voltage will appear on the rotor terminals R1 and R2 of the CT.

Any slight positional deviation from this alignment will produce a signal in the rotor winding whose phase relative to the reference voltage will depend on the direction of the deviation.

The control transformer can, therefore, be considered as a null detector and is used as such in servo systems (Figure 2).

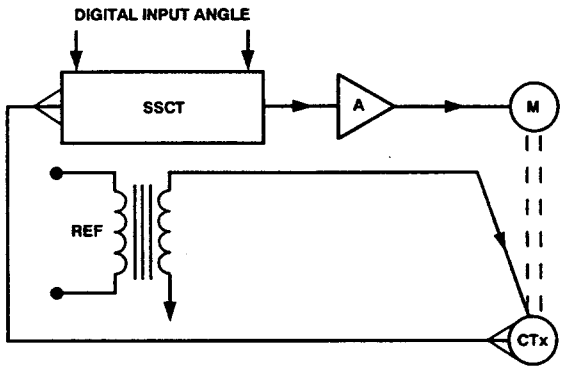

Figure 2.

Analog Devices has historically manufactured models SSCT1621 and RSCT1621, synchro and resolver input respectively, which were solid-state control transformers. The function of the above devices was identical to electromechanical control transformers, except that the mechanical inputs have been replaced by electronic digital inputs. A solid-state control transformer accepts either three-wire synchro or four-wire resolver input information and a parallel binary digital input angle. The output voltage amplitude is modulated at the carrier frequency with a magnitude proportional to the sine of the difference between the synchro (or resolver) angle and the binary digital input angle.

The output can be described by:

$$A \sin 2\pi ft \sin(\theta - \phi)$$

where: "A" is the amplitude of the ac error signal,
"sin 2 π ft" is the modulation frequency of the carrier,
"θ" represents the shaft input angle of the 3-wire synchro (or 4-wire resolver),
"ϕ" represents the parallel binary digital input angle and "f" is the carrier (excitation) frequency.

AD2S80A AS A CONTROL TRANSFORMER

The ratio multiplier section of the AD2S80A can be used independently to the rest of the converter to perform the function of control transformer. In this mode the signal from the resolver shaft, input angle θ, is compared to the parallel binary digital angle ϕ, loaded into the counters, Bit 1 (MSB) to Bit 16 (LSB), Pins 9 to 24 respectively.

Parallel Binary Data

The AD2S80A series accepts 16-bit parallel binary data. Please note that the byte select (Pin 27) input is non-operative in Control transformer mode. If less than 16 bits are required to be loaded into the AD2S80A series, the spare data inputs must be pulled to Logic HI with 10 kΩ pull up resistors. The pull up resistors above, would not affect the operation of the AD2S80 series in the R/DC mode.

In order to load a parallel binary digital angle into the counters of the AD2S80A:

1. The INHIBIT should be Logic HI.
2. The AD2S80A should be placed into high impedance state by using the ENABLE (Pin 26)—Logic HI places the parallel binary digital angle outputs in high impedance state.
3. Subsequently the parallel binary digital angle data may be loaded into the counters by using an external open collector driver to pull the DATA LOAD (Pin 32), to Logic LO. Note: The DATA LOAD is internally pulled to +12 V (Logic HI) with an (internal) 100 kΩ resistor. If an additional pull-up is required, it should be placed externally and connected to +12 V supply. The resulting pull-up resistor value would then be the parallel combination of the internal 100 kΩ resistor with the external additional resistor.

Any difference between the above two angles (θ–ϕ) results in an analog voltage, sin (θ–ϕ) modulated at reference frequency, at the ac error output (Pin 3 of AD2S80A). This is the control transformer output of the AD2S80A.

The ac error output signal is given by:

$$A1 \sin 2\pi ft \sin(\theta - \phi)$$

where *f* is the carrier (reference) frequency.

A1 is the gain of the ratio multiplier stage which is × 14.5

For 2 V rms input signals the ac error output (in volts/bit of error) is given by:

$$2 \times SIN\frac{360}{p} \times A1$$

Where p is = bits per revolution
= 1024 for 10-bits resolution
= 4096 for 12-bits resolution
= 16384 for 14-bits resolution
= 65536 for 16-bits resolution

The ac error output scaling of the AD2S80 is:

178 mV rms per bit at 10-bits resolution (1 in 1024)
44.5 mV rms per bit at 12-bits resolution (1 in 4096)
11.125 mV rms per bit at 14-bits resolution (1 in 16384)
2.78 mV rms per bit at 16-bits resolution (1 in 65536)

It is recommended that the AC ERROR OUTPUT is buffered with the circuit shown in Figure 3, if this signal is to be used.

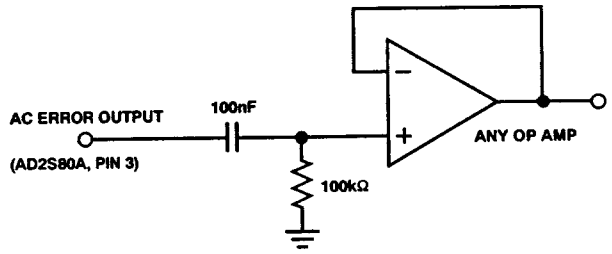

Figure 3. AC Error O/P Buffer

There are additional functions in the AD2S80A which can be used to further process the ac error output signal.

HIGH FREQUENCY FILTER

The high frequency filter is used to remove any dc offset from the ac error output prior to this signal being fed to the phase sensitive demodulator, and also to attenuate any high frequency "noise" which may have been induced to the converter if it is situated in particularly noisy environments.

The HF filter suggested in the AD2S80A data sheet, Figure 1 (R1, C1, R2, C2) gives an attenuation of 3 at the reference frequency.

For further information please see AD2S80A series data sheets.

PHASE SENSITIVE DEMODULATOR

The phase sensitive demodulator is used to derive a mean dc error voltage, available at the DEMODULATOR OUTPUT (Pin 40), from the ac error input signal to the PSD (DEMOD I/P, Pin 2).

$$DEMOD\ O/P = \frac{\pm 2\sqrt{2}}{\pi} \times (DEMOD\ I/P)$$

The above relationship applies to sinusoidal signals in phase or antiphase with the reference frequency.

Note: phase shift effects are excluded from the above relationship. The contribution of phase shifts would be to reduce the mean dc voltage value.

The scaling of the DEMODULATOR OUTPUT voltage is shown below:

DC Error Scaling
= 160 mV per bit at 10-bits resolution (1 in 1024)
= 40 mV per bit at 12-bits resolution (1 in 4096)
= 10 mV per bit at 14-bits resolution (1 in 16384)
= 2.5 mV per bit at 16-bits resolution (1 in 65536)

PID CONTROLLER CIRCUIT
The DEMODULATOR OUTPUT voltage (dc error of the converter) can be further processed to form the error signal in a PID (Proportional, Integral, Differential) type controller for closed loop position servo control system shown in Figure 5.

PROPORTIONAL TERM
The Proportional (Gain) element of the controller is the inverting amplifier A1 and its associated components.

The aim of this circuit is to react very rapidly to a change of the input error in order to reach a steady state. However, there is always an offset error (dead band), thus the output from the proportional term on its own never assumes the value required to reduce the error to zero; the larger the amplification the smaller the residual error signal.

The feedback loop consists of resistors R2 and R3 in parallel; diodes D1 and D2 are in series with R3, thus forming a nonlinear gain network. This was designed in such a way as to give maximum gain at low error signals, in both rotational directions, in order to overcome motor stiction. The ratio of minimum error (maximum gain) to maximum error (minimum gain) in this circuit is 3:2.

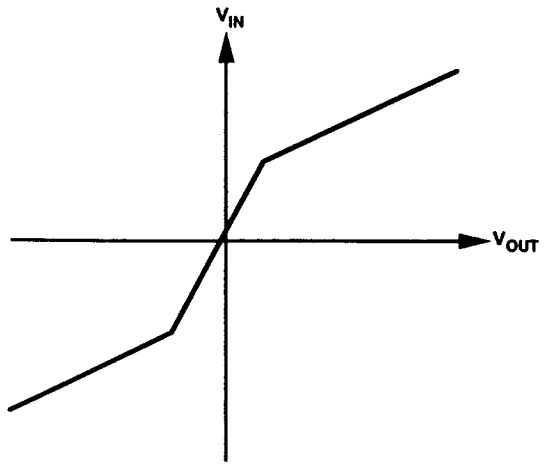

Figure 4. Input vs. Output Voltage of the Proportional Term

INTEGRAL TERM
The function of the integrating term is to eliminate any residual errors due to circuit offsets and/or motor stiction/response.

The integrating element of the controller is the inverting amplifier A2 and its associated components.

This circuit is an integrator whose time constant is given by:

$$T_I = R8\,C1$$

The "Reset Time" constant = VR1 × C1.

The "Reset Time" can be made adjustable by the user for tuning purposes by the optional potentiometer VR1. In order to make the phase advance negligible, the value of VR1 must be small compared with the value of R8.

VR1<<R8
i.e., 50 kΩ, 1 MΩ respectively.

DIFFERENTIAL TERM
The function of the differential term is to reduce the output of the error signal processing circuit (PI controller) by limiting the rate of change of the positional error voltage input to the PID controller.

The differentiating element of the controller is the amplifier A3 which is connected as a differentiator or differentiating time constant is:

$$T_D = R6\,C3$$

The greater the rate of change of the positional error signal, the greater is the output voltage of A3.

The inclusion of capacitor C2 (small value) is to provide some smoothing because purposefully there is no smoothing on the error signal of the AD2S80A which is a fully rectified waveform at reference frequency.

PID SUMMING AMPLIFIER
With reference to Figure 4, the proportional, integral and differential terms are summed by amplifier A4, in such a way as to provide an output to a motor drive; or as in this case to a power amplifier that in turn drives a small dc motor.

From the functional description of the three terms given above, it is worth noting that the P term and the D term are added together; the function of the D term is to limit the input signal's rate of change, i.e., oppose the output of the P term.

The I term is subtracted from P + D as it is "inverted" by amplifier A2.

The advantage offered by the above configuration is a fast-acting I term as it is driven by the amplified error signal (Amp A1). This configuration would be applicable to fast-acting small motors with low inertia loads.

AD2S80A Series Parameters Applicable to Control Transformer (Typical at +25°C)

Parameters	AD2S80A Series	Units	Comments
GAIN	× 14.5		Input Signals (Sin, Cos) to AC Error Output
PROPAGATION DELAY	150	ns	Digital Inputs to AC Error Output
AC ERROR AMPLIFIER OUTPUT DC Offset Voltage Output	 ±200 ±350 ±9	 mV mV maximum V peak-to-peak	
VOLTAGE OUTPUT SETTLING TIME	1.5 6	µs µs	Small Step <10° Large Step 179°C Digital Inputs Bit 1 (MSB) to Bit 16 (LSB) to AC Error Output
LINEARITY	1%		Up to ±5° Error
ATTENUATION OF THE AC ERROR SIGNAL BY THE HIGH FREQUENCY FILTER	÷3		Using the Passive Component R1, C1, R2, C2 as Recommended for the AD2S80A Resolver-to-Digital Converter
PHASE SENSITIVE DETECTOR GAIN	−0.9		

It is permissible to use a slightly different configuration. The I term input is connected to the dc positional error signal (Node R1, R5 and AD2S80A Pin 40). The output of A2 should be connected via R12 to the inverting input of A4 and be added with the P and D terms. See dotted lines in Figure 5.

The advantage of the second configuration is a slower acting I term. It would be better suited to larger motors which would drive an inertial load.

"Read Back" Mode

When the AD2S80A series of resolver-to-digital converter is utilized in the way described above, only certain functional parts of the device are used; namely the input latches (counter), the high precision ac ratio multiplier (ac error) and the phase sensitive detector (dc error).

By using the remaining functions of the device, it is possible to "read back" into a microprocessor the position which the motor has attained by use of the PID circuit.

The following should be noted:

1. To aid the transition from the Control Transformer mode to "Read Back" mode a READY signal may be derived from the level of the dc error signal. A "window" comparator, shown in Figure 6 may be used to detect the voltage signal level of the dc error. If this level is set for example at ±40 mV, it corresponds with an error of ±4 bits, when using the AD2S80A at 14-bit resolution (1 bit in 14 = 1.3 arc min).

   For further information please see the DC Error Scaling section. To avoid continuous switching of the comparators the dc error signal should also be buffered and smoothed before it is applied to the "window" comparator.

2. When the converter is placed into "Read Back" mode, the output of the PID circuit to the power amplifier (or motor drive) should be disconnected and connected in turn to 0 V because otherwise the integral term will integrate any residual errors/circuit offsets resulting in applying a drive signal to the motor without the presence of any feedback. See Figure 6.

3. For the "Read Back" mode the resolver-to-digital converter should be connected for normal operation as described in the relevant data sheets, and the passive components around the tracking loop should be used.

Applications of the Control Transformer

Synchro/Resolver Control Chains

Traditional Synchro/Resolver Control Transformer Chains as shown in Figure 1 normally lack power at the receiver Rx end of the chain. If the Rx synchro/resolver is replaced by a dc motor/gearbox/resolver combination and the PID circuit, then the power is only limited by the rating of the dc motor. In such a system the parallel 16 bit data would be replaced by a synchro/resolver to digital converter at the Tx end, and a parallel to serial digital interface. At the Rx end the serial digital information would be presented as parallel digital data by use of a serial to parallel interface. The advantages such a system would offer are:

High torque at the Rx,
Lower cost due to utilization of reasonably priced resolvers,
High noise immunity serial digital interface which could incorporate isolation barriers in the form of either opto-isolators or pulse transformers,
A reduction on the number of wires in the chain, thus saving weight and, if required, making use of the optical fiber technology for "tap free communication" links.

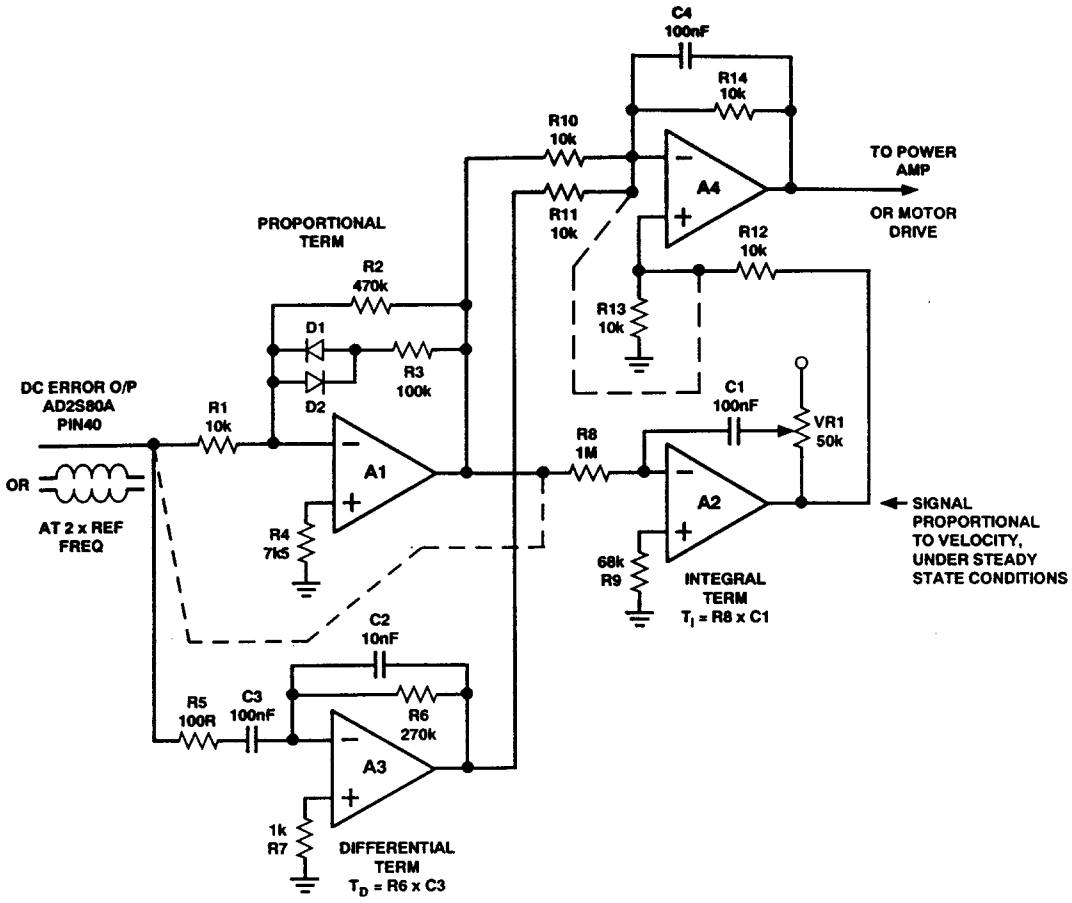

Figure 5.

Position Servo Systems

By using the AD2S80A Series in the Control Transformer mode as well as in the R/DC mode, the design of a positional servo can be simplified and the performance and accuracy of the system enhanced, limited only by budgetary restraints of the motor, resolver and accuracy grade of the R/DC.

The implementation of the digital processing part of the system does not require a powerful 16-bit microprocessor because of the closed-loop positional feedback in the AD2S80A/Motor/Resolver configuration.

The AD2S80A appears to the microprocessor as a DAC into which the required 16-bit position can be "written." Then the analog PID control loop takes over the error processing to ensure that the demanded 16-bit position is maintained regardless of load variation and fluctuation and, most important, without the frequent supervision of the attained position by the μP. Thus the μP may be released to perform other tasks for which it is better suited (number crunching!). For instance, a relatively low power 8-bit μP can be used to control a number of axes, for example in a robot, just by coordination of the required (demanded) positions of the axes.

Velocity (Speed) Control

By constantly changing the demanded digital position, (angle ϕ), e.g., by a 16-bit binary counter, the ac error output (θ–ϕ) and subsequently the dc error output that drives the PID loop circuit attain a voltage signal level that in turn drives the motor in such a manner as to maintain the demanded position.

By introducing a constant rate of change of position demand, i.e., d. position (demand) = velocity (demand), a 16-bit parallel binary counter (a digital set point, angle ϕ) is given to the 2S80 + PID circuit).

For example a 16-bit parallel digital linear counter can be used driven by a variable frequency "clock" pulse.

The constant rate of change of the demanded digital position (angle ϕ) in turn will drive the ac error signal (SIN (θ–ϕ) to an increasing value. Subsequently the dc error value will increase at the same rate as the ac error. The PID loop circuit will output a voltage signal which will drive the motor in such a manner so as to "keep up" with the changing demanded position.

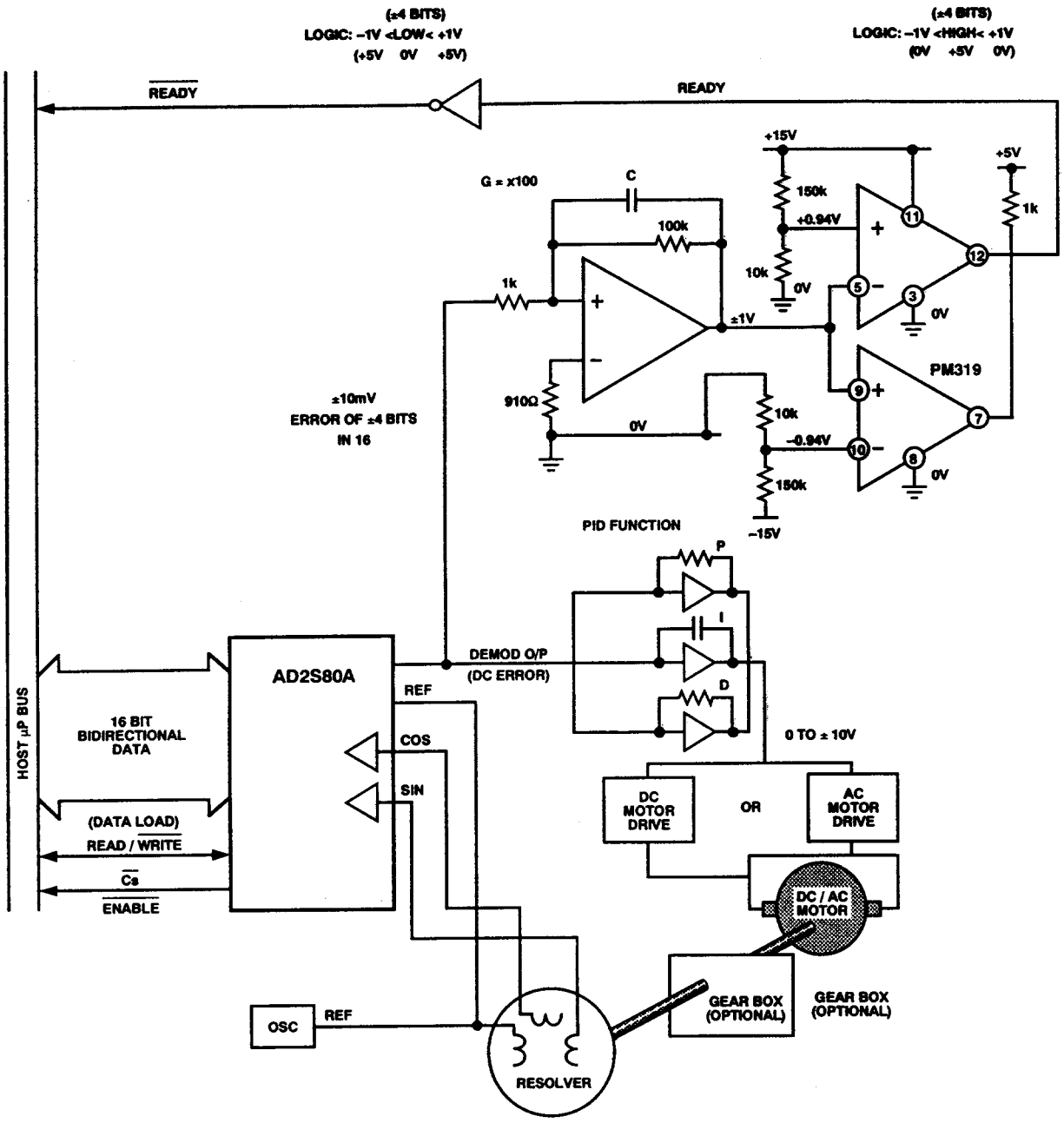
(±4 BITS)
LOGIC: –1V <LOW< +1V
(+5V 0V +5V)
(±4 BITS)
LOGIC: –1V <HIGH< +1V
(0V +5V 0V)
READY
READY
+15V
+5V
G = x100
C
150k
1k
100k
+0.94V
1k
10k
0V
±1V
0V
PM319
±10mV
ERROR OF ±4 BITS
IN 16
910Ω
10k
0V
–0.94V
150k
–15V
PID FUNCTION
P
I
D
AD2S80A
DEMOD O/P
(DC ERROR)
REF
COS
SIN
0 TO ± 10V
HOST µP BUS
16 BIT
BIDIRECTIONAL
DATA
(DATA LOAD)
READ / WRITE
Cs
ENABLE
DC
MOTOR
DRIVE
OR
AC
MOTOR
DRIVE
DC / AC
MOTOR
GEAR BOX
(OPTIONAL)
GEAR BOX
(OPTIONAL)
OSC
REF
RESOLVER

Figure 6.