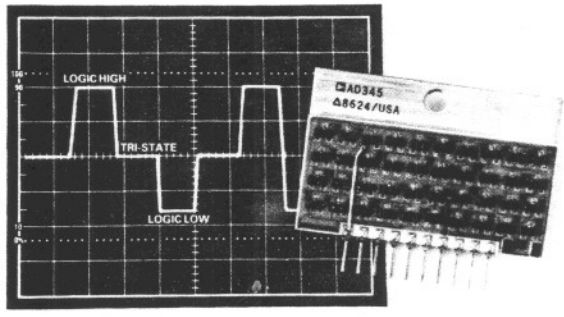
High-Speed Pin Driver with Inhibit Mode

AD345

FEATURES
- 100MHz Driver Operation
- Driver Inhibit (Tristate) Function
- Guaranteed Industry Specifications
  - 50Ω Output Impedance
  - 1V/ns Slew Rate
  - Variable Output Voltages for ECL, TTL and CMOS
- High-Speed Differential Inputs for Maximum Flexibility
- Small SIP Package
- Low Cost

APPLICATIONS
- Automatic Test Equipment
  - Semiconductor Test Systems
  - Board Test Systems
- Instrumentation & Characterization Equipment
- General Purpose Driver



PRODUCT DESCRIPTION

The AD345 is a complete high-speed pin driver designed for use in digital test systems. By combining surface mount technology and thick-film laser trimmed technology, this product attains superb electrical performance while preserving optimum packaging densities in a convenient 10-pin SIP package.

Featuring unity gain programmable output levels of −3 to +8 volts with output amplitude capability of 700mV to 11V, the AD345 is designed to stimulate ECL, TTL and CMOS logic families. The 100MHz (5ns pulse width) data rate capacity, 1V/ns controlled slew rate, and 50Ω output impedance allows for real-time stimulation of these digital logic families. To test I/O devices the pin driver can be switched into a high impedance state (inhibit or tristate) by using the inhibit mode. The pin driver leakage in tristate is typically 50nA and output charge transfer going into tristate is guaranteed at 200pC maximum.

The AD345 transition from hi/low or to tristate is effected through the data and inhibit inputs. The input circuitry is implemented utilizing high-speed differential inputs with a common-mode range of 8 volts. This allows for direct interface to the precision of differential ECL timing or the simplicity of stimulating the pin driver from a single ended TTL or CMOS logic source. The analog inputs V high or V low are equally easy to interface. Requiring typically 500μA of bias current, the AD345 can be directly coupled to the output of a DAC either singularly or in parallel with several other pin drivers.

The AD345 utilizes surface mount technology creating a small single in-line package which can be mounted upright or laying down (leads bent 90°) depending on the specific application. The SIP packaging enables the user to create a tight radial test head design or a custom high-speed dedicated probe card with the drivers placed in close proximity to the device under test guaranteeing optimum signal integrity. A metal tab is mounted on the back side allowing for heatsinking or mechanical support. The AD345 is available for operation over the 0 to +70°C range.

PRODUCT HIGHLIGHTS

1. The AD345 is a complete 100MHz pin driver designed to meet the requirements of ATE manufacturers.
2. Output high voltage level is adjustable from −2V to +8V and output low levels from −3 to +6V allowing compatibility with ECL, TTL, CMOS logic levels.
3. Certified large signal slew rates of better than 1V/ns with dynamic output impedance laser trimmed for waveform integrity and guaranteed performance with 50Ω transmission lines.
4. TRISTATE (inhibit) capability for testing I/O devices.
5. INHIBIT leakage current of 50nA typical virtually eliminates the requirement for a disconnect relay in a semiconductor test system.
6. Repeatability from driver-to-driver is guaranteed to meet published specifications through pretesting and active laser trimming.
7. The 10-pin SIP hybrid package with mounting tab provides high functional mechanical densities with maximum versatility.

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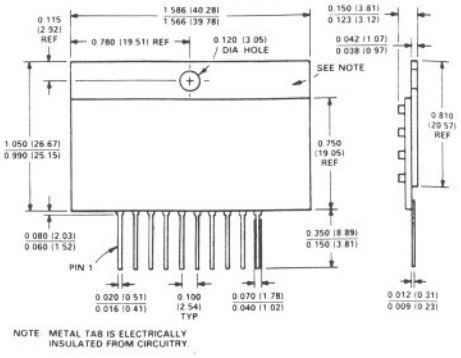
SPECIFICATIONS (All specs @ 25°C in free air, output unloaded, +V = +12V, −V = −8V, unless otherwise specified)

Parameter	AD345KY Min	Typ	Max	Units	Comments
DIFFERENTIAL INPUT CHARACTERISTICS					
D to $\overline{D}$, INH to $\overline{INH}$					
Voltage Range	$-V_S + 6V$		$+V_S - 6V$	Volts	
Pulse Amplitude	0.37	ECL	3.5	Volts p-p	See Note 1
Bias Current		500	750	μA	
REFERENCE INPUTS					See Note 2
V_{HIGH}	−2		+8.3	Volts	
V_{LOW}	−3		+6.2	Volts	
Bias Current		500	750	μA	
OUTPUT CHARACTERISTICS					See Notes 2 & 3
Logic High Range	−2		+8	Volts	
Logic Low Range	−3		+6	Volts	
Amplitude	0.7		11	Volts	
Initial Offset	−30		+30	mV	See Note 3
Gain Error	−1.2		+1.2	% of Set Level	Normalized to Figures 1 & 2
Output Voltage Temp. Coeff.		0.5	1.0	mV/°C	
Current Drive					
Static			60	mA	
Dynamic			100	mA	
Output Capacitance		9		pF	
Output Charge Going Into Inhibit Mode			200	pC	
Leakage Current in Inhibit Mode		50	200	nA	
Protection					
Output @ GND	INDEFINITELY				
Output @ +V	1 Minute w/o Damage				
Output @ −V	1 Minute w/o Damage				
DYNAMIC PERFORMANCE					See Notes 4 & 5
Driver Delay Time	1.5	2.0	2.5	ns	
Driver Delay Matching					
Edge to Edge	−0.5		+0.5	ns	
Driver to Driver	−1.0		+1.0	ns	
Slew Rate					
1V Swing 20% – 80%		1.5	2.5	ns	
4V Swing 10% – 90%		3.5	4.0	ns	
Large Signal	1.0	1.25		V/ns	
Toggle Rate			100	MHz	ECL Output Level
Overshoot and Preshoot					
In Driver Mode					
1V Swing			200	mV	
>2V Swing			120	mV	
In Inhibit Mode		350		mV	
Settling Characteristic			5	% of Steady State 50ns after Starting Time of Voltage Slew. Steady State is Greater Than 1ms after Starting Time of Voltage Slew.	
Inhibit Delay Time					
Inhibit to Active	14	15	16	ns	See Notes 6 & 7
Active to Inhibit	5.5	8	10.5	ns	See Notes 6 & 7
Output Impedance	47.5	50	52.5	Ω	See Note 8
POWER SUPPLIES					
$-V_S$ to $+V_S$ Range	20		25	Volts	
Positive Supply Range	+11	+12	+15	Volts	
Negative Supply Range	−5	−8	−10	Volts	
Current		100		mA	
+PSRR V_{OH} = 8V	−70		+70	mV	+V = ±2.5%
−PSRR V_{OL} = −3V	−60		+60	mV	−V = ±2.5%

NOTES
[1]The maximum allowable voltage from D to $\overline{D}$ and from INH to $\overline{INH}$ is 3.5V.
[2]The output voltage range is specified for −3V to +8V for typical power supply values of −8V and +12V but can be offset for different values of V_{OUT} such as 0V to +11V as long as the required headroom of 4V between V_H and $+V_S$ are maintained and the negative headroom of 5V between V_L and $-V_S$ is preserved.
[3]Dynamically trimmed at 5MHz, 50% duty cycle.
[4]Delay times are measured from the crossing of differential ECL outputs at inputs of the device to a 250mV transition at output with V_H and V_L set to ±1V respectively.
[5]Delay times, slew rates, overshoot and undershoot performance specified with a 10k, 2pF probe. Oscilloscope bandwidth to exceed 300MHz.
[6]Inhibit mode delay times are measured from the crossing of differential ECL outputs at INH inputs to threshold crossing at the pindriver output. V_{OUT} is connected to a 100Ωload terminated at +2V dc. The V_H and V_L are set to a normalized +3.5V and +0.5V respectively. High delay times are measured to a +1.5V threshold. Frequency is set to 10MHz with a 50% duty cycle.
[7]The inhibit delay time specification allows for device-to-device variations. The stability and jitter of a given device is better than 1ns and 200ps respectively.
[8]Dynamically trimmed at the factory for 50Ω. Other impedance values can be obtained on special request.
Specifications subject to change without notice.

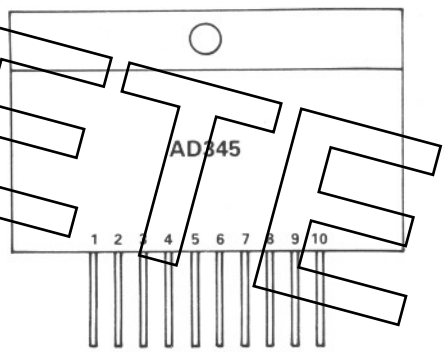
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



PIN CONFIGURATION

Component Side View



PIN NO.	SYMBOL	FUNCTION
1	V_L	Voltage Logic Low
2	V_H	Voltage Logic High
3	D	Driver Input
4	$\overline{D}$	$\overline{Driver}$ Input
5	$+V_S$	Positive Supply
6	$-V_S$	Negative Supply
7	V_{OUT}	Driver Output
8	GND	Circuit Ground
9	$\overline{INH}$	$\overline{Inhibit}$ Input
10	INH	Inhibit Input

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range . . . . . 0 to +70°C
Storage Temperature Range . . . . . −65°C to +125°C
Power Supply Voltage
  $+V_S$ to GND . . . . . +15V
  $-V_S$ to GND . . . . . −10V
  Difference from $+V_S$ to $-V_S$ . . . . . +25V
Input . . . . . $-V_S$ to $+V_s$
V_{OUT} . . . . . $+V_S$ +0.6V or $-V_S$ −0.6V
V_{OUT} to Short Circuit
  to GND . . . . . Indefinitely
  to +V or $-V_S$ . . . . . 1 Minute

DETERMINING LOGIC SET LEVELS

Within a system it is possible to minimize gain error and increase the output level accuracy of the AD345 by using the information provided by Figures 1 and 2. Figure 1 is a table of desired output high levels followed by the recommended input reference levels. Figure 2 accomplishes the same for the output low levels. Values of output levels not supplied by the tables can simply be interpolated from the data supplied.

Another potential source of output level error is offset error. The value, once determined for a specific device, should be algebraically subtracted for the appropriate V_{HIGH} or V_{LOW} set value.

V OUTPUT HIGH	V_H INPUT LEVEL
−2.00V	−2.016
−1.00V	−1.009
+1.00V	+1.007
+2.00V	+2.018
+3.00V	+3.028
+4.00V	+4.041
+5.00V	+5.054
+6.00V	+6.070
+7.00V	+7.098
+8.00V	+8.150

Figure 1. Table of Normalized V_{HIGH} Levels

V OUTPUT LOW	V_L INPUT LEVEL
−3.00V	−3.012
−2.00V	−2.007
−1.00V	−1.008
+1.00V	+1.015
+2.00V	+2.023
+3.00V	+3.031
+4.00V	+4.040
+5.00V	+5.050
+6.00V	+6.060

Figure 2. Table of Normalized V_{LOW} Levels

FUNCTIONAL DESCRIPTION

The AD345 is a complete high-speed pin driver designed for use in general purpose instrumentation and digital functional test equipment. The purpose of a pin driver is to accept digital, analog and timing information from a system source and interface those elements to the input of a digital device to be tested.

The circuit configuration for the AD345 has been summarized in Figure 3. Simply stated a pin driver performs the function of a precise, controlled, high-speed level translator with an output which can be disabled. The AD345 accepts digital information utilizing high-speed comparators on the D, $\overline{D}$ and INH, $\overline{INH}$ from ECL differential outputs for precise timing at logic cross-over and high-noise immunity. The wide input voltage range allows for ECL operation between 0 to −5.2V, or +2V to −3.2V and +5V to 0V. Where timing is less critical TTL or CMOS logic levels may be used to toggle the AD345. By biasing the $\overline{D}$ and $\overline{INH}$ inputs to approximately +1.3V for TTL and $1/2V_{CC}$ for CMOS, the D and INH inputs can be directly stimulated from these single-ended output sources. The output of the pin driver will follow the logic state of the D input providing the inhibit input is low. When the inhibit level is asserted the output will be disconnected and any activity on the input will not be transferred to the output.

Analog information is input to the pin driver through the V_H and V_L terminals as a reference voltage. These analog voltages are then buffered using unity gain followers. The resulting gain error has been characterized in Figures 1 and 2. System timing requirements are achieved through a specified 2.0ns, ±500ps second driver propagation delay, 1.25V/ns slew rate, defined preshoot and overshoot, and a dynamically trimmed 50Ω output impedance.

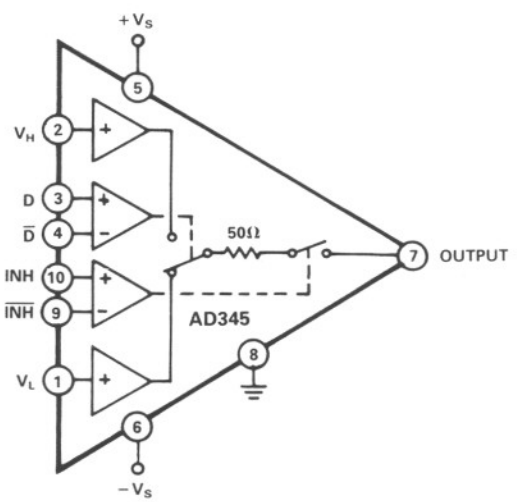


Figure 3. AD345 Block Diagram

LAYOUT CONSIDERATIONS

While it is generally considered good engineering practice to capacitively decouple an active device from the power supplies, it is absolutely essential for a high-power, high-speed device such as the AD345. The engineer merely has to consider the current pulse demanded from the power supply when a dynamic current change of −90mA to +90mA is required in only a few nanoseconds. Therefore, a 0.01μF high frequency decoupling capacitor must be located within 0.25 inches of the $+V_S$ and $-V_S$ terminals to a low impedance ground. A 10μF capacitor should also be situated between the power supplies and ground, however, the proximity to the device is less critical assuming low impedance power supply distribution techniques are employed. Circuit performance will be similarly enhanced and noise minimized by locating a 0.01μF capacitor as close as possible to V_H, V_L and connected to ground. Bypass considerations have been summarized in Figure 4.

An equally important consideration is the use of microwave stripline techniques on the output of the AD345. Failure to preserve the 50Ω output impedance of the pin driver will result in unwanted reflections, ringing and general corruption of the output waveshape. Care should therefore be exercised when selecting etch widths and routing, wire and cable to the device to be tested, and in choosing relays if they are required.

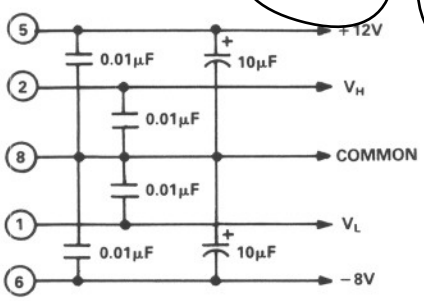


Figure 4. Basic Circuit Decoupling

The quality of the ECL differential driving source to the data inputs of the AD345 is another important consideration. The ECL driving outputs should be located close to the D and $\overline{D}$ inputs of the pin driver. Due to the low propagation delay of the AD345 excessive overshoot at the D input can be coupled to the pin driver output at low pulse amplitudes. In this case, an isolation resistor of approximately 62Ω can be inserted between the ECL output and the D input to the pin driver without any degradation in performance.

APPLICATIONS

The AD345 has been optimized to function as a pin driver in an ATE test system. Shown in Figure 5 is a block diagram illustrating the electronics behind a single pin of a high-speed digital functional test system with the ability to test I/O pins on logic devices. The AD345 pin driver, AD9687 high-speed dual comparator, and the AD394 quad 12-bit voltage DAC would comprise the pin electronics portion of the test system. Such a system could operate at 100MHz in the data mode or 50MHz in the I/O mode, yet fit into a neat trim package.

ORDERING GUIDE

Model	Temperature Range	Quantity	Price
AD345KY	0 to +70°C	1-24	$158.00
		25-99	$134.00
		100 +	$115.00

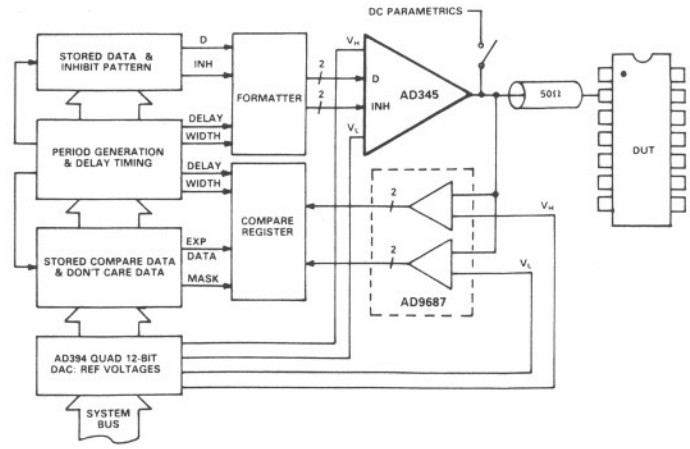


Figure 5. High-Speed Digital Test System Block Diagram

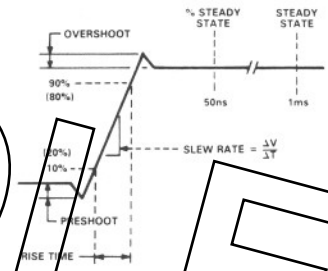


Figure 6. Definition of Terms

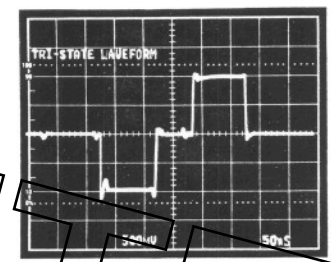


Figure 7. ±1 Volt Waveform with Inhibit (Output Terminated into 50Ω)

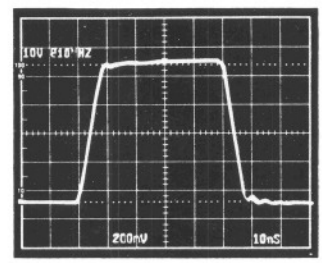


Figure 8. Large Signal 50ns Pulse

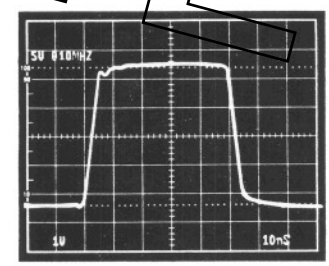
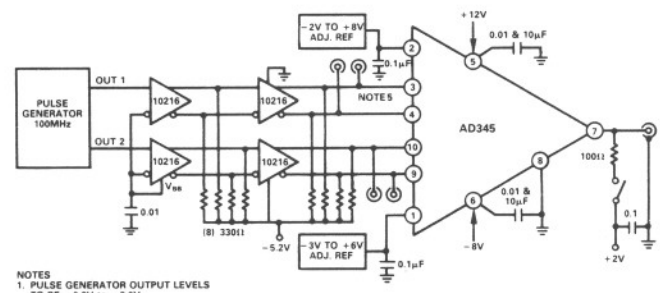


Figure 9. 5 Volt 50ns Pulse



NOTES
1. PULSE GENERATOR OUTPUT LEVELS TO BE −0.8V to −2.0V.
2. ALL SCOPE PROBES TO BE 10kΩ, 3pF, 300MHz BANDWIDTH.
3. SCOPE BANDWIDTH 300MHz.
4. FIXTURE REQUIRES GROUND PLANES.
5. SEE PARAGRAPH ON LAYOUT CONSIDERATIONS.

Figure 10. AD345 Test Setup