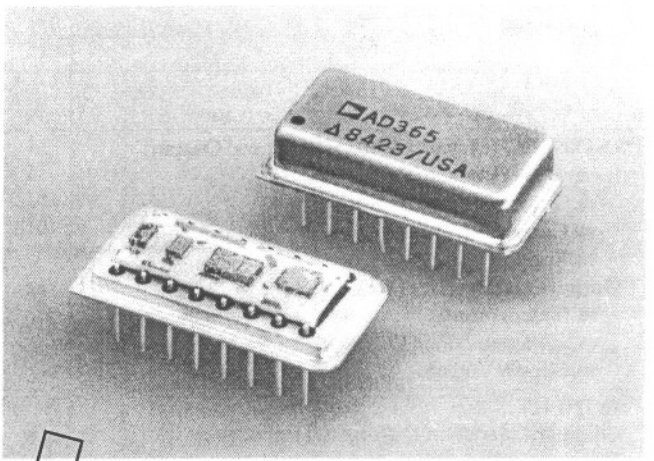
Programmable Gain & T/H DAS Amplifier

AD365

FEATURES
- Software Programmable Gain (1, 10, 100, 500)
- Low Input Noise (0.2μV p-p)
- Low Gain Error (0.05% max)
- Low Nonlinearity (0.005% max)
- Low Gain Drift (10ppm/°C max)
- Low Offset Drift (2μV/°C RTI max)
- Fast Settling (15μs @ Gain 100)
- Small 16-Pin Metal DIP

APPLICATIONS
- Digitally Controlled Gain Amplifier
- Auto-Gain Ranging Amplifier
- Wide Dynamic Range Measurement System
- Gain Selection/Channel Amplifier
- Transducer/Bridge Amplifier
- Test Equipment



HIGHLIGHTS

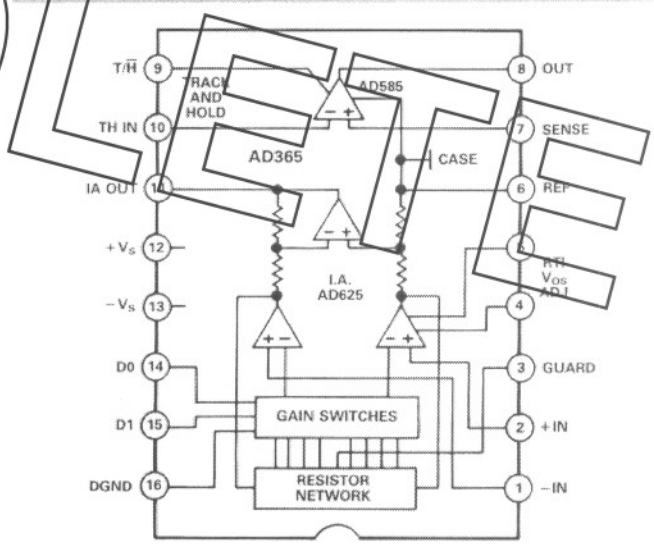
The AD365 is a two stage data acquisition system (DAS) front end consisting of a digitally selectable gain amplifier followed by an independent track/hold amplifier. The programmable gain amplifier features differential inputs for excellent common-mode rejection, high open loop gain for superior linearity, and fast settling for use in multiplexed high speed systems. The track/hold amplifier features high open loop gain for 12-bit compatible linearity, internal hold capacitor for high reliability, and fast acquisition time for use with multichannel systems. Both amplifiers are capable of being used separately and are specified as independent function blocks.

GENERAL DESCRIPTION

The AD365 is comprised of the AD625 monolithic precision instrumentation amplifier to provide a precision differential input, the AD7502 monolithic CMOS multiplexer to handle gain switching, a precision thin-film resistor network, and the AD585 monolithic track and hold amplifier with internal hold capacitor.

The input stage provides high common-mode rejection, low noise, fast settling at all gains, and low drift over temperature. The gains of 1, 10, 100, and 500 are digitally selected with the two gain control lines which are 5V CMOS compatible.

The track and hold amplifier section is ideally suited for high speed 12-bit applications where fast settling, low noise, and low sample-to-hold offset are critical. The T/H mode is controlled with a single input line which can be tied to the status output line of the accompanying A/D converter.



AD365 Functional Diagram

ORDERING INFORMATION

Model	Temperature Range	Price (100's)
AD365AM	−25°C to +85°C	$61.95

Two Technology Way; Norwood, MA 02062-9106 U.S.A.
Tel: 617/329-4700 **Twx: 710/394-6577**
Telex: 174059 **Cables: ANALOG NORWOODMASS**

SPECIFICATIONS (typical @ V_S = ±15V, R_L = 2kΩ and T_A = +25°C unless otherwise specified)

AD365AM	Min	Typ	Max	Units
PGA GAIN				
Inaccuracy[1]				
@ G = 1, 10, 100		0.02	0.05	%
@ G = 500		0.04	0.1	%
Nonlinearity				
@ G = 1, 10, 100			0.005	%
@ G = 500			0.01	%
Drift				
@ G = 1		1	5	ppm/°C
@ G = 10, 100, 500		3	10	ppm/°C
PGA OFFSET (May be Nulled at Input and Output)				
Input Offset Voltage (RTI)		25	200	µV
vs. Temperature		0.1	2	µV/°C
vs. Common-Mode Voltage		0.5	3.2	µV/V
vs. Supply Voltage		1	10	µV/V
Output Offset Voltage (RTO)		1	5	mV
vs. Temperature		30	150	µV/°C
vs. Common-Mode Voltage		60	316	µV/V
vs. Supply Voltage		60	316	µV/V
PGA INPUT				
Common-Mode and Differential Impedance		$10^9 \| 5$		Ω||pF
Differential Input Voltage, Linear	10	12		V
Common-Mode Voltage, Linear		$12 - V_{DIFF} \times G/2$		V
Input Stage Noise 0.1 to 10Hz		0.2		µV p-p
Input Stage Noise Density @ 1kHz		4		nV/√Hz
Bias Current		5	50	nA
vs. Temperature		50		pA/°C
Offset Current		2	20	nA
vs. Temperature		20		pA/°C
Noise Current (0.1 to 10Hz)		60		pA p-p
PGA OUTPUT				
Voltage 2kΩLoad	10	12		V
Output Impedance		0.2		Ω
Short Circuit Current		25		mA
Capacitive Load		500		pF
Output Stage Noise 0.1 to 10Hz		10		µV p-p
Output Stage Noise Density @ 1kHz		75		nV/√Hz
Guard Voltage		$(V_{+IN} + V_{-IN})/2$		V
Guard Offset		−550		mV
PGA DYNAMIC RESPONSE				
Small Signal −3dB				
G = 1		800		kHz
G = 10		400		kHz
G = 100		150		kHz
G = 500		40		kHz
Full Power Bandwidth G = 1 @ V_O = 20V p-p		60		kHz
Slew Rate		4		V/µs
Settling Time to 0.01% @ V_O = 20V p-p				
G = 1, 10		8	10	µs
G = 100		12	15	µs
G = 500		40	50	µs
Gain Switching Time		1.5		µs
Overdrive Recovery Time V_{IN} = 15V @ G = 1		7		µs
PGA DIGITAL INPUTS				
Logic Low	0		0.8	V
Logic High	3.0		$+V_S$	V
Current, I_{INH} or I_{INL}		0.01	1	µA

AD365AM	Min	Typ	Max	Units
TRACK AND HOLD AMPLIFIER SECTION				
TRANSFER CHARACTERISTICS				
Open Loop Gain $V_O = 10V$, $R_L = 2k$	100k	200k		V/V
Nonlinearity @ G = +1			0.005	% FSR
Output Voltage $R_L = 2k\Omega$	10	12		V
Capacitive Load		100		pF
Short Circuit Current		25		mA
TRACK MODE DYNAMICS				
Acquisition Time to 0.01% 10V Step		2	3	µs
20V Step		4	5	µs
Small Signal Bandwidth −3dB		2		MHz
Full Power Bandwidth (20V p-p)		120		kHz
Slew Rate		10		V/µs
TRACK/HOLD SWITCHING				
Aperture Time		35		ns
Aperture Uncertainty		0.5		ns
Switching Transient		40		mV
Settling Time to 2mV		0.5		µs
HOLD MODE				
Droop Rate @ +25°C		0.3	1	V/sec
from $T_{AMBIENT}$ to T_{MAX}		Doubles/10°C		V/sec
Feedthrough		25		µV/V
Pedestal, Offset @ +25°C		2	3	mV
Over Temperature		3		mV
T/H ANALOG INPUT				
Bias Current		0.1	2	nA
Over Temperature		0.2	5	nA
Offset Voltage			2	mV
Over Temperature			3	mV
vs. Common Mode		25	100	µV/V
vs. Supplies		100	316	µV/V
Input Impedance		$10^{12}\|\|10$		Ω||pF
Noise Density @ 1kHz		50		$nV/\sqrt{Hz}$
Noise 0.1Hz to 10Hz		10		µV p-p
T/H DIGITAL INPUT CHARACTERISTICS				
Logic Low (Hold Mode)	0		0.8	V
Logic High (Track Mode)	2.0		$+V_S$	V
Input Current		10	50	µA
AD365 POWER REQUIREMENTS				
Positive Supply Range	+11		+17	V
Negative Supply Range	−11		−17	V
Quiescent Current		12	16	mA
Power Dissipation		360	550	mW
Warm-Up Time to Specification		5		Minutes
Ambient Operating Temperature	−25		+85	°C
Package Thermal Resistance (θ_{ja})		60		°C/W
AD365 ABSOLUTE MAXIMUM RATINGS				
Positive Supply $+V_S$	−0.3		+17	V dc
Negative Supply $-V_S$	+0.3		−17	V dc
Analog Input Voltage	$-V_S$		$+V_S$	V
Analog Input Current	−10		+10	mA
Digital Input Voltage	−0.3		$+V_S$	V
T/H Differential V_{IN}			±30	V
Storage Temperature	−65		+150	°C
Lead Soldering, 10 Sec			300	°C
Short Circuit Duration		Indefinite		

NOTE
[1]Gain = 10, 100 and 500 are trimmed and tested ratiometric to G = 1.

Specifications subject to change without notice.

TYPICAL CHARACTERISTICS (@ +25°unless otherwise noted)

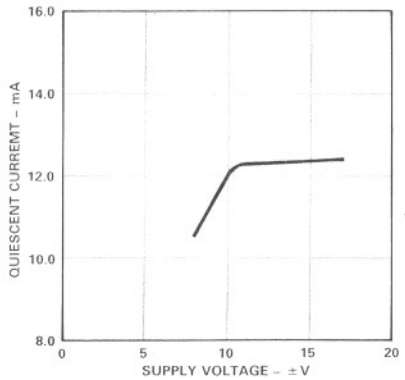


Figure 1. AD365 Quiescent Current vs. Supply Voltage

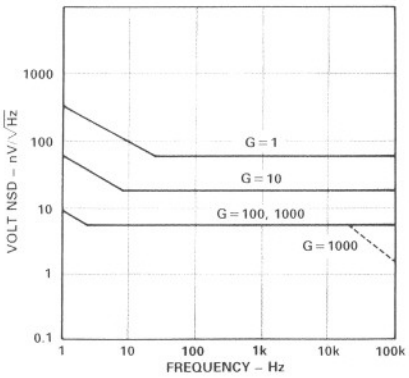


Figure 2. PGA RTI Noise Spectral Density vs. Gain

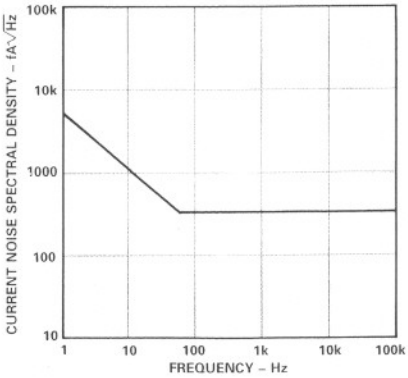


Figure 3. PGA Input Current Noise

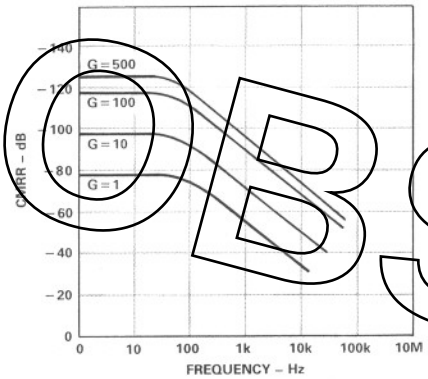


Figure 4. PGA CMRR vs. Frequency RTI, Zero to 1kΩ Source Imbalance

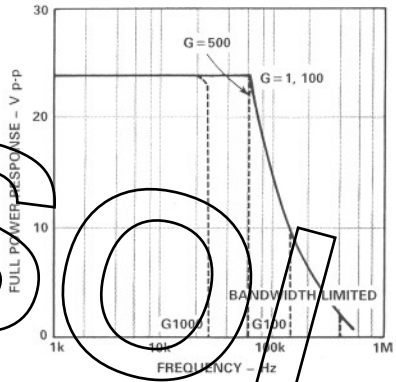


Figure 5. PGA Large Signal Frequency Response

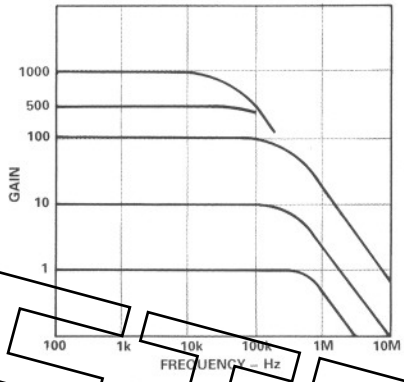


Figure 6. PGA Gain vs. Frequency

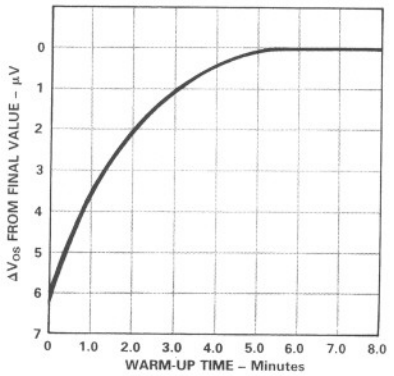


Figure 7. PGA Offset Voltage, RTI, Turn On Drift

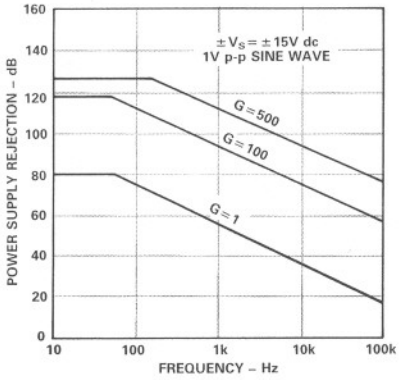


Figure 8. PGA PSRR vs. Frequency

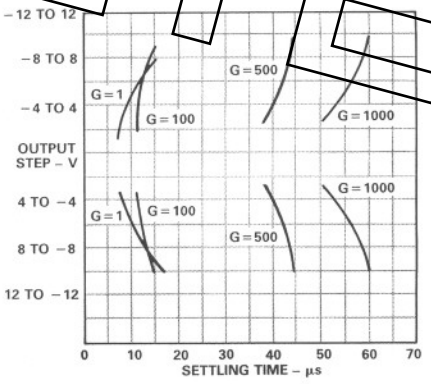


Figure 9. PGA Settling Time to 0.01%

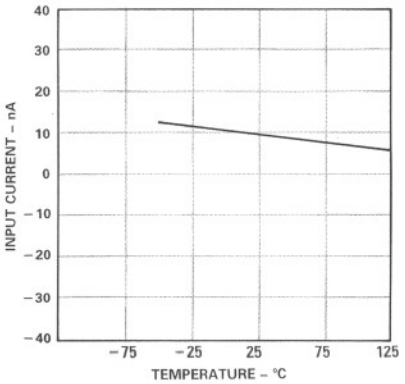


Figure 10. PGA Input Bias Current vs. Temperature

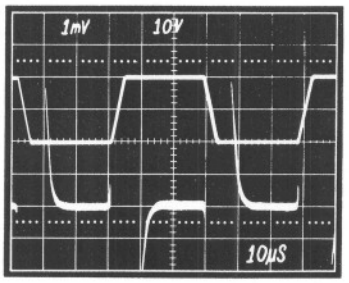


Figure 11. PGA Large Signal Pulse Response and Settling Time, G = 100

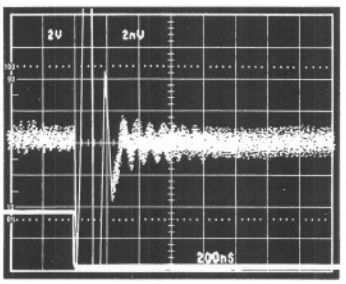


Figure 12. Sample-to-Hold Settling Time

The AD365 PGA section uses the AD625 monolithic instrumentation amplifier based on a modification of the classic three-op-amp approach. Monolithic construction and laser-wafer-trimming allow the tight matching and tracking of circuit components. This insures the high level of performance inherent in this circuit architecture.

A preamp stage (Q1-Q4) provides additional gain to A1 and A2. Feedback from the outputs of A1 and A2 forces the collector currents of Q1-Q4 to be constant, thereby, impressing the input voltage across R_G. This creates a differential voltage at the outputs of A1 and A2 which is given by the gain ($2R_F/R_G + 1$) times the differential portion of the input voltage. The unity gain subtractor, A3, removes any common-mode signal from the output voltage yielding a single ended output, V_{OUT}, referred to the potential at the reference pin.

Digital gain control is provided using the D0 and D1 inputs (pins 14 and 15) which are decoded internally in the gain switching AD7502 as shown in Figure 15 below. The switch selects the resistance R_G from the laser trimmed resistor network according to the following gain select table.

D1	D0	PGA GAIN
0	0	1
0	1	10
1	0	100
1	1	500

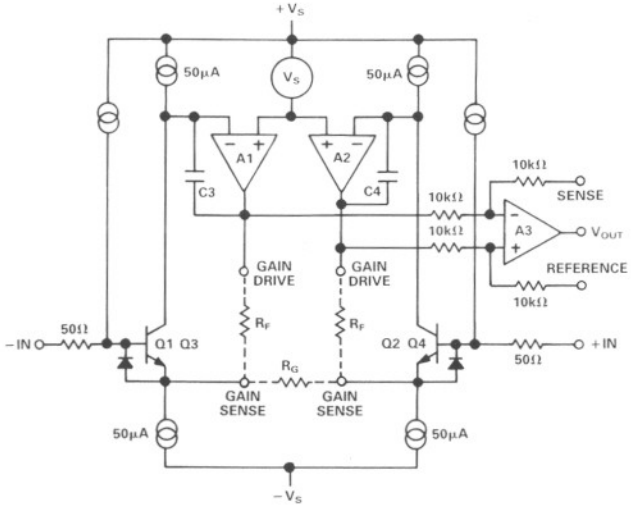


Figure 13. Simplified Circuit of the PGA

INPUT PROTECTION

Differential input amplifiers frequently encounter input voltages outside of their linear range of operation. There are two considerations when applying input protection for the PGA; 1) that continuous input current must be limited to less than 10mA and 2) that input voltages must not exceed either supply by more than one diode drop (approximately 0.6V @ 25°C).

Under differential overload conditions there is ($R_G + 300$)Ω in series with two diode drops (approximately 1.2V) between the plus and minus inputs, in either direction. With no external protection and R_G very small (i.e., 80Ω @ G = 500), the maximum overload voltage the PGA can withstand, continuously, is approximately ±5V. Figure 14 shows the external components

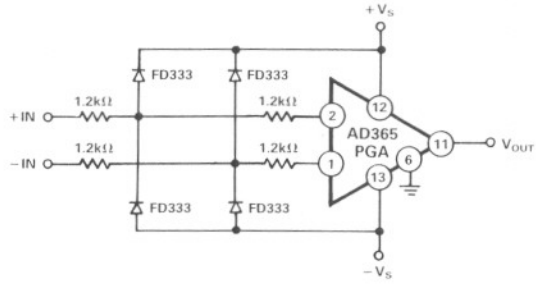


Figure 14. Input Protection Circuit for PGA

necessary to protect the PGA under all overload conditions at any gain. The diodes to the supplies are only necessary if input voltages outside of the range of the supplies are encountered.

REFERENCE TERMINAL

The reference terminal may be used to offset the output by up to ±2V. This is useful when the load is "floating" or does not share a ground with the rest of the system. It also provides a direct means of injecting a precise offset. It must be remembered, however, that the total output swing, to be shared between signal and reference offset, should be ±10 volts (from ground).

The PGA section reference terminal must be presented with nearly zero impedance. Any significant resistance, including those caused by PC layouts or other connection techniques, will increase the gain of the noninverting signal path, thereby, upsetting the common-mode rejection of the In-Amp. Inadvertent thermocouple connections created in the sense and reference lines should also be avoided as they will directly affect the output offset voltage and output offset voltage drift.

In the AD625, a reference source resistance will unbalance the CMR trim by the ratio of $10k\Omega/R_{REF}$. For example, if the reference source impedance is 1Ω, CMR will be reduced to 80dB ($10k\Omega/1\Omega$ = 80dB). An operational amplifier may be used to provide the low impedance reference point as shown in Figure 15. The input offset voltage characteristics of that amplifier will add directly to the output offset voltage performance of the instrumentation amplifier.

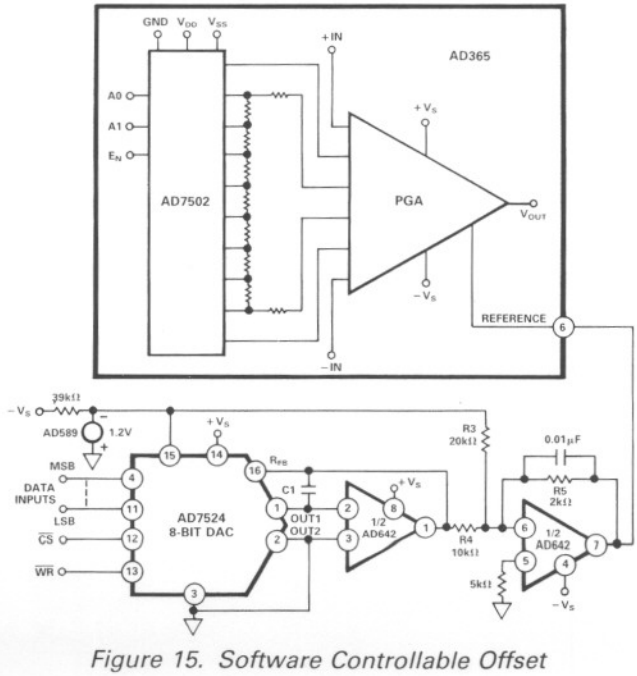


Figure 15. Software Controllable Offset

The circuit of Figure 15 also shows a CMOS DAC operating in the bipolar mode and connnected to the reference terminal to provide software controllable offset adjustments. The total offset range is equal to $\pm(V_{REF}/2 \times R_5/R_4)$. To be symmetrical about 0V, R_3 must be equal to $2 \times R_4$.

The offset per bit is equal to the total offset range divided by 2^N, where N = number of bits of the DAC. The range of offset for Figure 15 is ±120mV, and the offset is incremented in steps of 0.9375mV/LSB.

INPUT AND OUTPUT OFFSET VOLTAGE

Offset voltage specifications are often considered a figure of merit for instrumentation amplifiers. While initial offset may be adjusted to zero, shifts in offset voltage due to temperature variations will cause errors. Intelligent systems can often correct for this factor with an auto-zero cycle, but this requires extra circuitry.

Offset voltage and offset voltage drift each have two components: input and output. Input offset is that component of offset that is generated at the input stage. Measured at the output it is directly proportional to gain, i.e., input offset as measured at the output at G = 100 is 100 times greater than that measured at G = 1. Output offset is generated at the output and is constant for all gains. Input errors dominate at high gains and output errors dominate at low gains.

By separating these errors, one can evaluate the total error independent of the gain. For a given gain, both errors can be combined to give a total error referred to the input (RTI) or output (RTO) by the following formula:

Total Error RTI = input error + (output error/gain)

Total Error RTO = (Gain × input error) + output error

The AD365 provides for input offset voltage adjustment (see Figure 16). This simplifies nulling in very high precision applications and minimizes offset voltage effects in switched gain applications. In such applications the input offset is adjusted first at the highest programmed gain, then the output offset is adjusted at G = 1. If only a single null is desired, the input offset null should be used. The most additional drift when using only the input offset null is 0.9μV/°C, RTO.

Output offset adjustment is normally provided by the A/D converter offset adjustment which will compensate for the output offset of the PGA, offset of the T/H amplifier, and offset of the A/D.

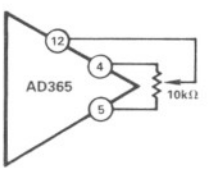


Figure 16. Input Voltage Offset Adjustment

COMMON-MODE REJECTION

In an instrumentation amplifier, degradation of common-mode rejection is caused by a differential phase shift due to differences in distributed stray capacitances. In many applications shielded cables are used to minimize noise. This technique can create common-mode rejection errors unless the shield is properly driven. Figure 17 shows active data guards which are configured to improve ac common-mode rejection by "bootstrapping" the capacitances of the input cabling, thus minimizing differential phase shift.

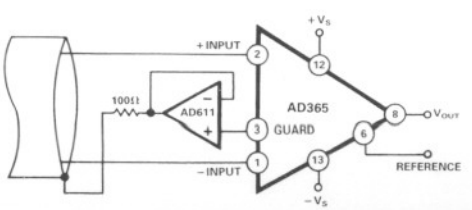


Figure 17. Common-Mode Shield Driver

GROUNDING

In order to isolate low level analog signals from a noisy digital environment, many data-acquisition components have two or more ground pins. These grounds must eventually be tied together at one point. It would be convenient to use a single ground line, however, current through ground wires and pc runs of the circuit card can cause hundreds of millivolts of error. Therefore, separate ground returns should be provided to minimize the current flow from the sensitive points to the system ground (see Figure 18). Since the AD365 output voltage is developed with respect to the potential on the reference terminal, it can solve many grounding problems.

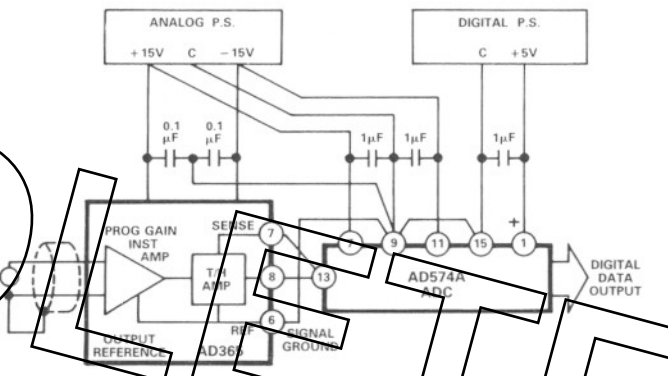


Figure 18. Basic Grounding Practice

GROUND RETURNS FOR BIAS CURRENTS

Input bias currents are those currents necessary to bias the input transistors of a dc amplifier. There must be a direct return path for these currents, otherwise they will charge external capacitances, causing the output to drift uncontrollably or saturate. Therefore, when amplifying "floating" input sources such as transformers, or ac-coupled sources, there must be a dc path from each input to ground as shown in Figure 19.

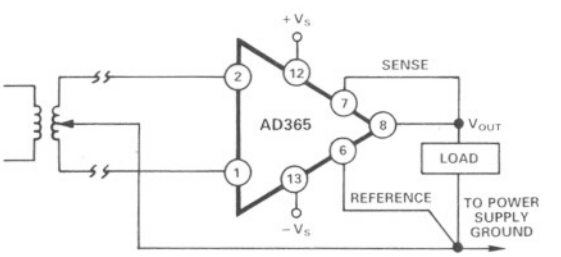


Figure 19a. Ground Returns for Bias Currents with Transformer Coupled Inputs

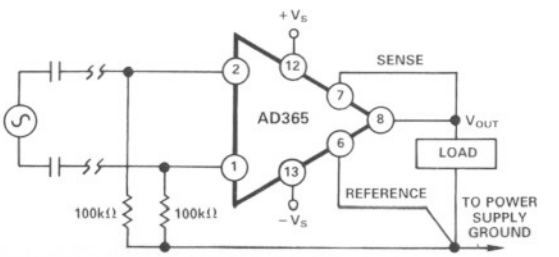


Figure 19b. Ground Returns for Bias Currents with ac Coupled Inputs

AUTO-ZERO CIRCUITS

In many applications it is necessary to maintain high accuracy. At room temperature, offset effects can be nulled by the use of offset trimpots. Over the operating temperature range, however, offset nulling becomes a problem. For these applications the auto-zero circuit of Figure 20 provides a hardware solution.

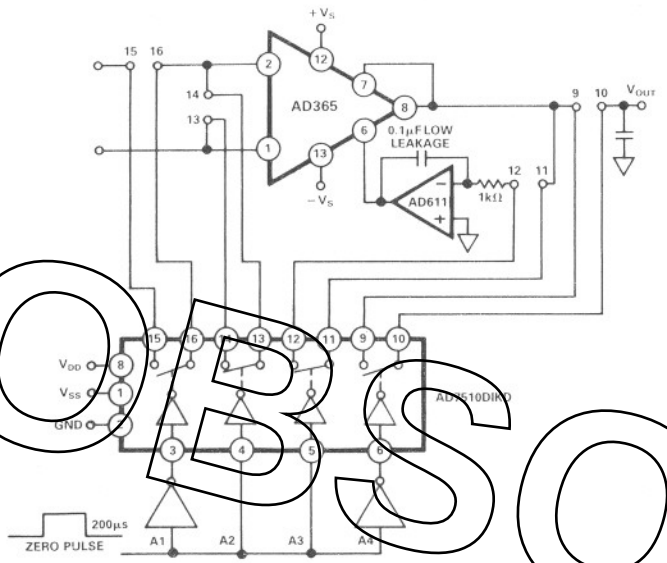


Figure 20. Auto-Zero Circuit

OTHER CONSIDERATIONS

One of the more overlooked problems in designing ultra-low-drift dc amplifiers is thermocouple induced offset. In a circuit comprised of two dissimilar conductors (i.e., copper, kovar), a current flows when the two junctions are at different temperatures. When this circuit is broken, a voltage known as the "Seebeck" or thermocouple emf can be measured. Standard IC lead material (kovar) and copper form a thermocouple with a high thermoelectric potential (about 35μV°C). This means that care must be taken to insure that all connections (especially those in the input circuit of the AD365) remain isothermal. This includes the input leads (1, 2). In addition, the user should also avoid air currents over the circuitry since slowly fluctuating thermocouple voltages will appear as "flicker" noise.

The base emitter junction of an input transistor can rectify out-of-band signals (i.e., RF interference). When amplifying small signals, these rectified voltages act as small dc offset errors. In the case of a resistive transducer, a capacitor across the input working against the internal resistance of the transducer may suffice to provide an RC filter. These capacitances may also be incorporated as part of the external input protection circuit (see section on input protection). As a general practice every effort should be made to match the extraneous capacitance at pins 1 and 2, to preserve high ac CMR.

THEORY OF OPERATION – T/H SECTION

In sampled data systems there are a number of limiting factors in digitizing high frequency signals accurately. Figure 21 shows pictorially the track-and-hold errors that are the limiting factors. In the following discussions of error sources the errors will be divided into the following groups: 1. Track-to-Hold Transition, 2. Hold Mode and 3. Hold-to-Track Transition.

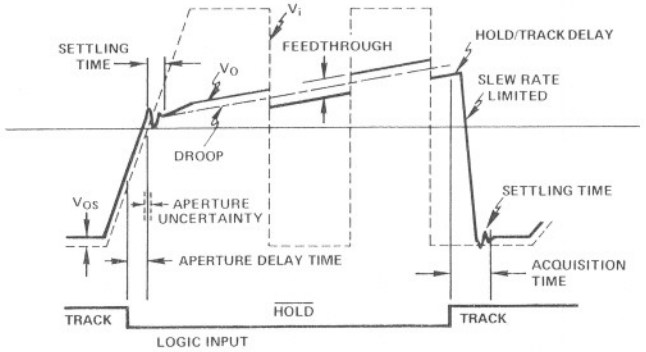


Figure 21. Pictorial Showing Various T/H Characteristics

TRACK-TO-HOLD TRANSITION

The aperture delay time is the time required for the track-and-hold amplifier to switch from track to hold. Since this is effectively a constant, it may be tuned out. If however, the aperture delay time is not accounted for then errors of the magnitude as shown in Figure 22 will result.

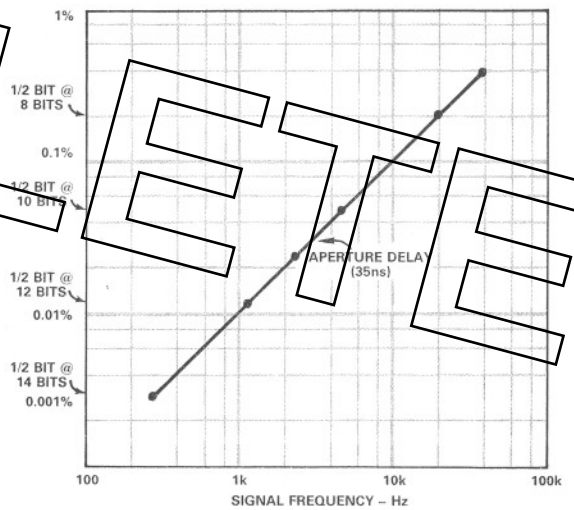


Figure 22. Aperture Delay Error vs. Frequency

To eliminate the aperture delay as an error source the track-to-hold command may be advanced with respect to the input signal.

Once the aperture delay time has been eliminated as an error source then T/H trigger uncertainty/jitter and internal aperture jitter which are the variations in aperture delay time from sample-to-sample remain. The aperture jitter is a true error source and must be considered. The aperture jitter is a result of noise within the switching network which modulates the phase of the hold command and is manifested in the variations in the value of the analog input that has been held. The aperture error which results from this jitter is directly related to the dV/dt of the analog input.

The error due to aperture jitter is easily calculated as shown below. The error calculation takes into account the desired accuracy corresponding to the resolution of the N-bit A/D converter.

$$F_{max} = \frac{2^{-(N+1)}}{\pi\ (\text{Aperture Jitter})}$$

For an application with a 12-bit A/D converter with a 10V full scale to a 1/2LSB error maximum:

$$F_{max} = \frac{2^{-(12+1)}}{\pi\,(0.5 \times 10^{-9})} = 77.7\text{kHz}$$

Track-to-hold offset is caused by the transfer of charge to the holding capacitor via the gate capacitance of the switch when switching into hold. Since the gate capacitance couples the switch-control voltage applied to the gate on to the hold capacitor, the resulting track-to-hold offset is a function of the logic level applied to the gate and the change in the gate capacitance over temperature.

HOLD MODE

In the hold mode there are two important specifications that must be considered; feedthrough and the droop rate. Feedthrough errors appear as an attenuated version of the input at the output while in the hold mode. Hold-Mode feedthrough varies with frequency, increasing at higher frequencies. Feedthrough is an important specification when a track and hold follows an analog multiplexer that switches among many different channels.

Hold-mode droop rate is the change in output voltage per unit of time while in the hold mode. Hold mode droop originates as leakage from the hold capacitor, of which the major leakage current contributors are switch leakage current and bias current. The rate of voltage change on the capacitor dV/dt is the ratio of the total leakage current I_L to the hold capacitance C_H.

$$\text{Droop Rate} = \frac{dV_{OUT}}{dt}\,(\text{Volts/Sec}) = \frac{I_L(\text{pA})}{C_H(\text{pF})}$$

For the AD365 in particular;

$$\text{Droop Rate} = \frac{100\text{pA}}{100\text{pF}} = 1\text{V/sec maximum}$$

Additionally the leakage current doubles for every 10°C increase in temperature above 25°C; therefore, the hold-mode droop rate characteristic will also double in the same fashion.

Since a track and hold is used typically in combination with an A/D converter, then the total droop in the output voltage has to be less than 1/2LSB during the period of a conversion. The maximum allowable signal change on the input of an A/D converter is:

$$\Delta V \text{ max} = \frac{\text{Full Scale Voltage}}{2^{(N+1)}}$$

Once the maximum ΔV is determined then the conversion time of the A/D converter (t_{CONV}) is required to calculate the maximum allowable dV/dt.

$$\frac{dV \text{ max}}{dt} = \frac{\Delta V \text{ max}}{t_{CONV}}$$

The maximum $\frac{dV \text{ max}}{dt}$ as shown by the previous equation is the limit not only at 25°C but at the maximum expected operating temperature range. Therefore, over the operating temperature range the following criteria must be met ($T_{OPERATION} - 25°C$) = ΔT.

$$\frac{dV\ 25°C}{dt} \times 2^{\frac{(\Delta T°C)}{10°C}} \leq \frac{dV \text{ max}}{dt}$$

HOLD-TO-TRACK TRANSITION

The Nyquist theorem states that a band-limited signal which is sampled at a rate at least twice the maximum signal frequency can be reconstructed without loss of information. This means that a sampled data system must sample, convert and acquire the next point at a rate at least twice the signal frequency. Thus the maximum input frequency is equal to

$$f_{MAX} = \frac{1}{2(T_{ACQ} + T_{CONV} + T_{AP})}$$

Where T_{ACQ} is the acquisition time of the sample-to-hold amplifier, T_{AP} is the maximum aperture time (small enough to be ignored) and T_{CONV} is the conversion time of the A/D converter.

DATA ACQUISITION SYSTEMS

The fast acquisition time of the AD365 when used with a high speed A/D converter allows accurate digitization of high frequency signals and high throughput rates in multichannel data acquisition systems. The AD365 can be used with a number of different A/D converters to achieve high throughput rates. Figures 23 and 24 show the use of an AD365 with the AD578 and AD574A.

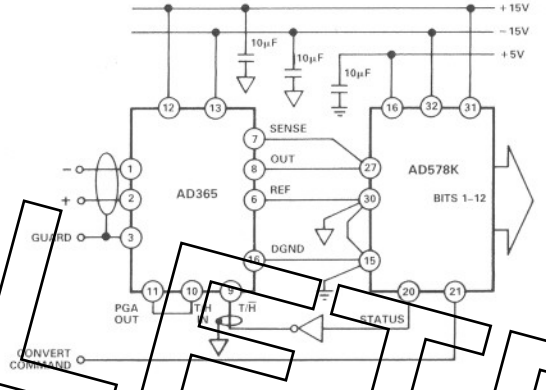


Figure 23. A/D Conversion System, 117.6kHz Throughput 58.8kHz Max Signal Input

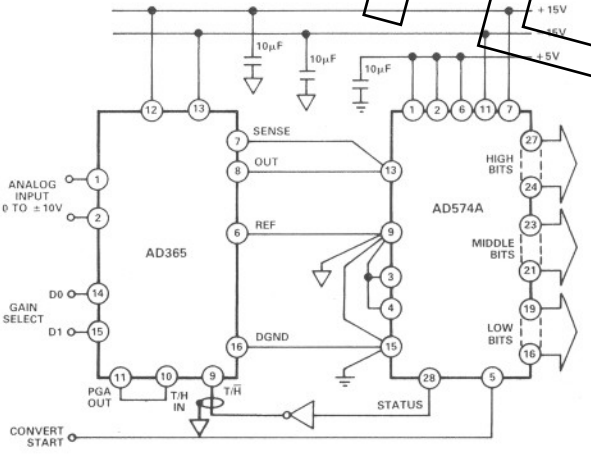
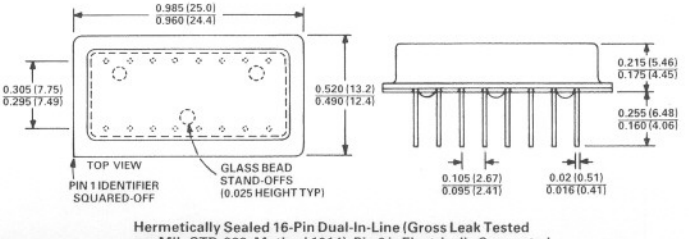


Figure 24. 12-Bit A/D Conversion System, 26.3kHz Throughput Rate, 13.1kHz Max Signal Input

PACKAGE DIMENSIONS

Dimensions shown in inches and (mm).

16-PIN DUAL-IN LINE METAL PACKAGE



Hermetically Sealed 16-Pin Dual-In-Line (Gross Leak Tested per MIL-STD-883, Method 1014). Pin 6 is Electrically Connected to the Case. Case Has Metal Bottom Surface.

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