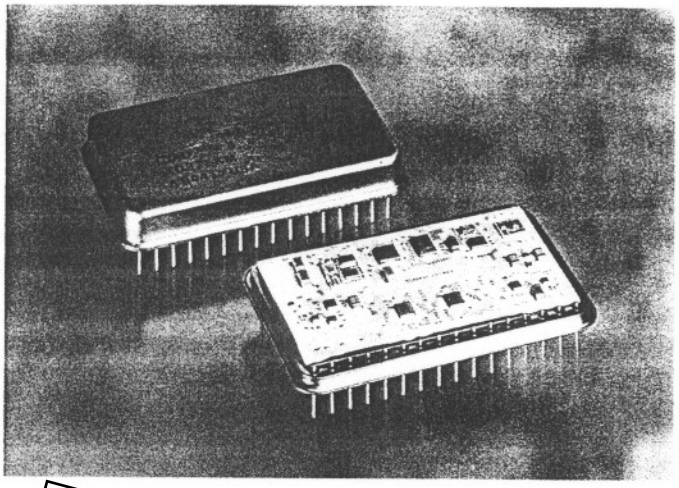
ANALOG DEVICES

Complete High Speed 16-Bit A/D Converter

AD376

FEATURES

- Complete 16-Bit Converter With Reference and Clock
- ±0.003% Maximum Nonlinearity
- No Missing Codes to 14 Bits
- Fast Conversion – 15μs (14 Bit)
- Short Cycle Capability
- Parallel Outputs
- Low Power: 1100mW Typical
- Industry Standard Pin Out



PRODUCT DESCRIPTION

The AD376 is a high resolution 16-bit hybrid IC analog-to-digital converter including reference, clock, and laser-trimmed thin-film components. The package is a compact 32-pin metal DIP. The thin-film scaling resistors allow analog input ranges of ±2.5V, ±5V, ±10V, 0 to +5V, 0 to +10V, and 0 to +20V.

Important performance characteristics of the devices are maximum linearity error of ±0.003% of FSR AD376KM, and maximum 14-bit conversion time of 15μs. This performance is due to innovative design and the use of proprietary monolithic D/A converter chips. Laser-trimmed thin-film resistors provide the linearity and wide temperature range for no missing codes.

The AD376 provides data in parallel form with corresponding clock and status outputs. All digital inputs and outputs are TTL compatible.

APPLICATIONS

The AD376 is excellent for use in applications requiring 14-bit accuracy over extended temperature ranges. Typical applications include medical and analytic instrumentation, precision measurement for industrial robots, automatic test equipment (ATE), multi-channel data acquisition systems, servo control systems and anywhere that excellent stability and wide dynamic range in the smallest space is required.

PRODUCT HIGHLIGHTS

1. The AD376 provides 16-bit resolution with maximum linearity error less than ±0.003% (±0.006% for J grade) at 25°C.
2. Conversion time is 14.5μs typical to 14 bits with short cycle capability.
3. Two binary codes are available on the AD376 output. They are complementary straight binary (CSB) for unipolar input voltage ranges and complementary offset binary (COB) for bipolar input ranges. Complementary two's complement (CTC) coding may be obtained by inverting pin 1 (MSB).
4. The proprietary chips used in this hybrid design provide excellent stability over temperature and lower chip count for improved reliability.

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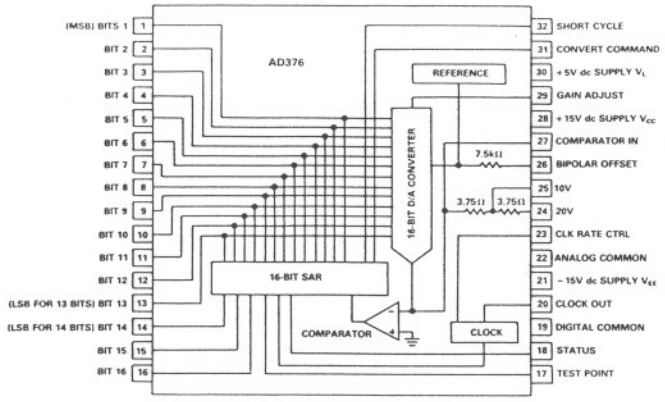
SPECIFICATIONS (typical at T_A = +25°C, V_S = ±15, +5 volts unless otherwise noted)

Model	AD376JM	AD376KM	Units
RESOLUTION	16 (max)	*	Bits
ANALOG INPUTS			
Voltage Ranges			
Bipolar	±2.5, ±5, ±10	*	Volts
Unipolar	0 to +5, 0 to +10, 0 to +20	*	Volts
Impedance (Direct Input)			
0 to +5V, ±2.5V	1.88	*	kΩ
0 to +10V, ±5.0V	3.75	*	kΩ
0 to +20V, ±10V	7.50	*	kΩ
DIGITAL INPUTS[1]			
Convert Command	Positive Pulse 50ns Wide (min) Trailing Edge Initiates Conversion		
Logic Loading	1	*	LS TTL Load
TRANSFER CHARACTERISTICS[2]			
ACCURACY			
Gain Error	±0.05[3] (±0.2 max)	*	%
Offset Error			
Unipolar	±0.05[3] (±0.1 max)	*	% of FSR[4]
Bipolar	±0.05[3] (±0.2 max)	*	% of FSR
Linearity Error (max)	±0.006 (J)	±0.003 (K)	% of FSR
Inherent Quantization Error	±1/2	*	LSB
Differential Linearity Error	±0.003	*	% of FSR
3σ Noise at Transitions (pk-pk)	0.001 (0.003 max)[7]	*	% of FSR
POWER SUPPLY SENSITIVITY			
±15V dc (±1V)	0.001	*	% of FSR/% ΔV_S
+5V dc (±0.25V)	0.001	*	% of FSR/% ΔV_S
CONVERSION TIME[6]			
12 Bits	12.5 (13 max)	*	µs
14 Bits	14.5 (15 max)	*	µs
16 Bits	16.5 (17 max)	*	µs
WARM-UP TIME	1 minute	*	Minutes
DRIFT[7]			
Gain	±15 (max)	±5 (±15 max)	ppm/°C
Offset			
Unipolar	±2 (±4 max)	±1 (±2 max)	ppm of FSR/°C
Bipolar	±10 (max)	±3 (±10 max)	ppm of FSR/°C
Linearity	±2 (3 max)	±0.3 (2 max)	ppm of FSR/°C
Guaranteed No Missing Code			
Temperature Range[8]	0 to 70 (13 bits)	0 to 70 (14 bits)	°C
DIGITAL OUTPUT[1]			
(All Codes Complementary)			
Parallel			
Output Codes[9]			
Unipolar	CSB	*	
Bipolar	COB, CTC[10]	*	
Output Drive	2	*	LS TTL Loads
Status	Logic "1" During Conversion		
Status Output Drive	2 (max)	*	LS TTL Loads
Internal Clock[5]			
Clock Output Drive	2 (max)	*	LS TTL Loads
Frequency	933	*	kHz
POWER SUPPLY REQUIREMENTS			
Power Consumption	1100	*	mW
Rated Voltage, Analog	±15 ±0.5 (max)	*	V dc
Rated Voltage, Digital	+5 ±0.25 (max)	*	V dc
Supply Drain +15V dc	+30	*	mA
Supply Drain −15V dc	−23	*	mA
Supply Drain +5V dc	+55	*	mA
TEMPERATURE RANGE			
Specification	0 to +70	*	°C
Operating (Derated Specs)	−25 to +85	*	°C
Storage	−55 to +125	*	°C

NOTES
[1] Logic "0" = 0.8V, max. Logic "1" = 2.0V, min for inputs. For digital outputs Logic "0" = +0.4V max. Logic "1" = 2.4V min.
[2] Tested on ±10V and 0 to +10V ranges.
[3] Adjustable to zero.
[4] Full Scale Range.
[5] With pin 23, clock rate controls tied to digital ground.
[6] Conversion time may be shortened with "Short Cycle" set for lower resolution.
[7] Guaranteed but not 100% production tested.
[8] For definition of "No Missing Codes", refer to Theory of Operation.
[9] CSB – Complementary Straight Binary. COB – Complementary Offset Binary. CTC – Complementary Two's Complement.
[10] CTC coding obtained by inverting MSB (Pin 1).
*Specifications same as AD376JM.
Specifications subject to change without notice.

FUNCTIONAL BLOCK DIAGRAM



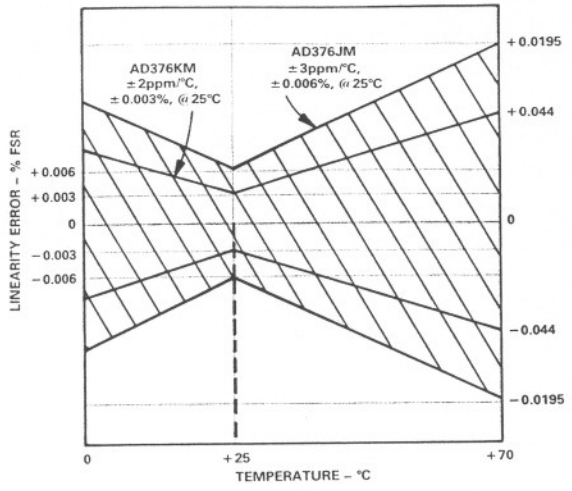
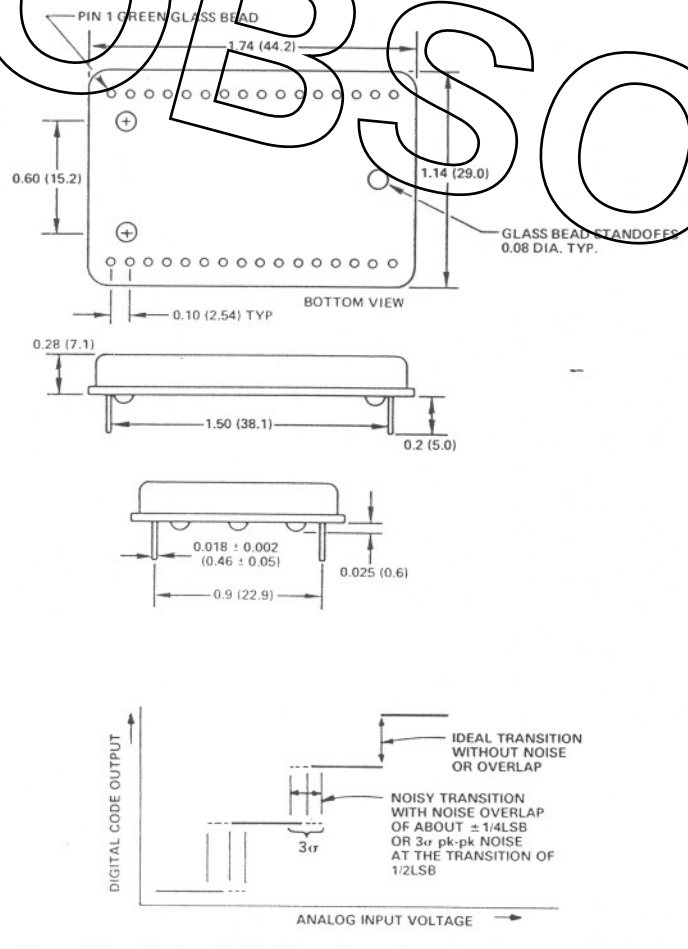


Figure 1. Linearity Error vs. Temperature

OUTLINE DIMENSIONS

(Dimensions shown in inches and (mm).



Transition Noise Definition Based on Dynamic Cross Plot

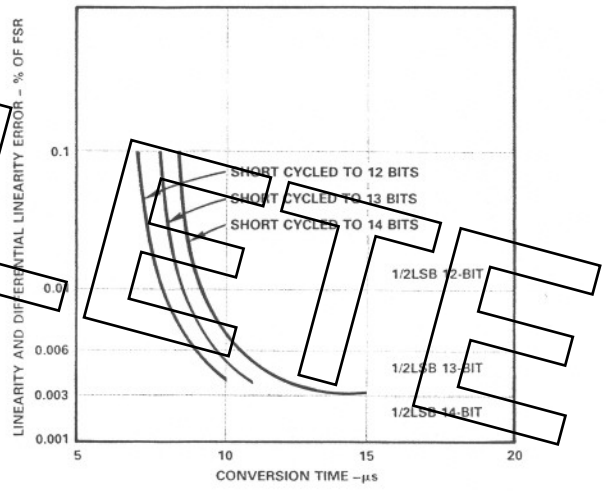


Figure 2. AD376 Nonlinearity vs. Conversion Time

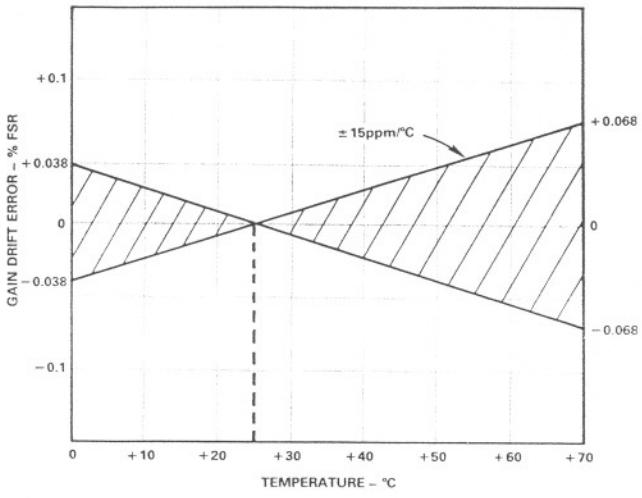


Figure 3. AD376 Gain Drift Error vs. Temperature

ORDERING GUIDE

Model	Max Linearity Error	Temperature Range	Price (100's)
AD376JM	0.006% FSR	0 to +70°C	$189.00
AD376KM	0.003% FSR	0 to +70°C	$219.50
AC1H72	Two 16-pin strip sockets		$6.00

THEORY OF OPERATION

The analog continuum is partitioned into 2^{16} discrete ranges for 16-bit conversion. All analog values within a given quantum are represented by the same digital code, usually assigned to the nominal midrange value. There is an inherent quantization uncertainty of $\pm 1/2$LSB, associated with the resolution, in addition to the actual conversion errors.

The actual conversion errors that are associated with A/D converters are combinations of analog errors due to the linear circuitry, matching and tracking properties of the ladder and scaling networks, reference error and power supply rejection. The matching and tracking errors in the converter have been minimized by the use of monolithic DACs that include the scaling network. The initial gain and offset errors are specified at $\pm 0.2\%$ FSR for gain and $\pm 0.1\%$ FSR for offset. These errors may be trimmed to zero by the use of external trim circuits as shown in Figures 5 and 7. Linearity error is defined for unipolar ranges as the deviation from a true straight line transfer characteristic from a zero voltage analog input, which calls for a zero digital output, to a point which is defined as a full scale. The linearity error is based on the DAC resistor ratios. It is unadjustable and is the most meaningful indication of A/D converter accuracy. Differential nonlinearity is a measure of the deviation in the staircase step width between codes from the ideal least significant bit step size (Figure 4).

Monotonic behavior requires that the differential linearity error be less than 1LSB, however a monotonic converter can have missing codes; the AD376 is specified as having no missing codes over temperature ranges as specified on the data page.

No Missing Code Definition for the AD376:
A code is defined as being present and not missing if it is at least 0.2LSB wide and not overlapped by the adjacent codes including their noise when viewed on a dynamic cross plot. For testing details, please refer to the "ADC Testing" section in "Analog-Digital Conversion Notes", by Dan Sheingold, Analog Devices, Inc., 1977, Pages 211 through 215.

There are three types of drift error over temperature: offset, gain and linearity. Offset drift causes a shift of the transfer characteristic left or right on the diagram over the operating temperature range. Gain drift causes a rotation of the transfer characteristic about the zero for unipolar ranges or minus full scale point for bipolar ranges. The worst case accuracy drift is the summation of all three drift errors over temperature. Statistically, however, the drift error behaves as the root-sum-squared (RSS) and can be shown as:

$$RSS = \sqrt{\epsilon_G^2 + \epsilon_O^2 + \epsilon_L^2}$$

ϵ_G = Gain Drift Error (ppm/°C)
ϵ_O = Offset Drift Error (ppm of FSR/°C)
ϵ_L = Linearity Error (ppm of FSR/°C)

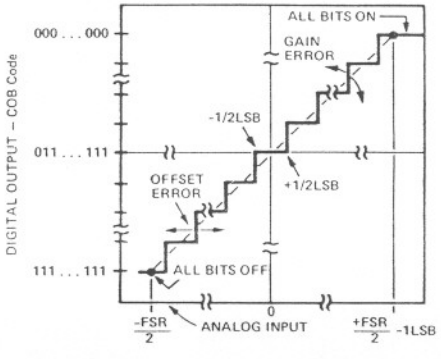


Figure 4. Transfer Characteristics for an Ideal Bipolar A/D

DESCRIPTION OF OPERATION

On receipt of a CONVERT START command, the AD376 converts the voltage at its analog input into an equivalent 16-bit binary number. This conversion is accomplished as follows: the 16-bit successive-approximation register (SAR) has its 16-bit outputs connected both to the device bit output pins and to the corresponding bit inputs of the feedback DAC. The analog input is successively compared to the feedback DAC output, one bit at a time (MSB first, LSB last). The decision to keep or reject each bit is then made at the completion of each bit comparison period, depending on the state of the comparator at that time.

TIMING

The timing diagram is shown in Figure 6. Receipt of a CONVERT START signal sets the STATUS flag, indicating conversion in progress. This, in turn, removes the inhibit applied to the gated clock, permitting it to run through 17 cycles. All the SAR parallel bits, STATUS flip-flops, and the gated clock inhibit signal are initialized on the trailing edge of the CONVERT START signal. At time t_0, B_1 is reset and $B_2 - B_{16}$ are set unconditionally. At t_1 the Bit 1 decision is made (keep) and Bit 2 is reset unconditionally. This sequence continues until the Bit 16 (LSB) decision (keep) is made at t_{16}. After a 40ns delay period, the STATUS flag is reset, indicating that the conversion is complete and that the parallel output data is valid. Resetting the STATUS flag restores the gated clock inhibit signal, forcing the clock output to the low Logic "0" state. Note that the clock remains low until the next conversion.

Corresponding parallel data bits become valid on the same positive-going clock edge.

Incorporation of this 40ns delay guarantees that the parallel data is valid at the Logic "1" to "0" transition of the STATUS flag, permitting parallel data transfer to be initiated by the trailing edge of the STATUS signal.

GAIN ADJUSTMENT

The gain adjust circuit consists of a 100ppm/°C potentiometer connected across $\pm V_S$ with its slider connected through a 300kΩ resistor to the gain adjust pin 29 as shown in Figure 5.

If no external trim adjustment is desired, pins 27 (offset adj) and pin 29 (gain adj) may be left open.

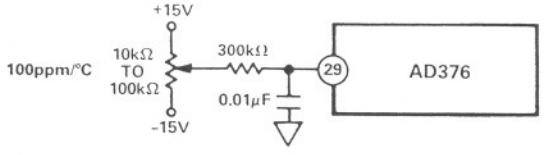


Figure 5. Gain Adjustment Circuit (±0.2% FSR)

OFFSET ADJUSTMENT

The zero adjust circuit consists of a 100ppm/°C potentiometer connected across $\pm V_S$ with its slider connected through a 1.8MΩ resistor to Comparator Input pin 27 for all ranges. As shown in Figure 7, the tolerance of this fixed resistor is not critical, and a carbon composition type is generally adequate. Using a carbon composition resistor having a −1200ppm/°C tempco contributes a worst-case offset tempco of $32LSB_{14} \times 61ppm/LSB_{14} \times 1200ppm/°C = 2.3ppm/°C$ of FSR, if the OFFSET ADJ potentiometer is set at either end of its adjustment range. Since the maximum offset adjustment required is typically no more than

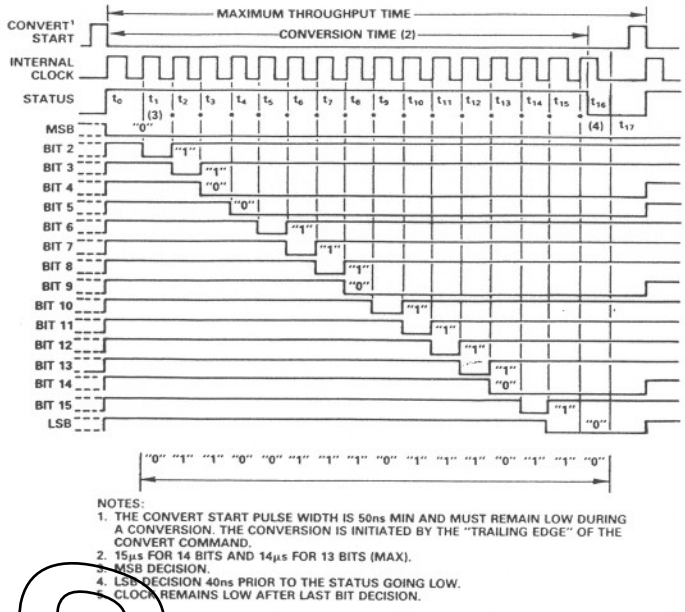


Figure 6. Timing Diagram (Binary Code 0110011101110110)

$\pm 16LSB_{14}$, use of a carbon composition offset summing resistor typically contributes no more than 1ppm/°C of FSR offset tempco.

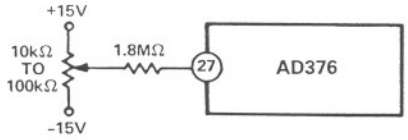


Figure 7. Offset Adjustment Circuit (±0.3% FSR)

An alternate offset adjust circuit, which contributes negligible offset tempco if metal film resistors (tempco <100ppm/°C) are used, is shown in Figure 8.

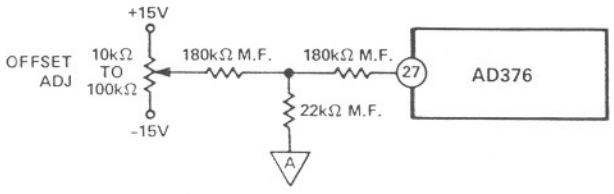


Figure 8. Low Tempco Zero Adjustment Circuit

In either adjust circuit, the fixed resistor connected to pin 27 should be located close to this pin to keep the pin connection runs short (Comparator Input pin 27 is quite sensitive to external noise pick-up and should be guarded by analog common).

DIGITAL OUTPUT DATA

Parallel data from TTL storage registers is in negative true form (Logic "1" = 0V and Logic "0" = 2.4V). Parallel data output coding is complementary binary for unipolar ranges and complementary offset binary for bipolar ranges. Parallel data becomes valid approximately 40ns before the STATUS flag returns to Logic "0", permitting parallel data transfer to be clocked on the "1" to "0" transition of the STATUS flag. Parallel data outputs change state on positive-going clock edges.

Short Cycle Input: A Short Cycle Input, pin 32, permits the timing cycle shown in Figure 6 to be terminated after any number of desired bits has been converted, permitting somewhat shorter conversion times in applications not requiring full 16-bit resolution. When 10-bit resolution is desired, pin 32 is connected to Bit 11 output pin 11. The conversion cycle then terminates and the STATUS flag resets after the Bit 10 decision (t_{10} + 40ns in timing diagram of Figure 6). Short cycle connections and associated 8-, 10-, 12-, 13-, 14-, and 15-bit conversion times are summarized in Table I, for a 933kHz clock.

Resolution		Maximum Conversion	Status Flag	Connect Short Cycle Pin 32 to
Bits	(%FSR)	Time (µs)	Reset	Pin:
16	0.0015	17.1	t_{16} + 40ns	N/C (Open)
15	0.003	16.1	t_{15} + 40ns	16
14	0.006	15.0	t_{14} + 40ns	15
13	0.012	13.9	t_{13} + 40ns	14
12	0.024	12.9	t_{12} + 40ns	13
10	0.100	10.7	t_{10} + 40ns	11
8	0.390	8.6	t_8 + 40ns	9

Table I. Short Cycle Connections

INPUT SCALING

The AD376 inputs should be scaled as close to the maximum input signal range as possible in order to utilize the maximum signal resolution of the A/D converter. Connect the input signal as shown in Table II. See Figure 9 for circuit details.

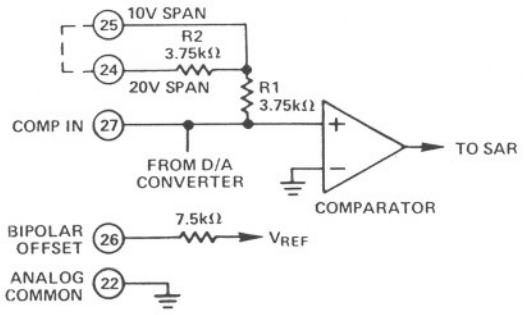


Figure 9. AD376 Input Scaling Circuit

Input Signal Line	Output Code	Connect Pin 26 to Pin	Connect Pin 24 to	For Direct Input, Connect Input Signal to
±10V	COB	27	Input Signal	24
±5V	COB	27	Open	25
±2.5V	COB	27	Pin 27	25
0V to +5V	CSB	22	Pin 27	25
0V to +10V	CSB	22	Open	25
0V to +20V	CSB	22	Input Signal	24

Note: Pin 27 is extremely sensitive to noise and should be guarded by analog common.

Table II. AD376 Input Scaling Connections

Transition Values MSB LSB	Range	±10V	±5V	±2.5V	0 to +10V	0 to +5V
000 . . . 000*	+ Full Scale	+10V −3/2LSB	+5V −3/2LSB	+2.5V −3/2LSB	+10V −3/2LSB	+5V −3/2LSB
011 . . . 111	Mid Scale	0	0	0	+5V	+2.5V
111 . . . 110	− Full Scale	−10V +1/2LSB	−5V +1/2LSB	−2.5V +1/2LSB	0V +1/2LSB	0V +1/2LSB

*Voltages given are the nominal value for transition to the code specified.
Note: For LSB value for range and resolution used, see Table IV.

Table III. Transition Values vs. Calibration Codes

Analog Input Voltage Range		±10V	±5V	±2.5V	0V to +10V	0V to +5V
Code Designation		COB* or CTC**	COB* or CTC**	COB* or CTC**	CSB***	CSB***
One Least Significant Bit (LSB)	$\frac{FSR}{2^n}$	$\frac{20V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$
	n = 8	78.13mV	39.06mV	19.53mV	39.06mV	19.53mV
	n = 10	19.53mV	9.77mV	4.88mV	9.77mV	4.88mV
	n = 12	4.88mV	2.44mV	1.22mV	2.44mV	1.22mV
	n = 13	2.44mV	1.22mV	0.61mV	1.22mV	0.61mV
	n = 14	1.22mV	0.61mV	0.31mV	0.61mV	0.31mV
	n = 15	0.61mV	0.31mV	0.15mV	0.31mV	0.15mV

NOTES
*COB = Complementary Offset Binary.
**CTC = Complementary Two's Complement – achieved by using an inverter to complement the most significant bit to produce $\overline{MSB}$.
***CSB = Complementary Straight Binary.

Table IV. Input Voltage Range and LSB Values

CALIBRATION (14-Bit Resolution Examples)

External ZERO ADJ and GAIN ADJ potentiometers, connected as shown in Figure 5 and 7, are used for device calibration. To prevent interaction of these two adjustments, Zero is always adjusted first and then Gain. Zero is adjusted with the analog input near the most negative end of the analog range (0 for unipolar and −FS for bipolar input ranges). Gain is adjusted with the analog input near the most positive end of the analog range.

0 to +10V Range: Set analog input to $+1LSB_{14} = 0.00061V$. Adjust Zero for digital output = 11111111111110. Zero is now calibrated. Set analog input to +FSR − 2LSB = +9.9987V. Adjust Gain for 00000000000001 digital output code; full-scale (Gain) is now calibrated. Half-scale calibration check: set analog input to +5.00000V; digital output code should be 01111111111111.

−10V to +10V Range: Set analog input to −9.99878V; adjust zero for 1111111111110 digital output (complementary offset

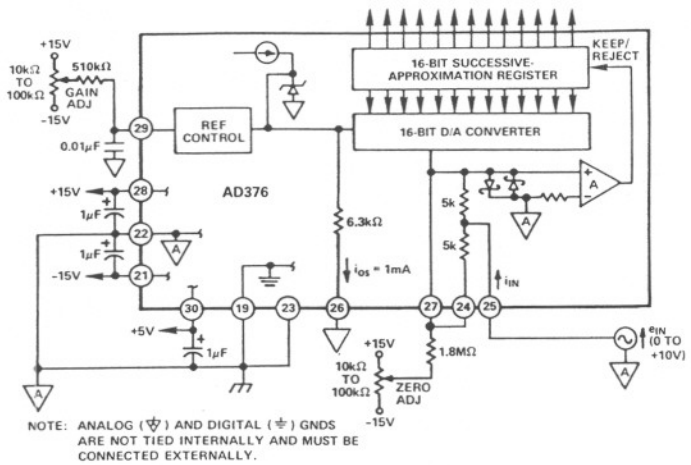


Figure 10. Analog and Power Connections for Unipolar 0 to +10V Input Range

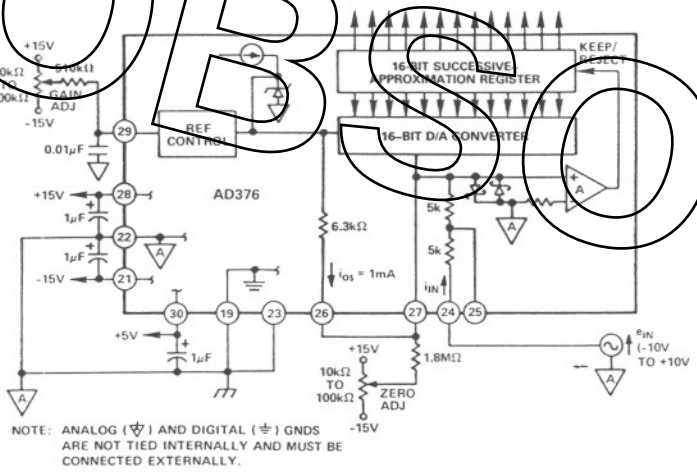


Figure 11. Analog and Power Connections for Bipolar +10V to +10V Input Range

binary) code. Set analog input to 9.99756V; adjust Gain for 00000000000001 digital output (complementary offset binary) code. Half-scale calibration check: set analog input to 0.00000V; digital output (complementary offset binary) code should be 01111111111111.

Other Ranges: Representative digital coding for 0 to +10V and −10V to +10V ranges is given above. Coding relationships and calibration points for 0 to +5V, −2.5V to +2.5V and −5V to +5V ranges can be found by halving proportionally the corresponding code equivalents listed for the 0 to +10V and −10V to +10V ranges, respectively, as indicated in Table III.

Zero and full-scale calibration can be accomplished to a precision of approximately ±1/2LSB using the static adjustment procedure described above. By summing a small sine or triangular wave voltage with the signal applied to the analog input, the output can be cycled through each of the calibration codes of interest to more accurately determine the center (or end points) of each discrete quantization level. A detailed description of this dynamic calibration technique is presented in "A/D Conversion Notes", D. Sheingold, Analog Devices, Inc., 1977, Part II, Chapter 4.

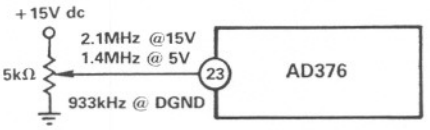


Figure 12. Clock Rate Control Circuit

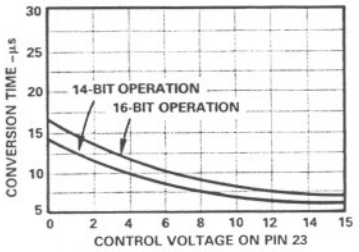


Figure 13. Converstion Time vs. Control Voltage

GROUNDING, DECOUPLING AND LAYOUT CONSIDERATIONS

Many data-acquisition components have two or more ground pins which are not connected together within the device. These "grounds" are usually referred to as the Logic Power Return, Analog Common (Analog Power Return) and Analog Signal Ground. These grounds (pins 19 and 22) must be tied together at one point for the AD376 as close as possible to the converter. Ideally, a single solid analog ground plane under the converter would be desirable. Current flows through the wires and etch stripes of the circuit cards, and since these paths have resistance and inductance, hundreds of millivolts can be generated between the system analog ground point and the ground pins of the AD376. Separate wide conductor stripe ground returns should be provided for high resolution converters to minimize noise and IR losses from the current flow in the path from the converter to the system ground point. In this way AD376 supply currents and other digital logic-gate return currents are not summed into the same return path as analog signals where they would cause measurement errors.

Each of the AD376 supply terminals should be capacitively decoupled as close to the AD376 as possible. A large value capacitor such as 1μF in parallel with a 0.1μF capacitor is usually sufficient. Analog supplies are to be bypassed to the Analog Power Return pin and the logic supply is bypassed to the Logic Power Return pin.

The metal case is internally grounded with respect to the power supplies, grounds and electrical signals. Do not externally ground the case. Glass beads standoff on the bottom will prevent shorting to board circuitry beneath the unit.

CLOCK RATE CONTROL

The AD376 may be operated at faster conversion times by connecting the Clock Rate Control (pin 23) to an external multiturn trim potentiometer (TCR <100ppm/°C) as shown in Figures 12 & 13. The integral linearity and differential linearity errors will vary with speed as shown in Figure 2.