AN-1417
APPLICATION NOTE

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Overvoltage Robustness Testing in the AD4110-1

by Dan O'Donnell and Brendan Somers

INTRODUCTION

The AD4110-1 is a complete, single-channel, universal input, analog-to-digital front end for industrial process control systems where sensor type flexibility is required.

The high voltage input is fully software configurable for current or voltage signals and allows a direct interface to all standard industrial analog signal sources, for example, ±20 mA, ±4 mA to ±20 mA, ±10 V, and all thermocouple types. Field power is supplied for loop powered, current output sensors. A range of excitation current sources for resistance temperature detectors (RTDs) and other resistive sensors are included. The integrated, fully differential, programmable gain amplifier (PGA) offers 16 gain settings from 0.2 to 24.

The high voltage input can be programmed to power up in either voltage mode or current mode. When programmed to current mode, the unique input circuit architecture provides a path for the loop current, even in the absence of the system power supply. For full details, see the AD4110-1 data sheet.

In some applications, an event can occur where the inputs of an analog input module are driven by voltages outside the level of the module power supply, known as an overvoltage condition. When an input pin goes more than one diode drop beyond the power supply rails, the internal diodes of the input amplifier can be forward-biased, causing excessive current to flow, which can damage the amplifier. This damage can result in a shift in the electrical specification parameters beyond the limits specified in the AD4110-1 data sheet, or cause the permanent failure of the input amplifier.

The AD4110-1 is designed on a high voltage silicon process and provides overvoltage protection of ±30 V dc on the input pins through the use of an external resistor-capacitor (RC) low-pass filter circuit. A diode is also required on the negative power supply.

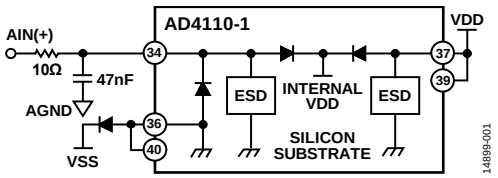

Figure 1. Analog Input Pin Structure

This application note outlines the test circuit configurations that confirm the data sheet specification for overvoltage protection. All possible operating modes of the AD4110-1 are tested. A socketed evaluation board was used for the test board, as shown in Figure 2. Refer to the AD4110-1 data sheet for details of the operating modes.

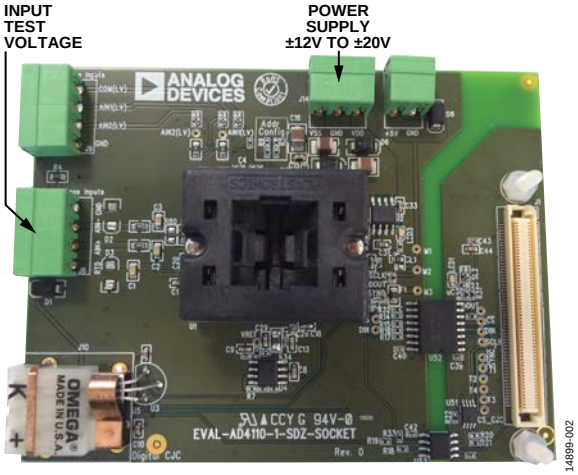

Figure 2. Test Board

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REVISION HISTORY

3/2019—Revision 0: Initial Version

TESTING SYSTEM AND METHOD

TEST SYSTEM

A socketed version of the EVAL-AD4110-1SDZ evaluation board (see Figure 2) is used as the test board for all test configurations. A Keysight® N6705B four-quadrant power supply analyzer supplies ±20 V to the test board for all test configurations except for the field power supply mode (FPSM) where ±15 V is used. A TTi® CPX200D power supply (current limited to 4 A) applies the overvoltage condition to the input terminals of the test board for all test configurations. For each test configuration, three devices were tested at three temperature points: −40°C, +25°C, and +105°C.

TEST METHOD

The test method is based on what can happen during a system installation where an analog input module is wired to a variety of industrial sensors when live system power cables are accessible. The possibility of connecting the system power supply to the module input terminals due to a miswiring condition was also tested. Typically, the system power supply is +24 V and can be specified with a tolerance of ±20%, giving a possible overvoltage range of ±19.2 V to ±28.8 V.

As shown in Figure 4 through Figure 35, the overvoltage condition is applied to the input terminals five times in quick succession and repeated for positive and negative voltages. For test configurations where the applied voltage is floating with respect to the test board ground, the source outputs are connected to the input terminals at the same time. For test configurations where the applied voltage is referenced to the test board ground, the test board RTD(−) terminal is connected first. The RTD(−) terminal is connected to the test board AGND via a 100 Ω resistor (see Figure 3).

After each AD4110-1 device is tested, the device production test program runs to ensure that no data sheet specifications have changed due to the result of the applied overvoltage condition. The AD4110-1 data sheet analog input overvoltage protection specification is determined from the worst case test result from all test configurations with a 2 V margin applied. Table 1 summarizes the test result.

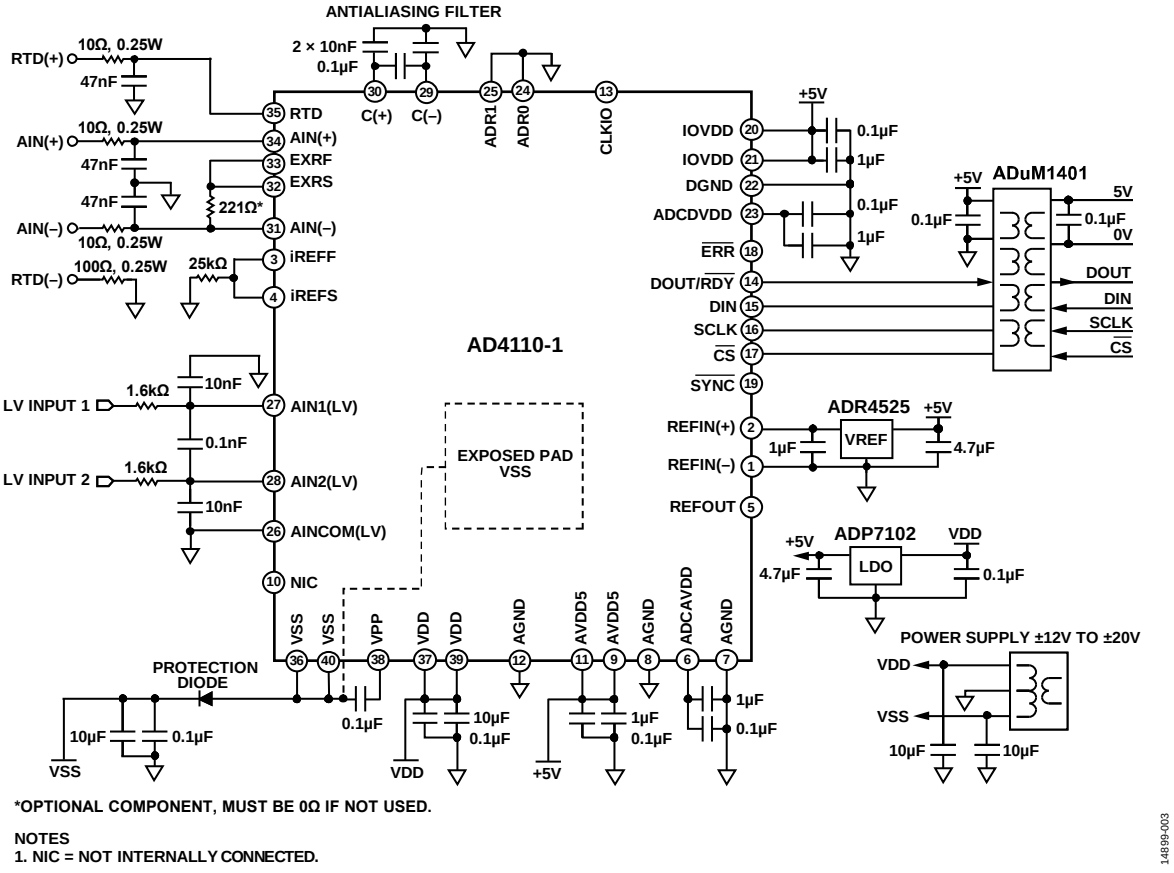

Figure 3. Test Board Schematic Diagram of EVAL-AD4110-1SDZ

RESULTS SUMMARY

The AD4110-1 data sheet specification for analog input overvoltage protection on the AIN(+) and AIN(−) pins, specified at ±30 V, is determined from the worst case test result from all test configurations and with a 2 V margin applied. The overall test results summary is outlined in Table 1. The pass level of the applied input voltage is the maximum overvoltage level at which the device meets the data sheet specifications after the test. See Figure 4 through Figure 35 for the test configuration diagrams and test results.

The lowest overvoltage condition applied where there was no deviation from the AD4110-1 specifications is 32 V, configured in field power supply mode, as shown in Table 1. Note that the power supply is limited to ±15 V is this configuration and is therefore not the worst-case condition.

The next lowest overvoltage condition applied where there was no deviation from the AD4110-1 specifications is −33 V, configured in 4-wire RTD mode. To verify this result, 30 additional devices in this configuration were tested, which allows the data sheet specification for overvoltage protection to be specified at ±30 V with a 3 V margin applied.

Table 1. Results Summary

	Pass Level of Applied Input Voltage (V)[1]			
Test Configuration/Mode	**RTD(+)**	**AIN(+)**	**AIN(−)**	**RTD(−)**
Voltage	Not applicable	+40, −35	+40, −40	Not applicable
Current	Not applicable	+40, −35	+40, −40	Not applicable
2-Wire RTD	Not applicable	+40, −35	+40, −40	Not applicable
3-Wire RTD	+40, −40	+40, −35	+40, −40	Not applicable
4-Wire RTD	+40, −40	+40, −33	+40, −40	Not applicable
Field Power Supply Mode[2]	Not applicable	+40, −35	+32	Not applicable
No Power Supply Mode	Not applicable	40	40	Not applicable

[1] The pass level of the applied input voltage is the maximum overvoltage level at which the device meets data sheet specifications after the test.
[2] The VDD or VSS power supply voltage is limited to ≤±15 V for this test configuration.

TEST RESULTS

VOLTAGE MODE

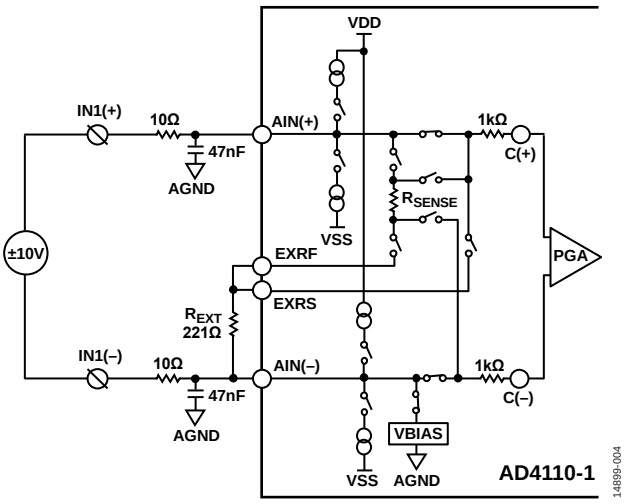

Figure 4. Typical Application Diagram—Voltage Mode

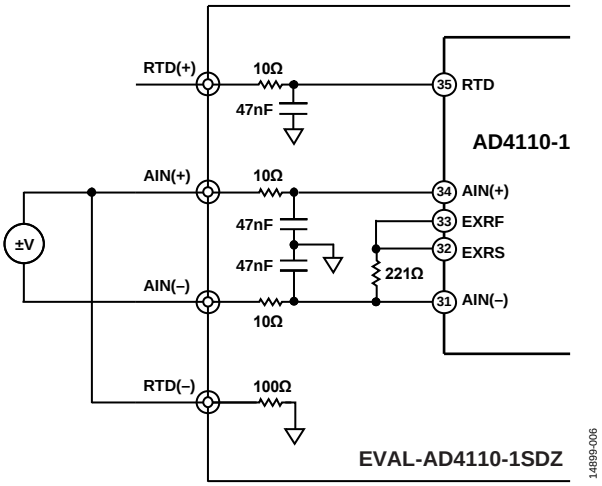

Figure 6. Voltage Mode, Test 3 and Test 4

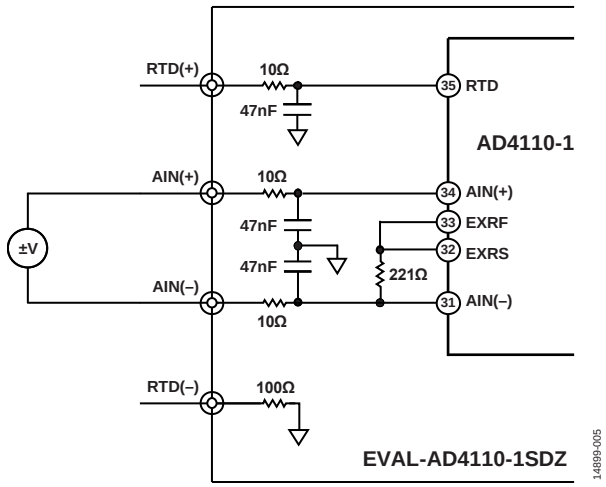

Figure 5. Voltage Mode, Test 1 and Test 2

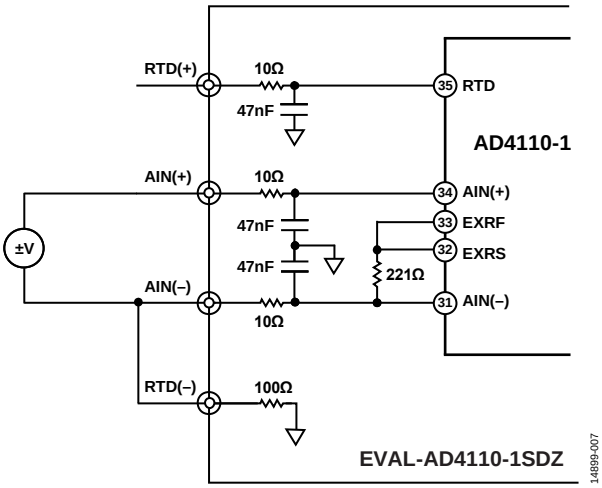

Figure 7. Voltage Mode, Test 5 and Test 6

Table 2. Test Results for Voltage Mode Configurations

		Pass Level of Applied Input Voltage (V)[1]			
Test Number	**Test Configuration**	**RTD(+)**	**AIN(+)**	**AIN(–)**	**RTD(–)**
Test 1	See Figure 5	No connect	40	0	No connect
Test 2	See Figure 5	No connect	0	40	No connect
Test 3	See Figure 6	No connect	0	−40	0
Test 4	See Figure 6	No connect	0	40	0
Test 5	See Figure 7	No connect	40	0	0
Test 6	See Figure 7	No connect	−35	0	0

[1] The pass level of the applied input voltage is the maximum overvoltage level at which the device meets data sheet specifications after the test.

CURRENT MODE

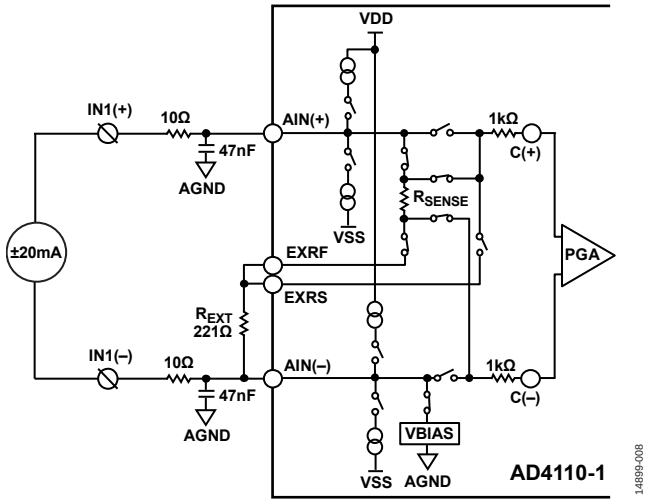

Figure 8. Typical Application Diagram—Current Mode

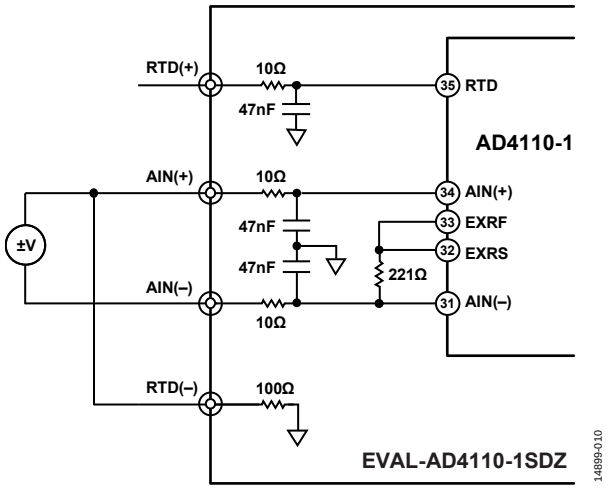

Figure 10. Current Mode, Test 3 and Test 4

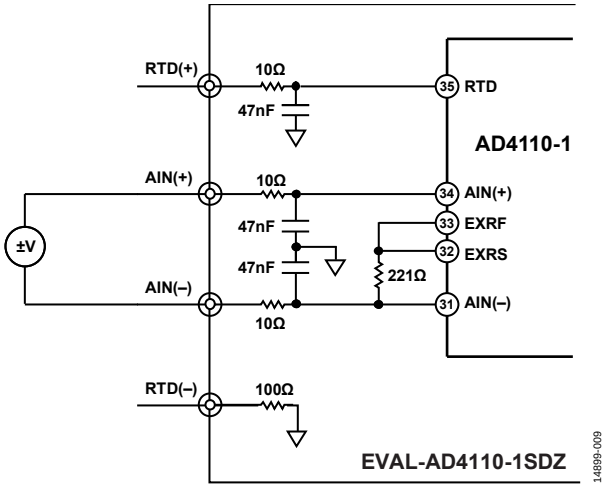

Figure 9. Current Mode, Test 1 and Test 2

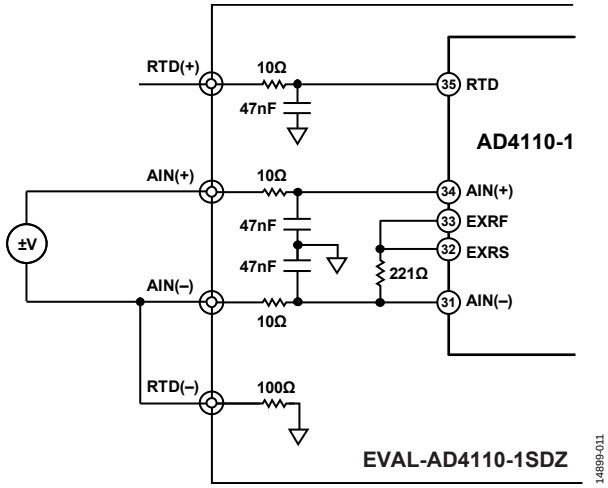

Figure 11. Current Mode, Test 5 and Test 6

Table 3. Test Results for Current Mode Configurations

		Pass Level of Applied Input Voltage (V)[1]			
Test Number	**Test Configuration**	**RTD(+)**	**AIN(+)**	**AIN(–)**	**RTD(–)**
Test 1	See Figure 9	No connect	40	0	No connect
Test 2	See Figure 9	No connect	0	40	No connect
Test 3	See Figure 10	No connect	0	−40	0
Test 4	See Figure 10	No connect	0	40	0
Test 5	See Figure 11	No connect	40	0	0
Test 6	See Figure 11	No connect	−35	0	0

[1] The pass level of the applied input voltage is the maximum overvoltage level at which the device meets data sheet specifications after the test.

2-WIRE RTD MODE

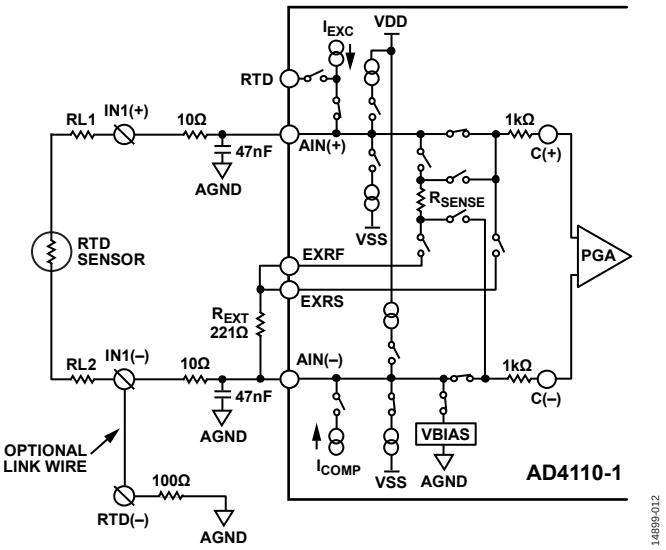

Figure 12. Typical Application Diagram—2-Wire RTD Mode

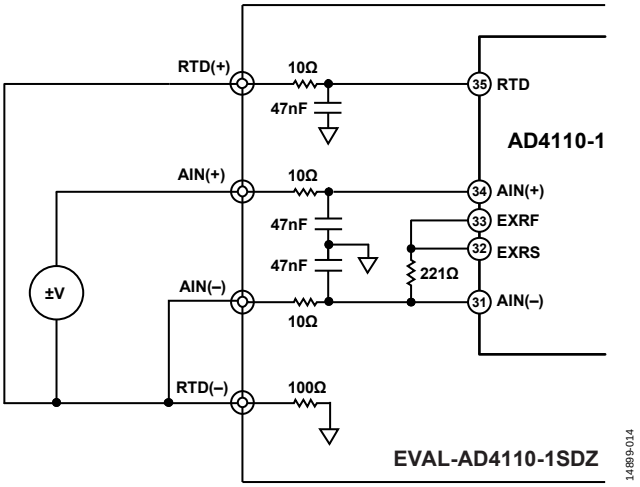

Figure 14. 2-Wire RTD Mode, Test 3 and Test 4

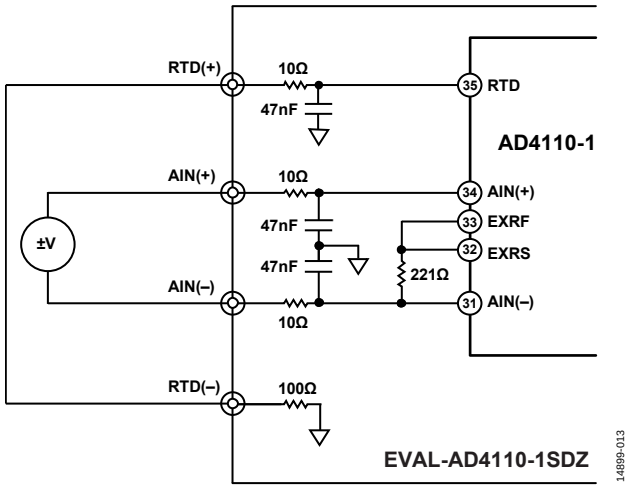

Figure 13. 2-Wire RTD Mode, Test 1 and Test 2

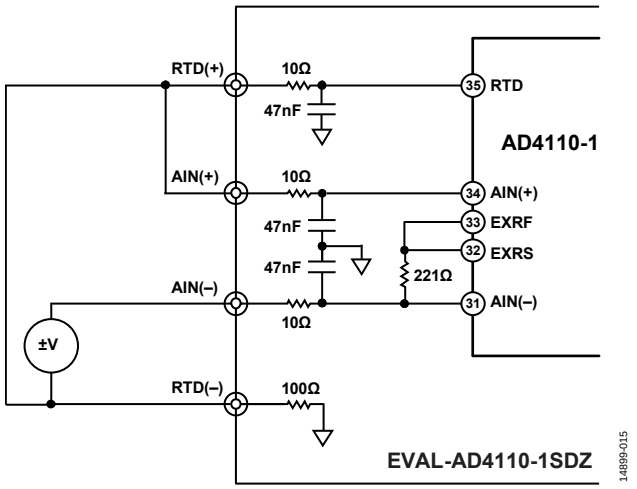

Figure 15. 2-Wire RTD Mode, Test 5 and Test 6

Table 4. Test Results for 2-Wire RTD Configurations

Test Number	Test Configuration	Pass Level of Applied Input Voltage (V)[1]			
		RTD(+)	AIN(+)	AIN(–)	RTD(–)
Test 1	See Figure 13	0	40	0	0
Test 2	See Figure 13	0	0	40	0
Test 3	See Figure 14	0	+40	0	0
Test 4	See Figure 14	0	−35	0	0
Test 5	See Figure 15	0	0	40	0
Test 6	See Figure 15	0	0	−40	0

[1] The pass level of the applied input voltage is the maximum overvoltage level at which the device meets data sheet specifications after the test.

3-WIRE RTD MODE

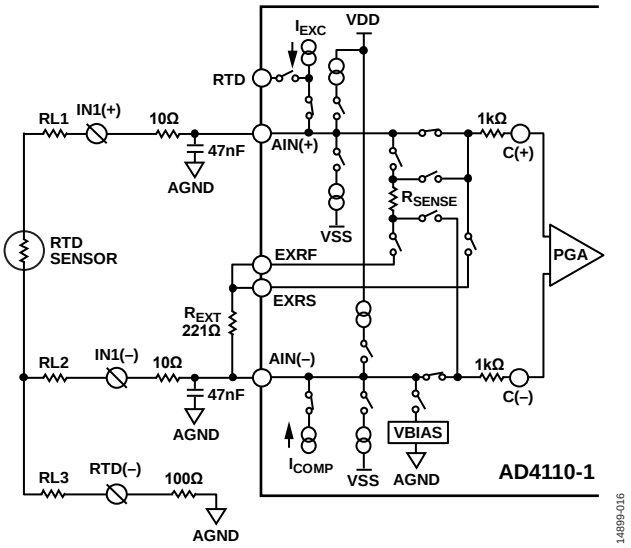

Figure 16. Typical Application Diagram—3-Wire RTD Mode

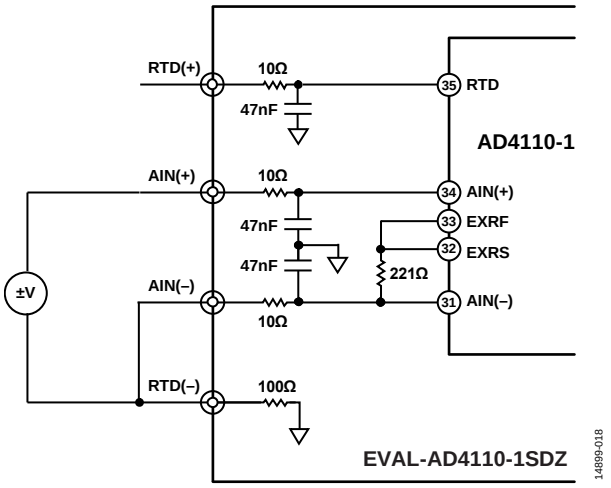

Figure 18. 3-Wire RTD Mode, Test 3 and Test 7

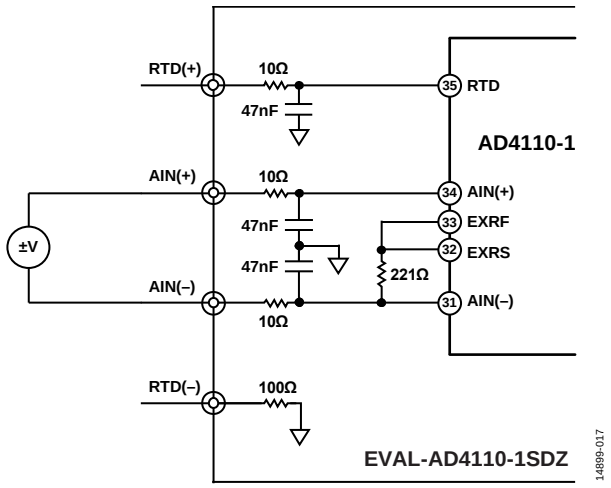

Figure 17. 3-Wire RTD Mode, Test 1 and Test 2

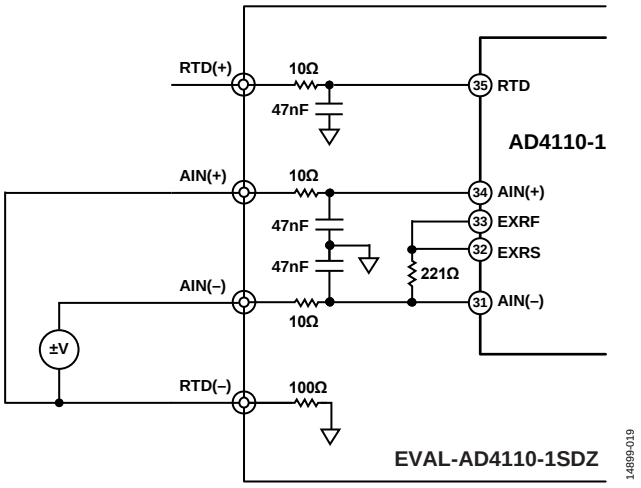

Figure 19. 3-Wire RTD Mode, Test 5 and Test 6

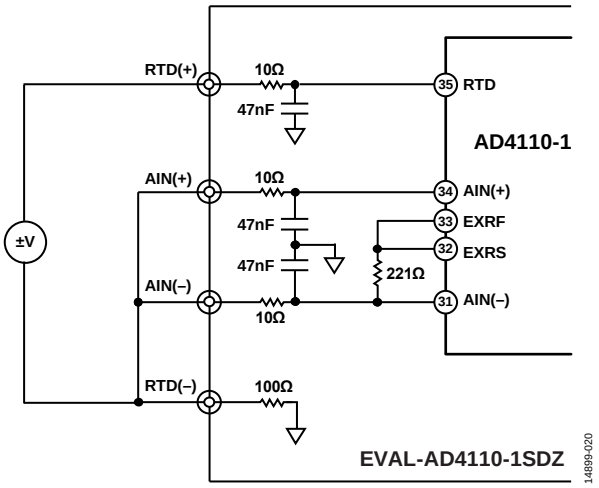

Figure 20. 3-Wire RTD Mode, Test 4 and Test 8

Table 5. Test Results for 3-Wire RTD Configurations

		Pass Level of Applied Input Voltage (V)[1]			
Test Number	**Test Configuration**	**RTD(+)**	**AIN(+)**	**AIN(–)**	**RTD(–)**
Test 1	See Figure 17	No connect	40	0	No connect
Test 2	See Figure 17	No connect	0	40	No connect
Test 3	See Figure 18	No connect	40	0	0
Test 4	See Figure 20	No connect	0	40	0
Test 5	See Figure 19	40	0	0	0
Test 6	See Figure 19	−40	0	0	0
Test 7	See Figure 18	No connect	−35	0	0
Test 8	See Figure 20	No connect	0	−40	0

[1] The pass level of the applied input voltage is the maximum overvoltage level at which the device meets data sheet specifications after the test.

4-WIRE RTD MODE

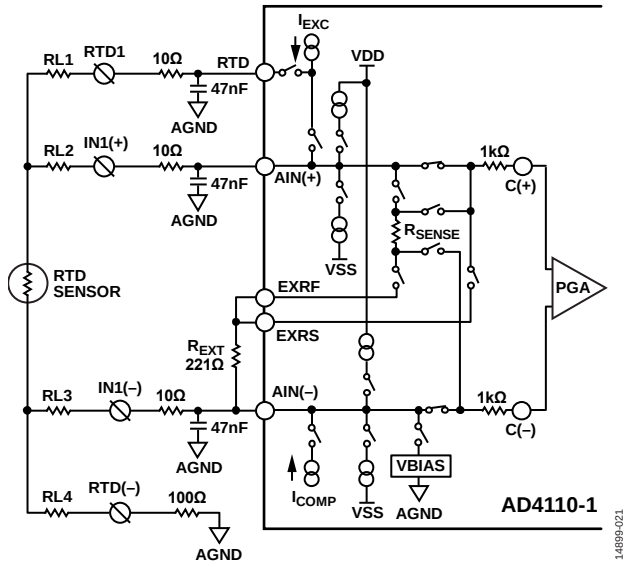

Figure 21. Typical Application Diagram—4-Wire RTD Mode

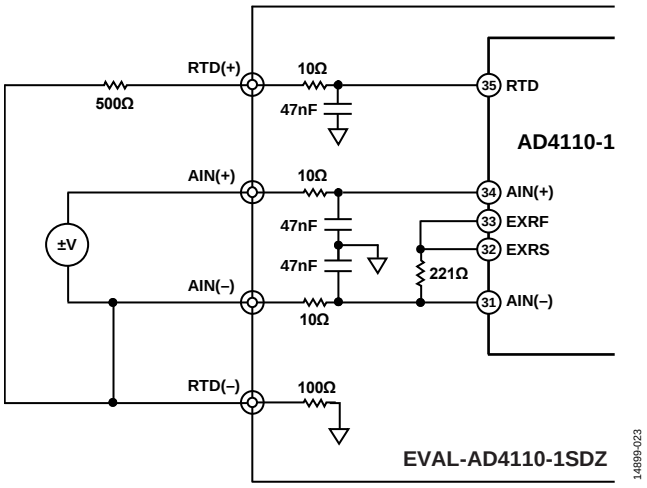

Figure 23. 4-Wire RTD Mode, Test 3 and Test 8

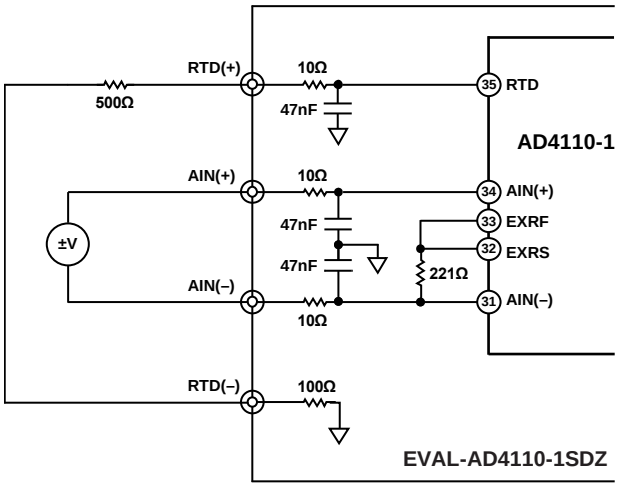

Figure 22. 4-Wire RTD Mode, Test 1 and Test 2

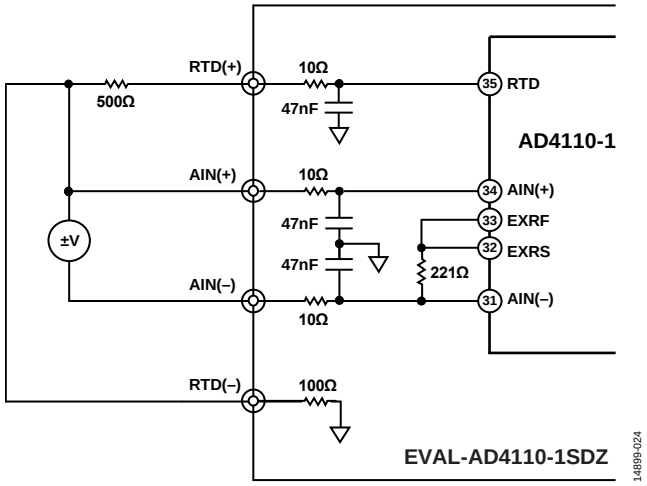

Figure 24. 4-Wire RTD Mode, Test 4 and Test 9

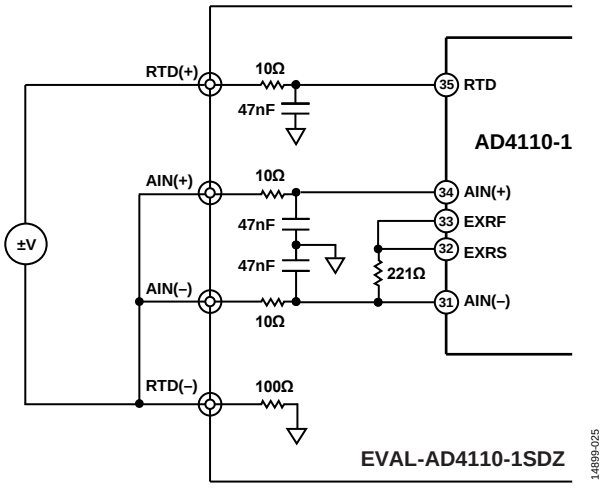

Figure 25. 4-Wire RTD Mode, Test 5 and Test 10

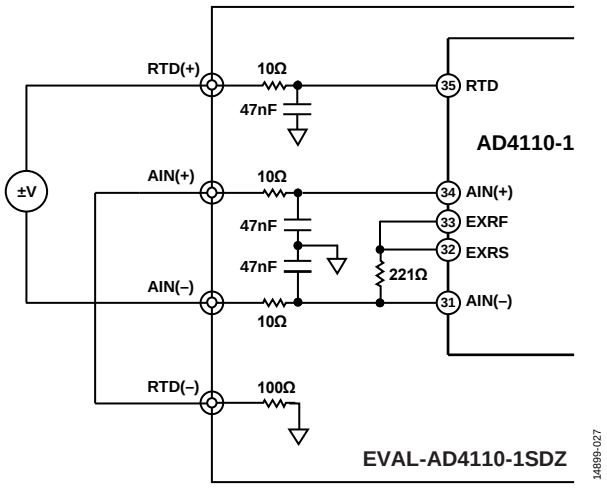

Figure 27. 4-Wire RTD Mode, Test 7 and Test 11

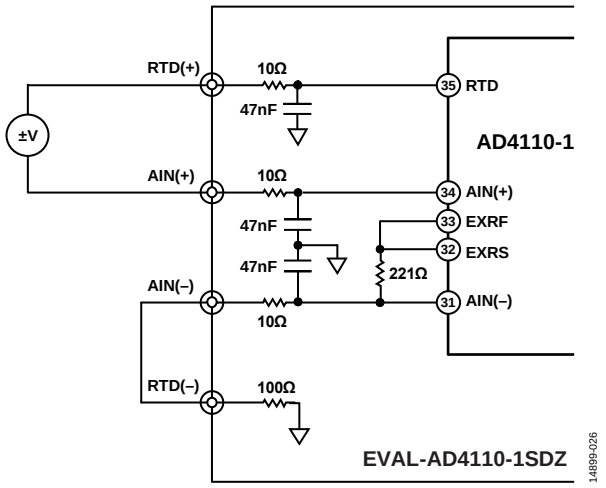

Figure 26. 4-Wire RTD Mode, Test 6 and Test 12

Table 6. Test Results for 4-Wire RTD Configurations

		Pass Level of Applied Input Voltage (V)[1]			
Test Number	**Test Configuration**	**RTD(+)**	**AIN(+)**	**AIN(–)**	**RTD(–)**
Test 1[2]	See Figure 22	0	40	0	0
Test 2[2]	See Figure 22	0	0	40	0
Test 3[2]	See Figure 23	0	−33	0	0
Test 4[2]	See Figure 24	0	0	−40	0
Test 5	See Figure 25	−40	0	0	0
Test 6	See Figure 26	40	0	0	0
Test 7	See Figure 27	40	0	0	0
Test 8[2]	See Figure 23	0	40	0	0
Test 9[2]	See Figure 24	0	0	40	0
Test 10	See Figure 25	40	0	0	0
Test 11	See Figure 27	0	0	40	0
Test 12	See Figure 26	0	40	0	0

[1] The pass level of the applied input voltage is the maximum overvoltage level at which the device meets data sheet specifications after the test.
[2] RTD excitation current set to 600 µA; therefore, RTD(+) = 0.36 V and RTD(−) = 0.06 V.

FIELD POWER SUPPLY MODE

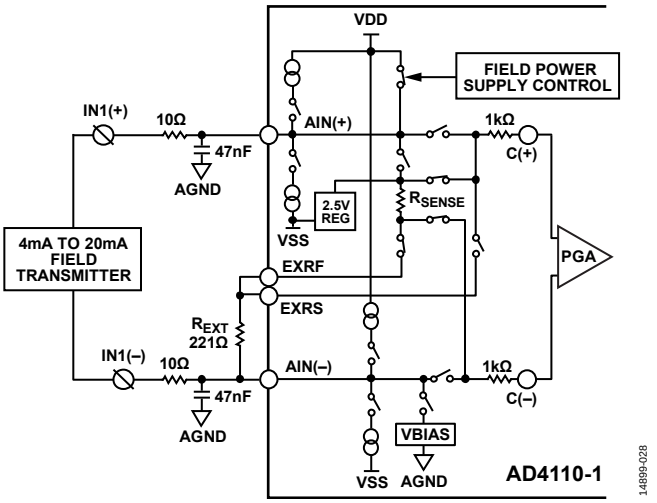

Figure 28. Typical Application Diagram—Field Power Supply Mode

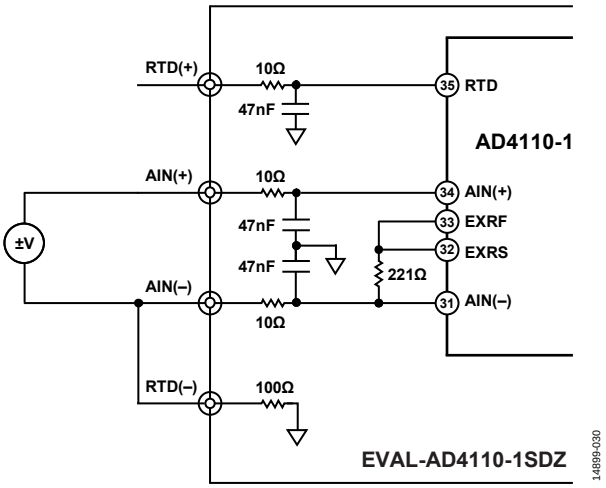

Figure 30. Field Power Supply Mode, Test 3 and Test 5

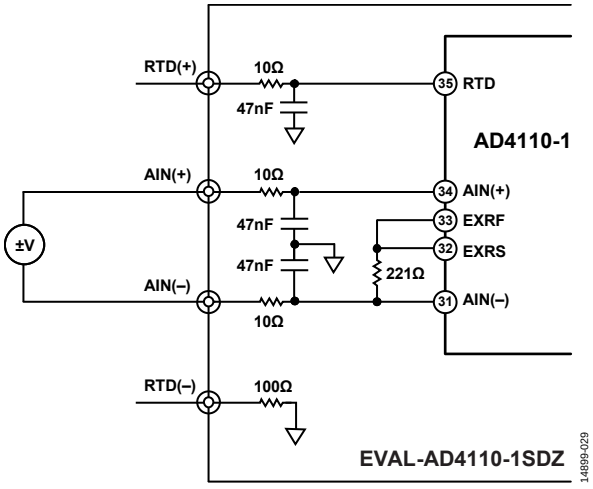

Figure 29. Field Power Supply Mode, Test 1 and Test 2

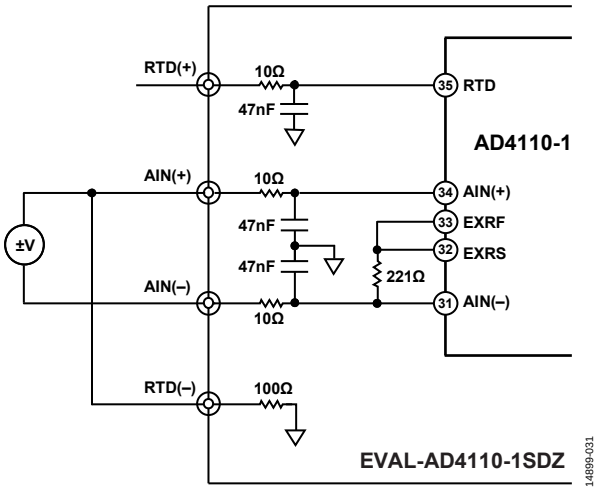

Figure 31. Field Power Supply Mode, Test 4 and Test 6

Test Results

The VDD and VSS power supply voltage is limited to ≤±15 V for the test configurations described in Table 7. The default state is AIN(+) ≈ VSS + 2.5 V = −12.5 V. Both the AIN(+) and AIN(−) pins are current limited to ~ 40 mA when shorted to AGND through the 100 Ω resistor connected to the RTD(−) pin.

Table 7. Test Results for Field Power Supply Mode Configurations

		Pass Level of Applied Input Voltage (V)[1]			
Test Number	**Test Configuration**	**RTD(+)**	**AIN(+)**	**AIN(−)**	**RTD(−)**
Test 1	See Figure 29	No connect	40	0	No connect
Test 2	See Figure 29	No connect	0	32	No connect
Test 3	See Figure 30	No connect	−35	0	0
Test 4	See Figure 31	No connect	0	40	0
Test 5	See Figure 30	No connect	40	0	0
Test 6	See Figure 31	No connect	0	40	0

[1] The pass level of the applied input voltage is the maximum overvoltage level at which the device meets data sheet specifications after the test.

NO POWER SUPPLY MODE (NPSM)

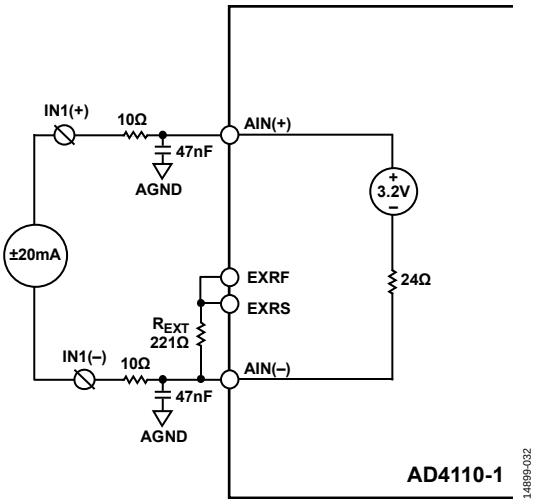

Figure 32. Typical Application Diagram—NPSM in Current Mode

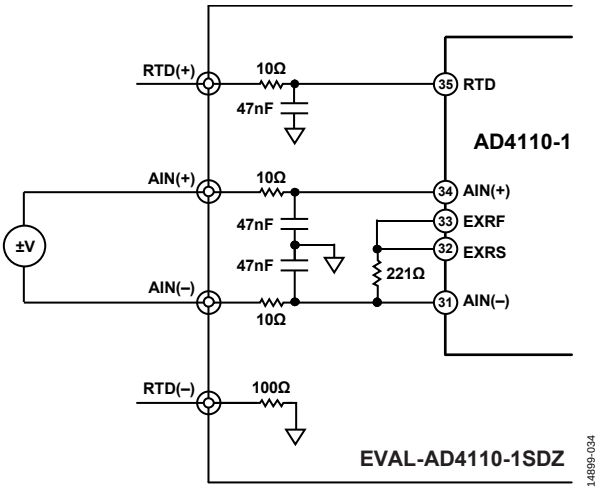

Figure 34. NPSM (Current Mode), Test 1 and Test 2

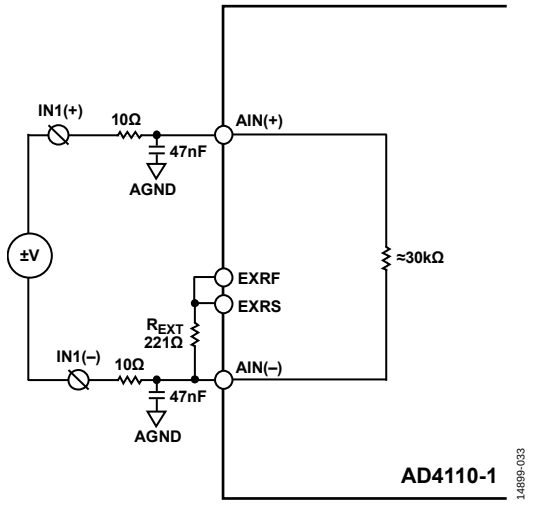

Figure 33. Typical Application Diagram—NPSM in Voltage Mode

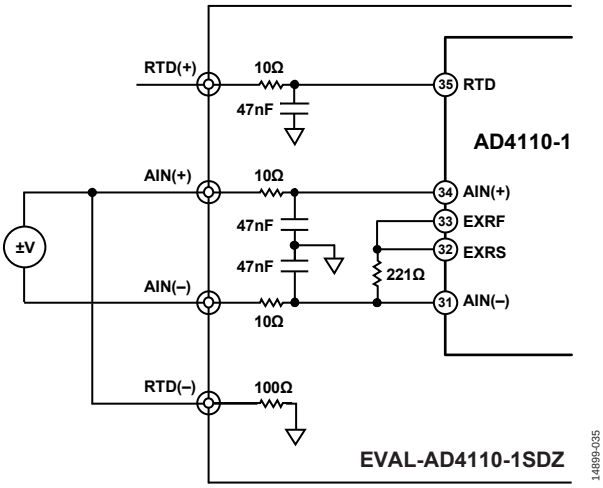

Figure 35. NPSM (Voltage Mode), Test 3 and Test 4

NPSM Test Results

The VDD and VSS power supply terminals are left open circuit.

Table 8. Test Results for NPSM Configurations

		Pass Level of Applied Input Voltage (V)[1]			
Test Number	**Test Configuration**	**RTD(+)**	**AIN(+)**	**AIN(–)**	**RTD(–)**
Test 1	See Figure 34	No connect	40	0	No connect
Test 2	See Figure 34	No connect	0	40	No connect
Test 3	See Figure 35	No connect	40	0	No connect
Test 4	See Figure 35	No connect	0	40	No connect

[1] The pass level of the applied input voltage is the maximum overvoltage level at which the device meets data sheet specifications after the test.