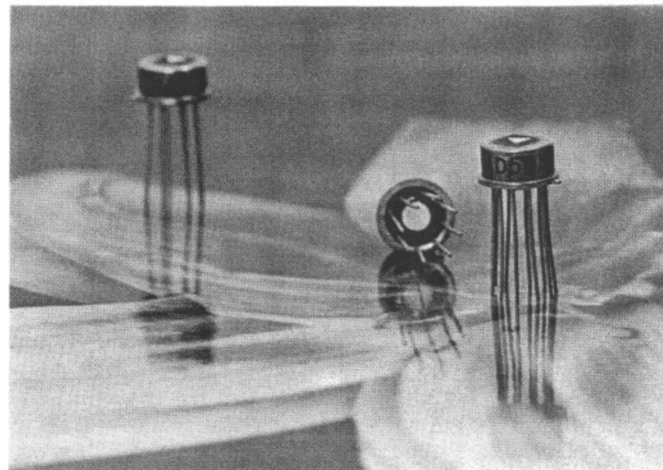
ANALOG DEVICES

Integrated Circuit High Speed Operational Amplifier

AD505

FEATURES
High Slew Rate: 120V/μsec min
Fast Settling Time: 0.1% in 800nsec
0.01% in 2μsec
Low I_b: 25nA max (K)
Low V_{os}: 2.5mV max (K)
Low V_{os} Drift: 15μV/°C max (K)
Drives 1000pF
Low Price: $10.00 (100's, J)



APPLICATIONS
D/A and A/D Conversion
Wideband Amplifiers
Active Filters
Pulse Amplifiers
Fast Multiplier Pre-Amps

PRODUCT DESCRIPTION

The Analog Devices AD505J, AD505K and AD505S are monolithic operational amplifiers that are specifically designed for applications requiring high slew rate and fast settling time to high accuracy. The AD505 achieves a minimum slew rate of 120V/μsec, provides an adjustable unity gain bandwidth product of 4MHz to 10MHz, and settles to 0.1% in 800nsec. In addition to its superior dynamic characteristics, the AD505 maintains high gain, maximum offset voltage drift of 15μV/°C, maximum bias currents of 25nA and high output swing.

The circuit has a stable 6dB/octave rolloff for closed loop operation. It is also capable of being externally adjusted for up to 35dB of additional closed loop gain at high frequencies, without causing the small signal or large signal bandwidth to decrease, and without increasing settling times.

The AD505 is designed for high speed inverting applications by using a feed-forward technique. It can drive capacitive loads in excess of 1000pF and is short circuit protected.

The AD505 provides performance superior to most high speed IC op amps and comparable to modular versions. Because of its monolithic construction, however, its cost is significantly below that of modules, and becomes even lower in large quantities.

All the circuits are supplied in the TO-100 package. The AD505J and AD505K are specified for 0°C to +70°C temperature range operation; the AD505S for operation from −55°C to +100°C.

PRODUCT HIGHLIGHTS

1. The AD505 achieves a minimum slew rate of 120V/μsec and settles to 0.1% in 800nsec.
2. All guaranteed parameters, including slew rate and offset voltage drift, are 100% tested.
3. The AD505 maintains low bias currents of 25nA max and low V_{OS} drift of 15μV/°C max.
4. Ease of use and predictability of operation make the AD505 an all-purpose amplifier that is free of the problems found in most high frequency amplifiers.

SLEW RATE AND SETTLING TIME

Both slew rate and settling time are measures of an amplifier's speed of response to an input. Slew rate is an inherent characteristic of the amplifier and, thus, is generally less subject to misinterpretation than is settling time, which is often more dependent upon the test circuit than the amplifier's ability to perform.

Slew rate defines the maximum rate of change of output voltage for a large input step change and can be related to the full power response (f_p) by the relationship . . . . .

$$S = 2\pi f_p E_o$$

. . . . . where E_o is the peak output voltage.

(continued on page 3)

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SPECIFICATIONS (typical @ +25°C and ±15VDC, unless otherwise noted)

PARAMETER	AD505J	AD505K	AD505S
OPEN LOOP GAIN			
$R_L = 2k\Omega$, $V_o = \pm10V$	100,000 min (500,000 typ)	200,000 min (500,000 typ)	**
Over Temp Range (T_{min} to T_{max})	75,000 min	150,000 min	100,000 min
OUTPUT CHARACTERISTICS			
Voltage @ $R_L = 2k\Omega$			
Over Temp Range (T_{min} to T_{max})	±10V min (±12V typ)	*	*
Current @ $V_o = \pm10V$	±10mA	*	*
Short Circuit Current	25mA	*	*
FREQUENCY RESPONSE			
Unity Gain, Small Signal	4 - 10MHz (adjustable)	*	*
Full Power Response	2.0MHz min (2.5MHz typ)	*	*
Slew Rate	120V/µsec min (150V/µsec typ)	*	*
Settling Time (Note 1)			
to 0.1%	800nsec	*	*
to 0.01%	2.0µsec	*	*
INPUT OFFSET VOLTAGE			
Initial, $R_S \leq 10k\Omega$	5.0mV max (1.0mV typ)	2.5mV max (1.0mV typ)	**
Avg vs Temp (T_{min} to T_{max})	15µV/°C	15µV/°C max (8µV/°C typ)	20µV/°C max (10µV/°C typ)
vs Supply (T_{min} to T_{max})	150µV/V max (80µV/V typ)	*	*
INPUT BIAS CURRENT			
Initial	75nA max (15nA typ)	25nA max (15nA typ)	**
Over Temp Range ($_{min}$ to T_{max})	100nA max	40nA max	80nA max
Avg vs Temp (T_{min} to T_{max})	0.1nA/°C	*	*
INPUT IMPEDANCE			
DC	2MΩ	*	*
Above 10Hz	20kΩ	*	*
INPUT NOISE			
Voltage, 0.01 to 10Hz(p-p)	2.5µV	*	*
0.01 to 1.0MHz(rms)	10µV	*	*
Current, 0.01 to 10Hz(p-p)	0.1nA	*	*
POWER SUPPLY			
Rated Performance	±15V	*	*
Operating, Derated Performance	±(5 to 20)V	*	*
Current, Quiescent	8.0mA max (6.0mA typ)	*	*
TEMPERATURE RANGE			
Rated Performance (T_{min} to T_{max})	0°C to +70°C	*	−55°C to +100°C (Note 2)
Operating	−25°C to +85°C	*	−55°C to +100°C (Note 2)
Storage	−65°C to +150°C	*	*
PRICE (Note 3)			
(1−24)	$15.00	$18.00	$21.00
(25−99)	$12.00	$14.40	$16.80
(100−999)	$10.00	$12.00	$14.00

NOTES:

[1] See Figure 1 for test circuit diagram.
[2] +125°C operation is possible with a 100°C/W heat sink.
[3] Subject to change; refer to latest Microcircuit Price List

*Specifications same as AD505J
**Specifications same as AD505K

(continued from page 1)

Settling time is defined as the time elapsed from the application of a fast step input to the time when the amplifier output has entered and remained within a specified error band that is symmetrical about the final value. Settling time, therefore, is comprised of an initial propagation delay, an additional time for the amplifier to slew to the vicinity of some value of output voltage, and a time period to recover from overload and settle within the given error band (see Figure 1).

ADI tests for slew rate and settling time in a unity gain configuration ($R_S = R_f = 10k\Omega$), no capacitive load, and a −10 volt to a +10 volt output swing.

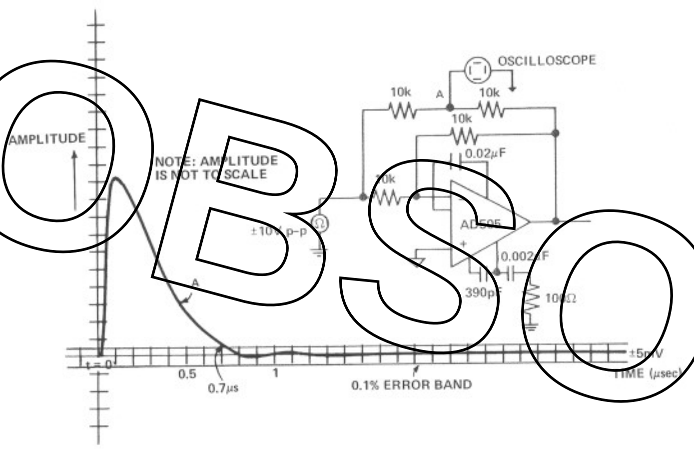


Figure 1. Settling Time of the AD505.

The full power response of the AD505 is displayed in Figure 2 for supply voltages of ±15V and ±10V. Note that at $V_S = \pm15V$ the full power response is greater than 2MHz and that it decreases as the supply voltages are lowered.

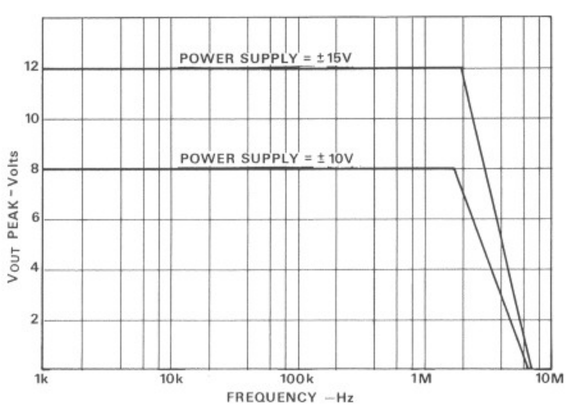


Figure 2. Full Power Response of the AD505.

APPLICATIONS CONSIDERATIONS

The AD505 combines excellent DC characteristics and dynamic performance with ease of application. Because it is a wideband, fast settling amplifier, certain practical stabilization and interconnection techniques are suggested to insure proper operation and minimize user experimentation.

The feed-forward operation of the AD505 is shown in the block diagram in Figure 3. The DC signal is via the input differential current amplifier, followed by a gain stage. An external 390pF capacitor connected between pins 1 and 9 makes this gain stage an integrator and optimizes settling time. A 4700pF capacitor in series with a 100Ω resistor is connected between pins 9 and 5 (V−) to provide a lag which insures that this portion of the amplifier rolls off to below unity gain above the frequency at which the fast DC amplifier starts its rolloff. The AC signal is fed forward by an external 0.02µF capacitor connected between pin 4 and pin 10 into the other differential input of the fast DC amplifier.

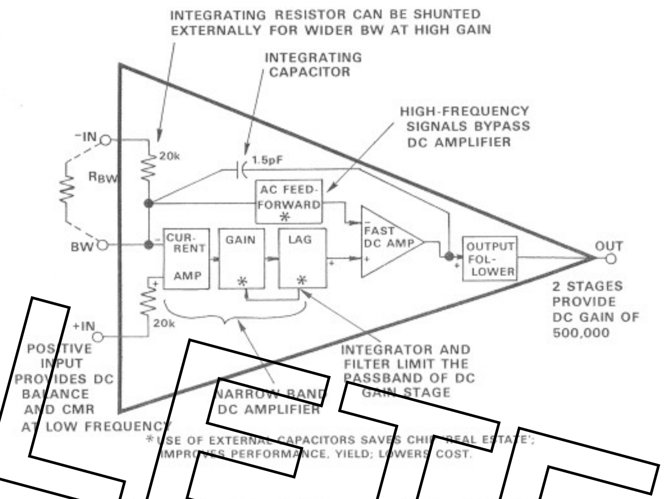


Figure 3. Block Diagram of the AD505.

To help the user achieve best results with the AD505, here are a few reminders . . . . .

(1) Power supply bypasses should be provided as close to the amplifier as possible to eliminate ringing due to the inductance of power supply leads. A tantalum 10µF capacitor in parallel with a ceramic 0.01µF capacitor is sufficient for this purpose (see Figure 4).

(2) All ground connections should be made at a single ground point.

(3) Keep leads short to eliminate stray impedance effects.

Figure 4 shows an optimum wiring diagram of the AD505.

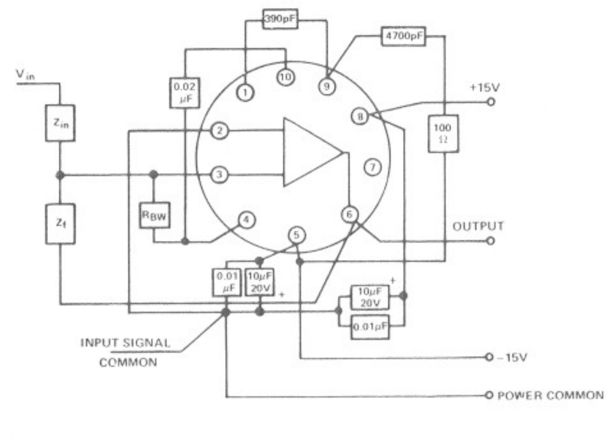


Figure 4. Wiring Diagram of the AD505.

GENERAL PURPOSE WIDEBAND COMPENSATION

An approximate high frequency equivalent circuit of the AD505 is shown in Figure 5. The unity gain open loop gain bandwidth product can be adjusted over the range of 4MHz to 10MHz by selecting resistor (R_{BW}) which is connected between pin 4 and pin 3. The lowest gain bandwidth product is a result of an open circuit ($R_{BW} = \infty$) between pins 3 and 4, while the maximum is achieved by a short circuit ($R_{BW} = 0$). Figure 6 displays the open loop frequency and phase response of the AD505. Note that as R_{BW} decreases the open loop gain increases, and that the amplifier is stable as long as the loop unity gain crossover is below 10MHz. In the $R_{BW} = \infty$ condition, the leading phase shift above 200kHz is a result of stray capacitance across the 20kΩ input resistor, and can be used by the designer to increase network stability.

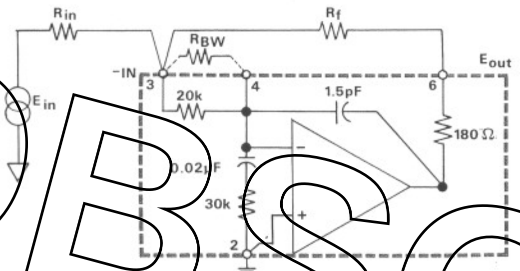
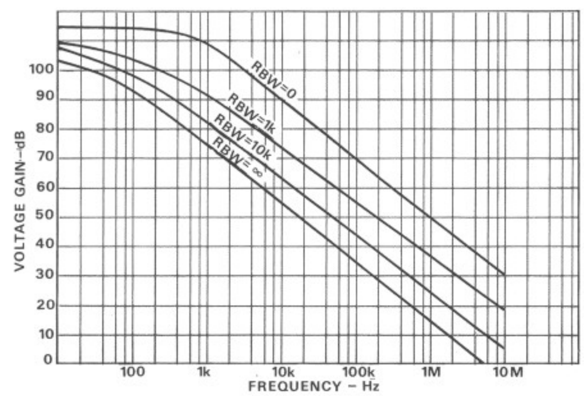
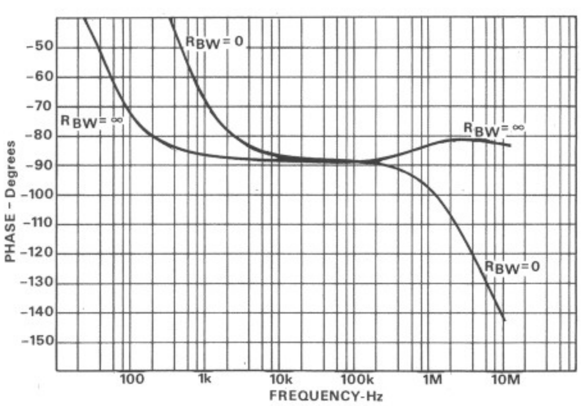


Figure 5. Approximate High Frequency Equivalent Circuit.



(a)



(b)

Figure 6. Open Loop Frequency and Phase Response.

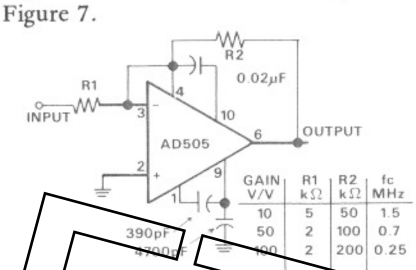
The input impedance at high frequencies can be represented by, in effect, a 350Ω resistor to common (the "Miller" impedance of a 1.5pF capacitor*). This low impedance effectively permits the amplifier to be stable (for large enough values of R_f) even at low values of signal gain. For example, with $R_{BW} = 0$, a stable gain of 10 (20dB) can be obtained using $R_S = 5k\Omega$ and $R_f = 50k\Omega$, since the input impedance of 500Ω dominates the 5kΩ source resistor. Similarly, a gain of 50.....without any reduction in bandwidth.....can be obtained using a 1kΩ:50kΩ ratio.

$$^*Z_{in} \approx \frac{X_c(\omega)}{G(\omega)} = \frac{1}{2\pi \cdot f \cdot C \cdot G(\omega)} = 350\Omega \text{ at } f = 1\text{MHz},$$

where $G(\omega)$ = open loop gain as a function of frequency and $X_c(\omega)$ = reactive capacitance of capacitor.

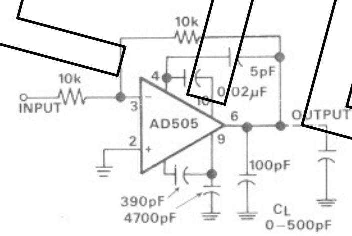
Note: At high frequencies, Z_{in} is approximately constant since f and $G(\omega)$ are inverse functions of frequency.

In order to provide application flexibility and low cost, the AD505 is externally compensated with several capacitors. Several compensation circuits for differing conditions are shown in Figure 7.

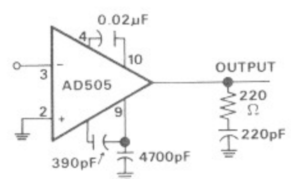


GAIN V/V	R1 kΩ	R2 kΩ	fc MHz
10	5	50	1.5
50	2	100	0.7
100	2	200	0.25

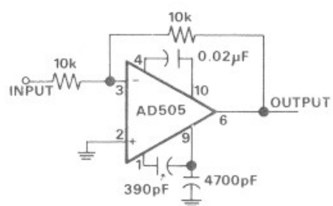
(a) Connection for higher gains (up to 500pF load)



(b) Connection as unity gain inverter (capacitive load)



(c) Connection for 100% feedback (e.g., as low-frequency integrator)



(d) Connection as unity gain inverter

Figure 7. Compensation Connections of AD505 for Various Conditions of Feedback.

NULLING THE AD505

The offset voltage of the AD505 is extremely small and, therefore, nulling is generally not required. However, should offset nulling be desirable, Figure 8 shows a very effective, high resolution nulling circuit that may be used without degrading other performance parameters. This offset arrangement can also be used to correct for any system error that may be present, without affecting the performance of the amplifier.

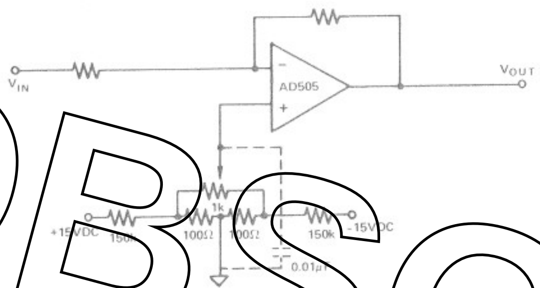


Figure 8. High Resolution External Nulling Circuit.

The indicated values in Figure 8 represent one specific case and can be easily adjusted to any particular application. If the impedance of this network as seen from the positive terminal of the AD505 is higher than 10kΩ, it is suggested that a 0.01μF capacitor to ground be used to bypass the network.

INPUT CHARACTERISTICS

In addition to its superior dynamic characteristics, the AD505 maintains low bias currents of 25nA max and a low V_{OS} drift of 15μV/°C max.

Figure 9 displays the input bias current vs. temperature characteristic of the AD505. Note that the bias current at room temperature is 15nA and increases to less than 25nA at −55°C.

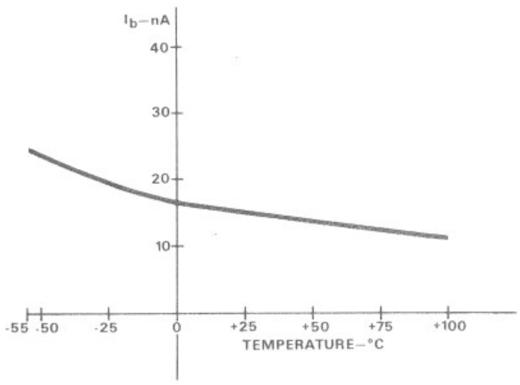


Figure 9. Input Bias Current vs. Temperature.

Figure 10 displays the offset voltage drift characteristic of the AD505. Note that average temperature coefficient of the offset voltage is approximately 2.5μV/°C for higher temperatures and 5.0μV/°C for low temperatures.

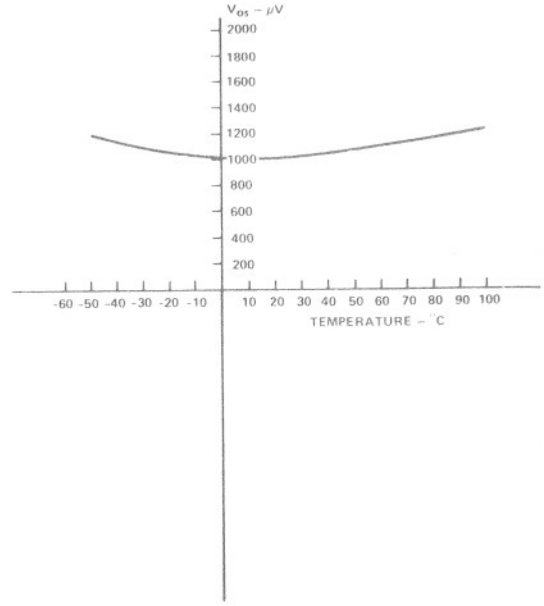
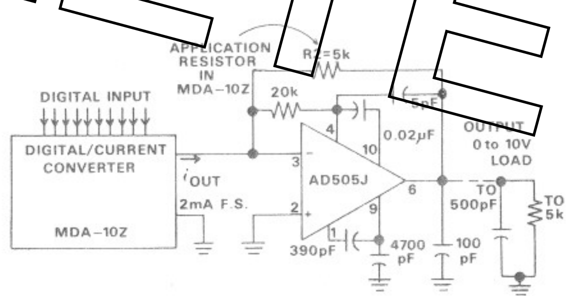


Figure 10. Offset Voltage Drift of the AD505.

TYPICAL APPLICATIONS

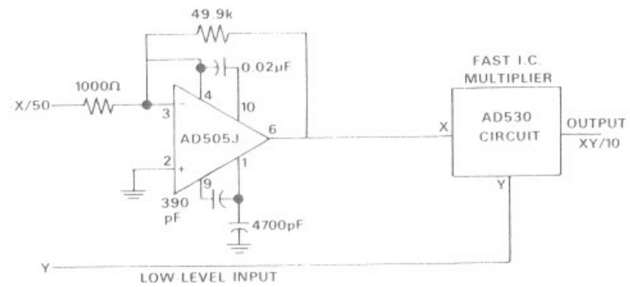


AD505J as Fast Current-to-Voltage Converter.

Fast Output Buffer for Digital/Current Converter

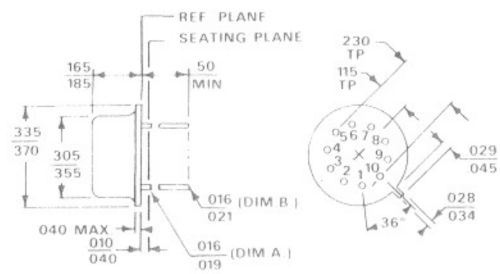
In this configuration, the converter and amplifier settle to within 0.1% (1 LSB) in 3μs, and to within ½ LSB in 5μs, typically. With the component values indicated, the AD505 can feed load impedance of 5kΩ in parallel with 500pF. Interwiring capacitance between the converter output and the amplifier input, plus the converter's output capacitance, should be held to within 10pF if possible. When applied with the *bipolar* version of MDA-10Z, the built-in feedback resistor for ±10V output is 10kΩ. The 20kΩ R_{BW} shunt should be replaced by about 5kΩ.

Although the MDA-10Z is indicated in this example, the AD505 may be used to unload converters having output impedance values other than the MDA-10Z's 1.5kΩ. For example, when used with a 10-bit converter assembled from μDAC switches and resistor networks, the external R_{BW} shunt may be omitted and a 7.5kΩ load connected from the summing point to ground.

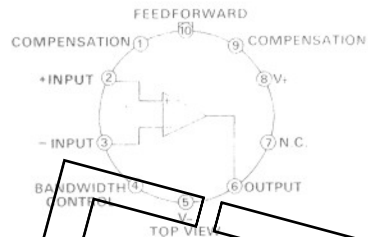


Preamplifier for Fast IC Multiplier

OUTLINE DIMENSIONS



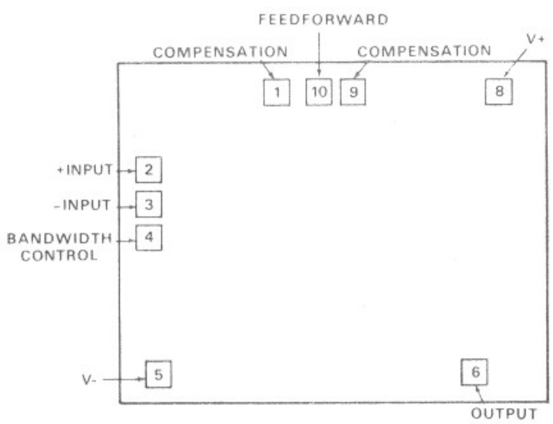
TO-100 PIN CONFIGURATION



Preamplifier for Fast IC Multiplier
Multipliers often provide their best accuracy when both inputs and output can swing through the full-scale range. One of the problems in taking advantage of the excellent high frequency capabilities of the AD530 Multiplier-Divider is simply finding a low-cost integrated-circuit amplifier capable of driving it with ±10V at frequencies up to 1MHz. The AD505J makes an excellent preamplifier for this purpose; it is shown above connected for gain of 50, and applied to one of the AD530 inputs. Either or both input signals can be preamplified in this manner.

In this circuit, the internal 20kΩ resistor has been shorted out for maximum bandwidth. The frequency for −3dB response in this configuration is typically 1.6MHz, with full output capability.

BONDING DIAGRAM



The AD505 is available in chip or wafer form. Because of the critical nature of using unpackaged devices, it is suggested that the factory be contacted for specific information regarding price, delivery and testing.

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