PRODUCT DESCRIPTION

The Analog Devices AD508 is the highest accuracy IC operational amplifier presently available. Its combination of low drift (0.5μV/°C max), low offset current (1.0nA max), and long term stability (10μV/month max) make it the choice for all applications requiring the utmost in precise performance from an IC op amp. Guaranteed parameters also include gain greater than 10^6, PSRR less than 10μV/V, CMRR above 110dB, and offset voltage below 0.5mV – nullable to zero. In addition, the AD508's superbeta input transistor quad results in maximum offset and bias currents of 1nA and 10nA, while permitting the input stage to operate at sufficiently high current levels to provide a unity gain slew rate of 0.12V/μsec and small signal bandwidth of 300kHz.

The outstanding long term stability of the AD508 is attained by subjecting 100% of the devices to a 100 hour stabilization burn-in. Following this, the AD508L is closely monitored during an additional 500 hours of operation, during which time it must meet interim and end-point limits in order to be qualified to its 10μV/month maximum drift performance. The AD508 thus provides overall accuracy which equals or exceeds that of most discrete component modules utilizing conventional low drift circuit approaches. For the ultimate in long term stability, however, a chopper stabilized amplifier, such as the Analog Devices model 260 (1μV/month) should be used. Because of its monolithic construction, the cost of the AD508 is significantly below that of modules, and becomes even lower in large quantities.

The AD508J, K and L are supplied in the TO-99 package for operation over the 0°C to +70°C temperature range. The AD508S, for operation from –55°C to +125°C will be available in the Fall of 1972.

PRODUCT HIGHLIGHTS

1. Fully guaranteed and 100% tested maximum offset voltage drift of ±0.5μV/°C and maximum offset voltage of 500μV (AD508K).
2. Offset and bias currents of 1.0nA and 10nA achieved by superbeta processing (AD508K and AD508L).
3. Guaranteed maximum long term V_{OS} drift of ±10μV/month (AD508L).
4. Fully protected input (±V_S) and output circuitry. The input protection circuit prevents offset voltage and bias current degradation due to reverse breakdown, and is of critical importance in this type of device whose overall performance is strongly dependent on front-end stability.
5. Single capacitor compensation eliminates elaborate stabilizing networks while providing flexibility not possible with an internally compensated op amp. This feature allows bandwidth to be optimized by the user for his particular application.
6. High gain is maintained independent of offset nulling, power supply voltage and load resistance.
7. Bootstrapping of the circuit input transistor quad produces CMRR and PSRR compatible with the tight ±0.5μV/°C drift. CMRR and PSRR are errors in the vicinity of 1 part per million.
8. Noise performance is closely monitored at Outgoing QC to insure compatibility with the low error budgets afforded by the performance of all other parameters.
9. To insure reliability and long-term stability, every AD508 is stored for 48 hours at 200°C, temperature cycled 10 times from –65°C to +200°C and subjected to a high 'g' shock test prior to a 100-hour stabilization burn-in.

APPLICATIONS

The AD508 is specifically designed for high precision applications calling for error budgets in the parts-per-million category, such as stable references and accurate analog computing. It is ideally suited for numerous low level applications in precision measurement, telemetry, and data acquisition. Because of its low drift and noise, it is well qualified for pre-amplification of small signals in the dc-to-audio frequency range. Its excellent common mode rejection and protected inputs make the AD508 well suited for bridge measurements, follower applications, and use in such instruments as variable-range high-input-impedance voltmeters. Its low power drain (typically 5mW with a ±5V supply) and insensitivity to temperature variations make it ideal for use in battery-powered instrumentation.

PRELIMINARY CHARACTERIZATION DATA

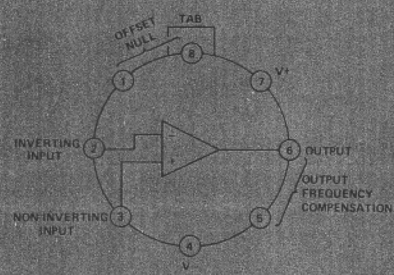
AD508J
AD508K
AD508L

INTEGRATED CIRCUIT CHOPPERLESS LOW DRIFT OPERATIONAL AMPLIFIER

FEATURES

- Low V_{OS} Drift (100% tested)
  ±0.5μV/°C max (K)
  ±1.0μV/°C max (L)
  ±3.0μV/°C max (J)
- Low Input Currents
  I_{OS} 1.0nA max (K, L)
  I_b 10nA max (K, L)
- Guaranteed Long-Term Drift
  ±10μV/month max (L)
- High Gain
  > 10^6 for all conditions
- Uncompromised Frequency Response
  f_t = 300kHz
  f_p = 1.5kHz
- Low Noise
  1.0μV(p-p)
- Low Cost
  $14.00 (100's, J)

TO-99 PIN CONFIGURATION



TOP VIEW

ANALOG DEVICES
LINEAR INTEGRATED CIRCUITS
ROUTE ONE INDUSTRIAL PARK
P.O. BOX 280, NORWOOD, MASS. 02062
TEL: 617/329-4700 TWX: 710/394-6577

ELECTRICAL SPECIFICATIONS (typical at 25°C and ±15VDC, unless otherwise specified)

PARAMETER	AD508J	AD508K	AD508L
OPEN LOOP GAIN			
V_O = ±10V, $R_L \geq 2k\Omega$	250,000 min (4 x 10^6 typ)	10^6 min (8 x 10^6 typ)	10^6 min (8 x 10^6 typ)
@ T_A = 0°C to +70°C	125,000 min (10^6 typ)	500,000 min (10^6 typ)	500,000 min (10^6 typ)
OUTPUT CHARACTERISTICS			
Voltage, $R_L \geq 2k\Omega$, T_A = 0°C to +70°C	±10V min (±13V typ)	*	*
Load Capacitance	1000pF	*	*
Output Current	10mA min	*	*
Short Circuit Current	25mA	*	*
FREQUENCY RESPONSE			
Unity Gain, Small Signal, C_C = 390pF	300kHz	*	*
Full Power Response, C_C = 390pF	1.5kHz	*	*
Slew Rate, Unity Gain, C_C = 390pF	0.12V/μsec	*	*
INPUT OFFSET VOLTAGE			
Initial Offset, $R_S \leq 100\Omega$	±2.5mV max (±1.0mV typ)	±0.5mV max (±0.2mV typ)	±0.5mV max (±0.2mV typ)
vs. Temperature,			
T_A = 0°C to +70°C, V_{os} nulled	±3.0μV/°C max (±0.5μV/°C typ)	±0.5μV/°C max (±0.25μV/°C typ)	±1.0μV/°C max (±0.3μV/°C typ)
T_A = 0°C to +70°C, V_{os} unnulled†	±10μV/°C max (±1.5μV/°C typ)	±2.5μV/°C max (±1.0μV/°C typ)	±2.5μV/°C max (±1.0μV/°C typ)
vs. Supply	±25μV/V max	±10μV/V max	±10μV/V max
@ T_A = 0°C to +70°C	±40μV/V	±15μV/V max	±15μV/V max
vs. Time	±15μV/mo	±10μV/mo	±10μV/mo max
INPUT OFFSET CURRENT			
Initial	±5.0nA max (±2.5nA typ)	±1.0nA max (±0.5nA typ)	±1.0nA max (±0.5nA typ)
@ T_A = 0°C to +70°C	±8.0nA max	±1.5nA max	±1.5nA max
vs. Temp, T_A = 0°C to +70°C	±14pA/°C	±4pA/°C	±4pA/°C
INPUT BIAS CURRENT			
Initial	25nA max (10nA typ)	10nA max (6nA typ)	10nA max (6nA typ)
@ T_A = 0°C to +70°C	40nA max	15nA max	15nA max
vs. Temp, T_A = 0°C to +70°C	±100pA/°C	±40pA/°C	±40pA/°C
INPUT IMPEDANCE			
Differential	4MΩ	6MΩ	6MΩ
Common Mode	100MΩ‖4pF	*	*
INPUT NOISE			
Voltage, 0.01 to 10Hz	1.0μV (p-p)	*	*
100Hz	12nV/√Hz (rms)	*	*
1kHz	10nV/√Hz (rms)	*	*
Current, 100Hz	0.3pA/√Hz (rms)	*	*
1kHz	0.2pA/√Hz (rms)	*	*
INPUT VOLTAGE RANGE			
Differential or Common Mode, Max Safe	$\pm V_S$	*	*
Common Mode Rejection, V_{in} = ±10V	94dB min (120dB typ)	110dB min (120dB typ)	110dB min (120dB typ)
vs. Temp, T_A = 0°C to +70°C	100dB	100dB min	100dB min
POWER SUPPLY			
Rated Performance	±15V	*	*
Operating	±(5 to 18)V	*	*
Current, Quiescent	±4.0mA max (±1.5mA typ)	±3.0mA max (±1.5mA typ)	±3.0mA max (±1.5mA typ)
TEMPERATURE RANGE			
Operating, Rated Performance	0°C to +70°C	*	*
Storage	−65°C to +150°C	*	*
PRICE**			
1 - 24	$21.20	$29.80	$38.00
25 - 99	16.80	24.00	34.00
100 - 999	14.00	20.00	30.00

*Specification same as for AD508J.
**Subject to change; refer to latest Microcircuit Price List.
†This parameter is not 100% tested; typically, 90% of the units meet this limit.

STABILIZATION

All AD508's, after complete dc testing at 25°C, are subjected to 100 hours of operating stabilization. A substantial number of unit-hours of amplifier operation demonstrate that there is a considerable reduction in V_{OS} variation with time during the first 100 hours of powered operation. Further, long term drift performance can be inferred from 100 hour drift performance.

Figure 1 shows V_{OS} variation vs. time for a typical AD508 during 168 hours of power operation. The V_{OS} readings are normalized to the final value. Note that the major V_{OS} variations occur during the first 48 to 72 hours of operation, and that there is an order of magnitude improvement in V_{OS} stabilization by the 100 hour point.

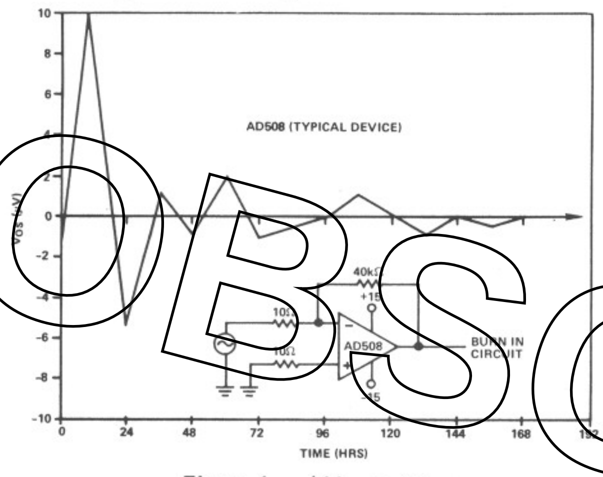


Figure 1. ΔV_{OS} vs. Time

The 100 hour stabilization provided for all AD508's thus provides the user with two distinct advantages........

(1) Since the vast majority of component malfunctions generally occur during the first 100 hours of operation, an extremely high operating confidence level is attained.

(2) From the time the device is first operated in its circuit application, its stability is approximately an order of magnitude better than an unstabilized unit.

Following the initial 100 hour operating period, all AD508's are tested over temperature to determine their V_{OS} drift classification. All potential AD508L's are operated for an additional 500 hours, during which time they must meet interim and end point stability limits in order to be qualified to the AD508L maximum variation of ±10μV/month. Figure 2 shows V_{OS} variation with time for a typical AD508L, with the readings normalized to the end point value.

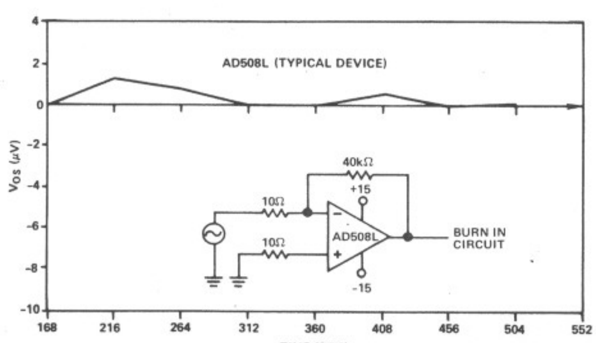


Figure 2. ΔV_{OS} vs. Time

Figure 3 shows, in flow chart form, the entire stabilization procedure used to qualify AD508's.

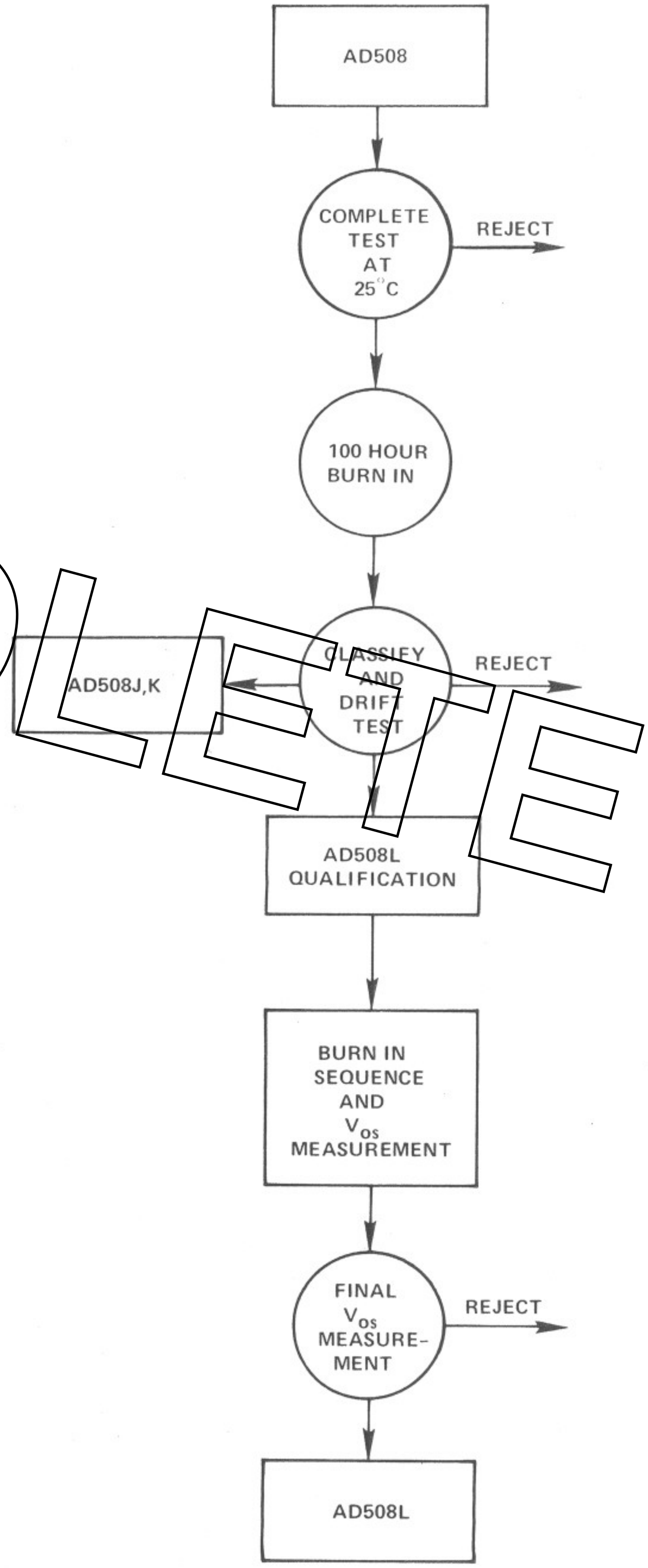


Figure 3. AD508 Stabilization

ERROR BUDGET FOR AD508

The guaranteed long term drift stability of the AD508 allows the user, for the first time, to calculate a long term IC error budget that he can rely on. (See Table I.) Note that voltage drift and gain are specified with the device nulled.

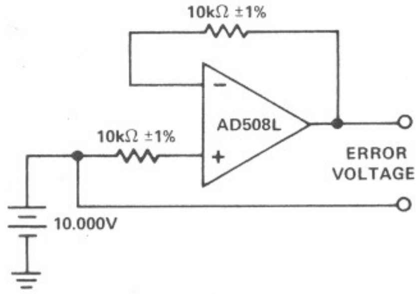


Figure 4. Circuit Configuration

Parameter	Specification and Condition at 25°C	Error (25°C)	Error (70°C)*
Gain	10^6 min, 10V input	10µV	20µV
Bias Current	10nA max x 200Ω (assuming 2% resistor mismatch)	2µV	3µV
Offset Current	1nA max x 10kΩ	10µV	15µV
Voltage Drift	1µV/°C max	—	45µV
Stability	10µV/month max	10µV	10µV
CMRR	110dB min, 10V input	32µV	100µV
PSRR	10µV/V max (assuming a worst case of ±5% variation in power supply voltage)	30µV	45µV
Noise (0.01 to 10Hz)	1.0µV (p-p) typ (assuming worst case = 3 x typ)	1.5µV	3µV
	TOTAL	95.5µV	241µV

* For specifications over temperature, see electrical specifications portion of data sheet.

Table 1. Error Budget for the AD508L.

The above table displays the worst case output voltage error for a period of one month using the AD508L. Note that total maximum error at room temperature is less than 10ppm full scale and, in actual practice, will be substantially lower, since all errors will not be worst case and will add as an rms total error. This performance is an order of magnitude improvement above most other available precision op amps. Thus it is possible to guarantee that, if an AD508L is used in the above configuration, the worst case error voltage for one (1) year at 25°C will not exceed 0.002% of 10V full scale!

DRIFT VS. SOURCE RESISTANCE

The excellent input characteristics of the AD508 permit the designer to use relatively large values of source resistance without degrading the offset voltage drift performance of the device. Figure 5 displays the worst case offset drift vs. source resistance for the AD508. Note that when using the AD508K in nulled applications, the maximum voltage error referred to the input is less than 1.0µV/°C for all values of R_S below 100kΩ.

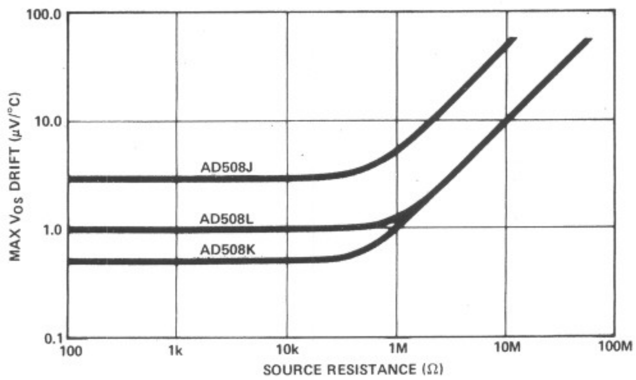


Figure 5. Max Equivalent Input Offset Drift vs R_S

OFFSET VOLTAGE DRIFT AND NULLING

Most differential operational amplifiers have provisions for adjusting the initial offset voltage to zero with an external trim potentiometer. It is often not realized that there is a secondary increase in voltage drift which accompanies this initial offset adjustment. The increased voltage drift can often be safely ignored in conventional amplifiers, since it may be a small percentage of the specified voltage drift. However, the voltage drift of the AD508 is so small that this effect cannot be ignored.

To achieve low drift over temperature, it is necessary to maintain equal current densities in the input pair. Unless the initial offset nulling circuit is carefully arranged, the nulling circuits will themselves drift with temperature. The resulting change in the input transistor current ratio will produce an additional input offset voltage drift. This drift component can actually be larger than the unnulled drift.

Typically, IC op amps are nulled by using an external potentiometer to adjust the ratio of two resistances. These resistances are part of a network from which the input stage emitter currents are derived. Most commercially available op amps use diffused resistors in their internal nulling circuitry, which typically display large positive temperature coefficients of the order of 2000ppm/°C. As a result of the failure of the external potentiometer resistance to track the diffused resistors over temperature, the two resistance branches will drift relative to one another. This will cause a change in the emitter current ratio and induce an offset drift with temperature.

In the AD508, this problem is reduced an order of magnitude by the use of thin film resistors deposited on the monolithic amplifier chip. These resistors, which make up the critical bias network from which the input stage emitter current balance is determined, display typical temperature coefficients of less than 200ppm/°C, an order of magnitude improvement over diffused types. Thus, when the initial offset of the AD508 is trimmed using a low TC pot in combination with the thin film network, the drift induced by nulling even relatively large offsets is extremely small. This means that AD508 units of all three grades (J, K, L) will typically yield significantly better temperature performance in nulled applications than an all-diffused amplifier with comparable initial offset.

Since the intrinsic offset drift of the amplifier is improved by nulling, the direct measurement of any additional drift induced by differing temperature coefficients of resistors would be extremely difficult. However, the induced offset drift can be established by calculating the change in the emitter current ratio brought about by the differing TC's of resistance. From the change in this ratio, the offset voltage contribution at any temperature can be easily calculated.

A simple computer program was written to calculate induced offset drift as a function of initial offset voltage nulled. The results of these calculations are summarized graphically in Figure 6.

Figure 6 shows the variation of induced voltage drift with nulled offset voltage for..........

(a) AD508 op amp
(b) 725 type op amp

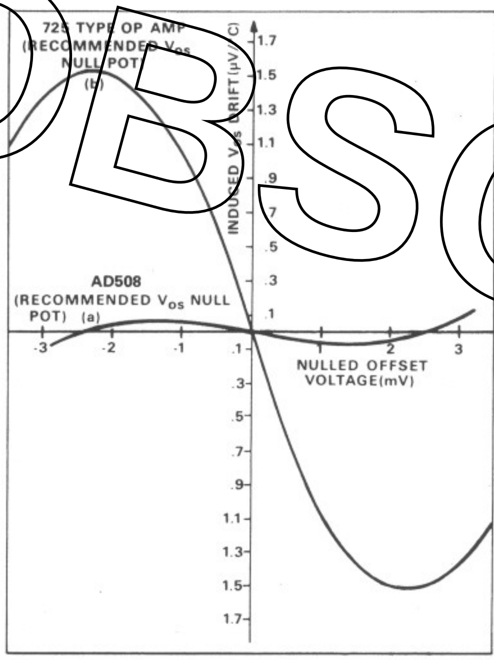


Figure 6. Induced Offset Drift vs. Nulled Offset Using Manufacturer's Recommended Adjustment Potentiometer

Note that as a result of nulling 1.4mV of offset, the AD508 induces 30X less offset drift (only 0.05µV/°C) than the 725 type op amp with its actual diffused resistor values and the recommended 100kΩ pot to trim the offset. Actual induced drifts from this source for the AD508 may be even lower in the practical case when metal film resistors or pots are used for nulling, since their TC's tend to closely match the negative TC's of the thin film resistors on the AD508 chip.

NULLING THE AD508

Since calculations show that superior drift performance can be realized with the AD508, special care should be taken to null it in the most advantageous manner. Using the actual values of resistors in the 508, it is possible to calculate that the total adjustment range of the 508 is approximately 8mV. Since the amplifier may often be trimmed to within 1µV, this represents an adjustment of 1 part in 8000. This type of accuracy would require a pot with 0.0125% resolution and stability. Because of the problems of obtaining a pot of this stability, a slightly more sophisticated nulling operation is recommended for applications where initial drift is critical. (See Figure 7A.)

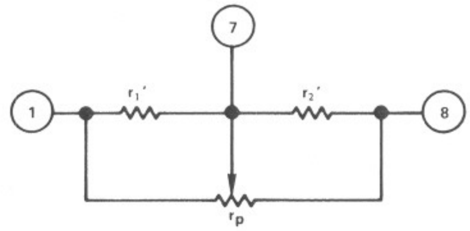


Figure 7A. High Resolution, High Stability Nulling Circuit

NULLING PROCEDURE

1. Null the offset to zero using a commercially available pot (suggest r_p = 10kΩ).
2. Measure pot halves r_1 and r_2.
3. Calculate..........

$$r_1' = \frac{r_1 \times 50k\Omega}{50k\Omega - r_1}; \quad r_2' = \frac{r_2 \times 50k\Omega}{50k\Omega - r_2}$$

4. Insert r_1' and r_2' (closest 1% fixed metal film resistors).
5. Use an industrial quality 100kΩ pot (r_p) to fine tune the trim.

For applications in which stringent nulling is not required, the user may choose a simplified nulling scheme as shown in Figure 7B. For best results the wiper of the potentiometer should be connected directly to pin 7 of the op amp. This is true for both nulling schemes.

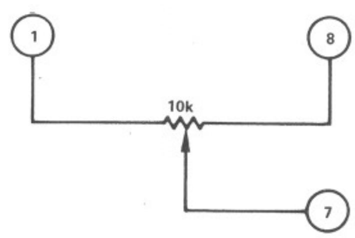


Figure 7B. Simplified Nulling Circuit

INPUT BIAS CURRENT

Superbeta processing of input transistors achieves maximum bias currents of 10nA. The input bias current vs. temperature characteristic is displayed in Figure 8.

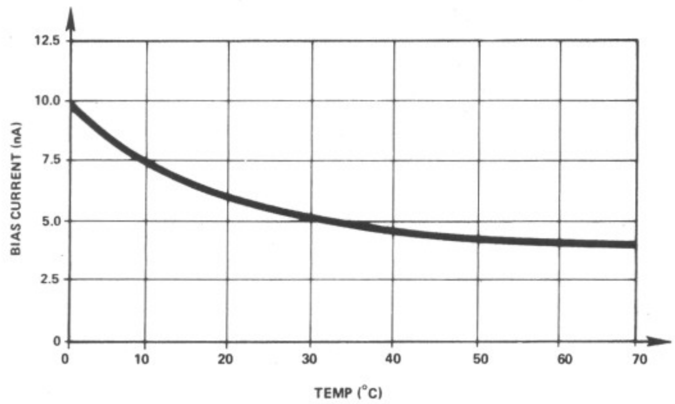


Figure 8. Input Bias Current vs. Temperature

GAIN PERFORMANCE

Most commercially available monolithic op amps have gain characteristics that vary considerably with..........

(1) Offset Nulling
(2) Load Resistance
(3) Supply Voltage

Careful design allows the AD508 to maintain gain well in excess of 10^6, independent of nulling, load or supply voltage.

The gain of the 508 is relatively independent of nulling.

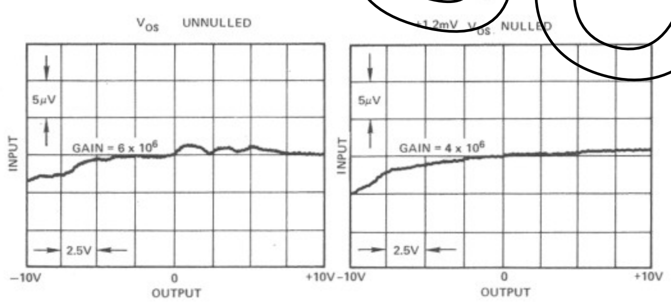


Figure 9. Gain Error Voltage Before and After Nulling the AD508

Load Resistance – The gain of the AD508 is flat with load resistance to 1kΩ loads and below.

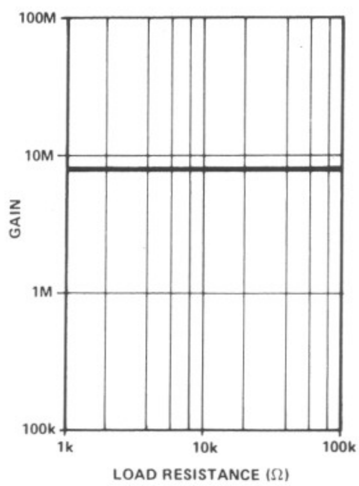


Figure 10. Gain vs. Load Resistance

Supply Voltage – The gain of the AD508 stays well above 1M down to $V_S = \pm 5V$.

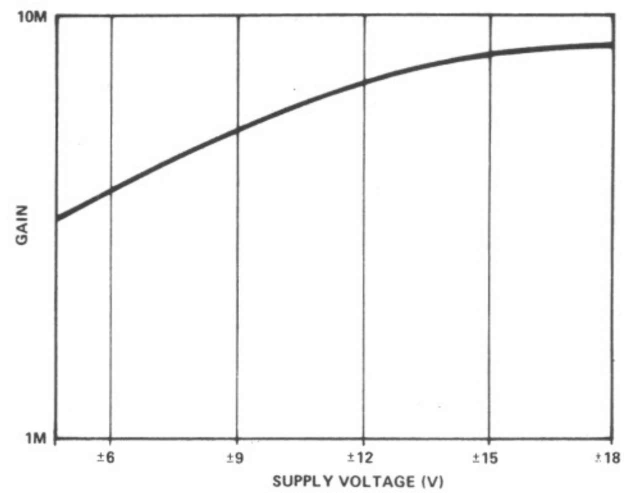


Figure 11. Gain vs. Supply Voltage

NOISE CHARACTERISTICS

An op amp of the caliber of the AD508 must have correspondingly low noise levels if the user is to be assured he will be able to take advantage of its exceptional dc characteristics. Of primary importance in this type of amplifier is the absence of popcorn noise and minimum l/f or "flicker" noise in the 0.01Hz to 10Hz frequency band. Sample noise testing is done on every lot to guarantee that better than 90% of all devices will meet the noise specifications.

Superbeta processing of input transistors achieves extremely low input current noise (see Figure 12). Current noise is typically less than 0.3pA/√Hz at 100Hz and less than 0.2pA/√Hz at 1kHz.

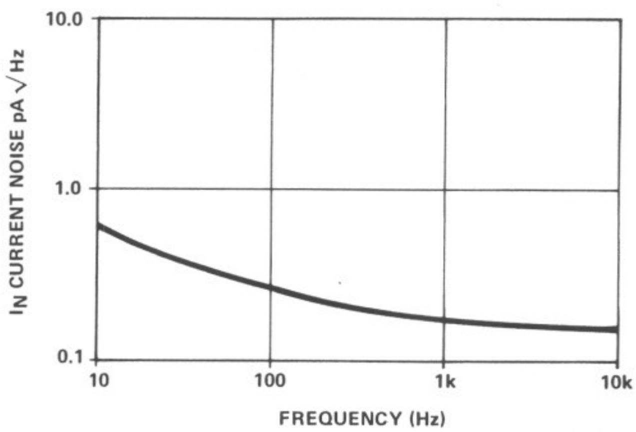


Figure 12. Spot Noise vs. Frequency

The key to success in using the 508 in precision low noise applications is "attention to detail."

Here are a few reminders to help the user achieve optimum noise performance from the AD508.

1. Use metal film resistors in the source and feedback networks.
2. Use fixed resistors instead of potentiometers for nulling or gain setting.

3. Take advantage of the excellent common-mode noise rejection qualities of the 508 by connecting the input differentially.
4. Limit the bandwidth of the system to the minimum possible consistent with the desired response time.
5. Use input guarding to reduce capacitive and leakage noise pickup.
6. Avoid ground loops and proximity to strong magnetic or electro-static fields, etc.

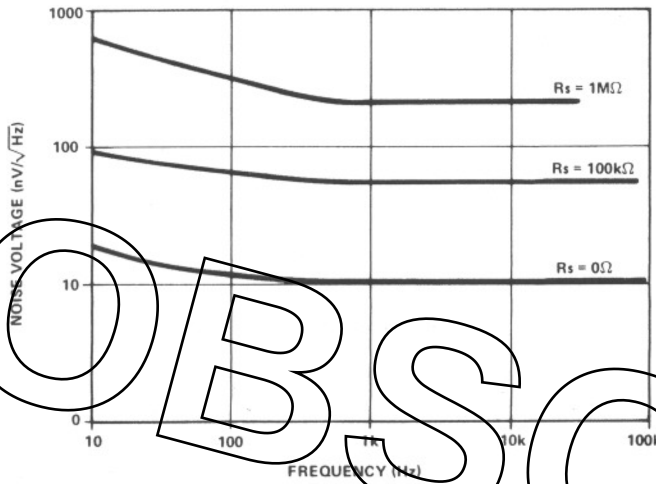


Figure 13. RMS Noise vs. Frequency

DYNAMIC PERFORMANCE

The dynamic performance of the AD508, although comparable to most general purpose op amps, is superior to most low drift op amps. Figure 14 shows the small signal frequency response for both open and closed loop gains for a variety of compensating values. Note that the circuit is completely stable for C_C = 390pF with a −3dB bandwidth of 300kHz; with C_C = 0, the −3dB bandwidth is 50kHz, at a gain of 2000.

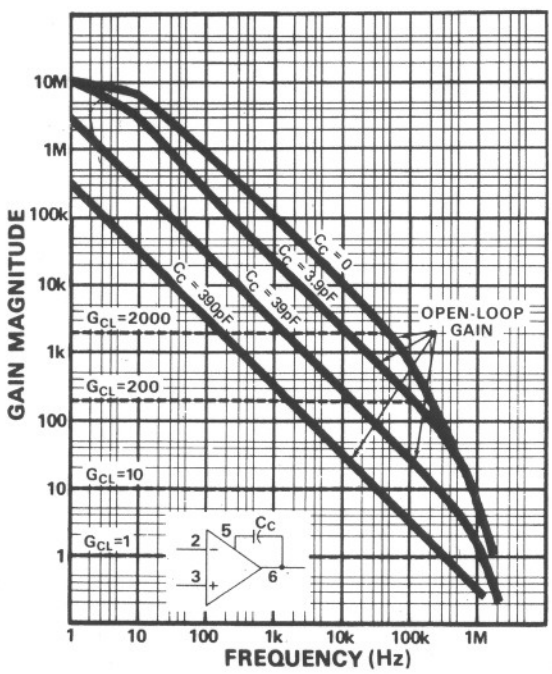


Figure 14. Small Signal Gain vs. Frequency

More important, at unity gain (390pF), full power bandwidth is (Figure 15) 2kHz which corresponds to a 0.12V/μsec slew rate. At a gain of 10 (39pF), it increases to 20kHz, corresponding to 1.2V/μsec, a 20X improvement over the 0.06V/μsec typically found in conventional low drift IC amplifiers at this gain.

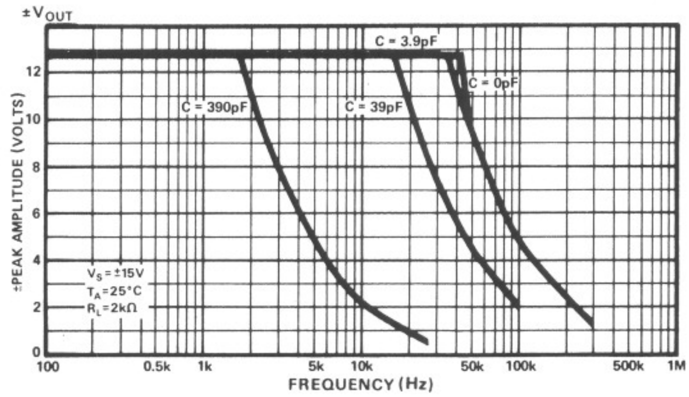


Figure 15. Output Voltage Swing vs. Frequency

Figure 16 shows the voltage follower step response for V_S = ±15V, R_L = 2kΩ, C_L = 200pF and C_c = 390pF.

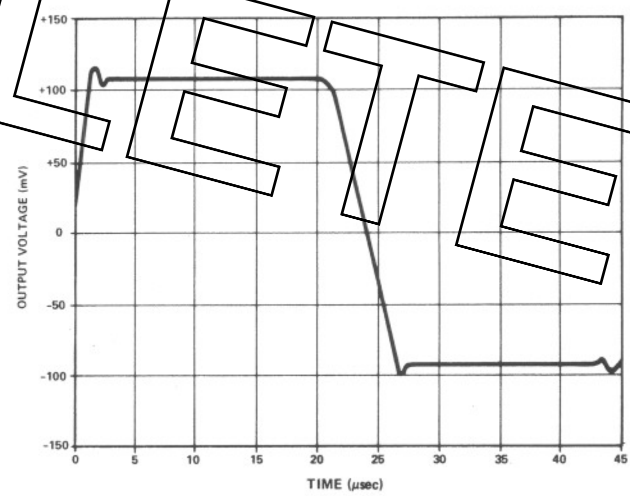


Figure 16. Voltage Follower Step Response

The common mode rejection of the AD508 is typically 120dB, and is shown as a function of frequency in Figure 17.

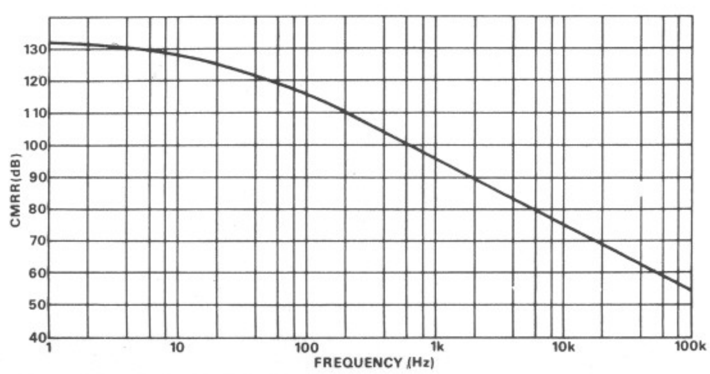


Figure 17. CMRR vs. Frequency

The power supply rejection ratio of the AD508 is shown in Figure 18.

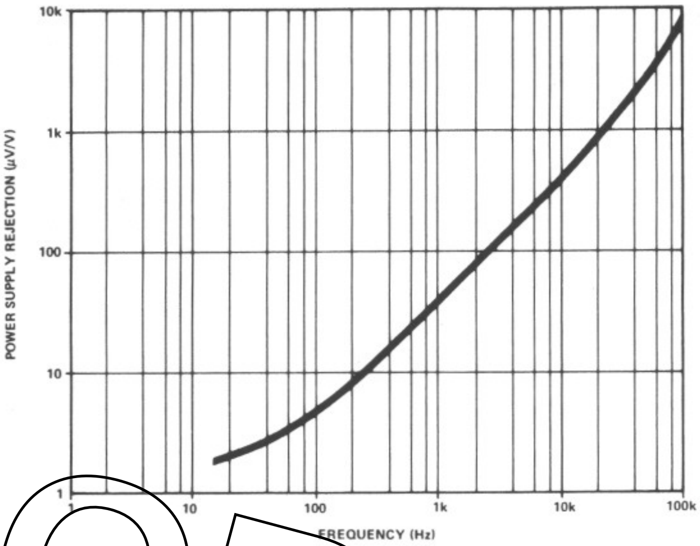


Figure 18. PSRR vs. Frequency

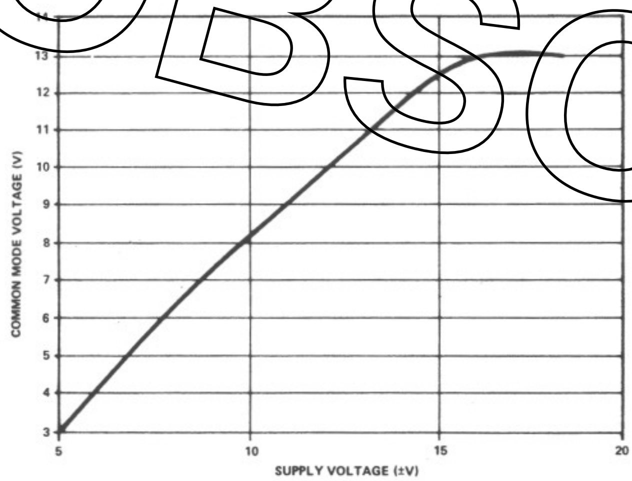


Figure 19. CMV Range vs. Supply Voltage

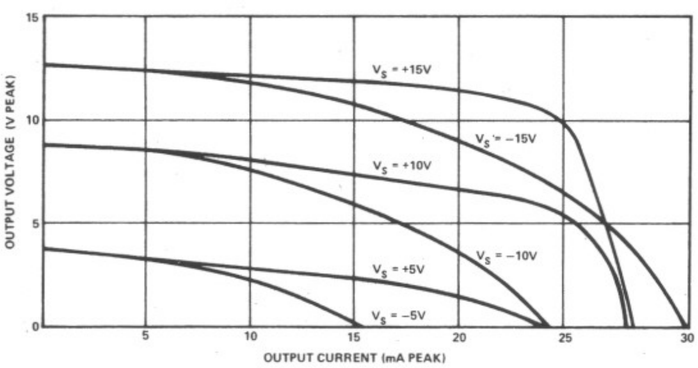
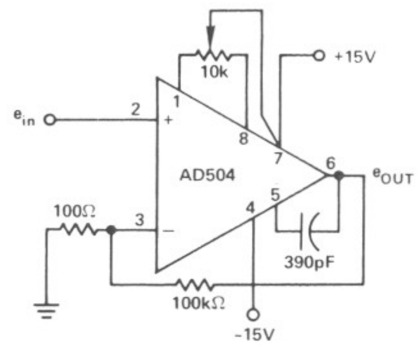


Figure 20. Output Characteristics

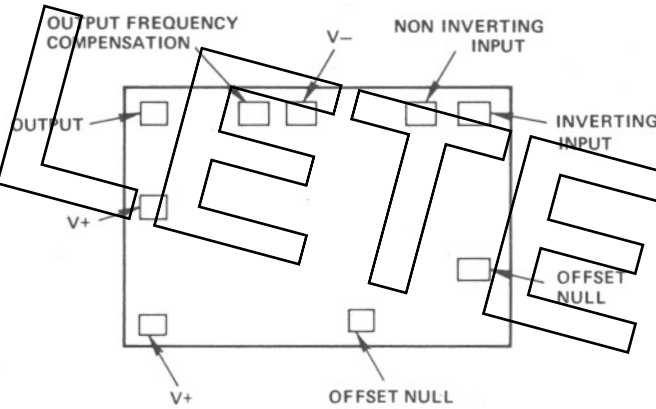
THERMAL PERFORMANCE

Most modular op amps are extremely sensitive to thermal gradients, often resulting in large overshoots, long settling times, and considerable hysteresis. Monolithic technology affords the AD508 significant improvements in this area. For a more complete treatment of the thermal performance of the AD508, the user should consult the AD504 Applications Note.

TYPICAL INVERTING AMPLIFIER CONFIGURATION



AD508 BONDING DIAGRAM



The AD508 is available in chip or wafer form. Because of the critical nature of using unpackaged devices, it is suggested that the factory be contacted for specific information regarding price, delivery and testing.

PHYSICAL DIMENSIONS