Linear Gain Setting Mode: A Detailed Description
by Miguel Usach

INTRODUCTION

Digipots are commonly used to digitally program the gain in an amplifier or set the output voltage of a power supply regulator as shown in Figure 1 and Figure 2.
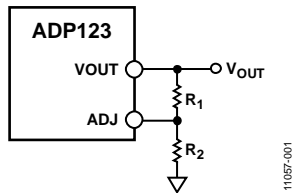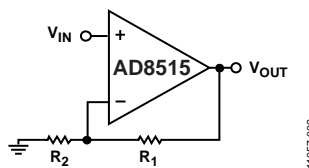
Figure 1. Adjustable Output Voltage LDO

Figure 2. Noninverting Amplifier

In both cases, the transfer equation depends on two different variables, R_1 and R_2, as shown in Equation 1 for the LDO and in Equation 2 for the noninverting amplifier.

$$V_{OUT} = 0.5 \times \left(1 + \frac{R_1}{R_2}\right) \qquad (1)$$

$$V_{OUT} = V_{IN} \times \left(1 + \frac{R_1}{R_2}\right) \qquad (2)$$

Using the digipot in potentiometer mode in these transfer equations is not straightforward since both resistors strings, R_{AW} and R_{WB}, are complementary; in other words, $R_{AW} = R_{AB} - R_{WB}$, as shown in Figure 3.
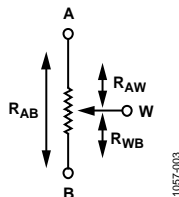
Figure 3. Potentiometer Resistance

If the resistances R_1 and R_2 are directly replaced with a digital potentiometer, then the transfer function becomes logarithmic. Figure 4 shows an example for the LDO.
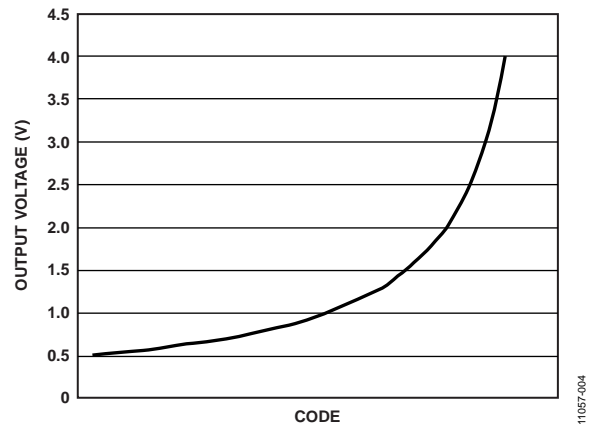
Figure 4. Logarithmic Transfer Function for the LDO

This logarithmic transfer function can be desirable in some applications, such as light or audio control, because the human body is not a linear receptor of those stimuli, but in many electronic applications a linear transfer function is preferred.

LINEARIZING THE OUTPUT

There are three different methods to achieve a linear output directly proportional to the code loaded in the digipot. These three methods are described in detail in the sections that follow.

Use the Digipot in Rheostat Mode

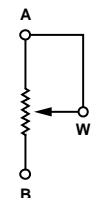The digipot can be used in rheostat mode, where only two terminals are used, as shown in Figure 5.

Figure 5. Rheostat Mode

This mode requires using a discrete resistor in conjunction with the digipot. An example of the noninverting amplifier is shown in Figure 6.
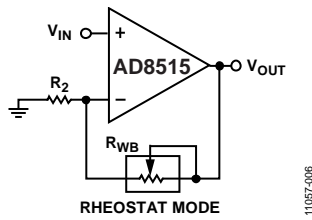

Figure 6. Noninverting Amplifier with Rheostat Control

The main benefit of using this solution is the simplicity in the circuit, the wide output ranges, and the fast settling time. As a trade-off, the overall output error may be quite high because the typical tolerance error in a digipot is around ±20% maximum. Given that R_2 is fixed, this can cause resistor mismatches.

Analog Devices, Inc., offers ±8% and ±1% resistor tolerance error digipots to improve the performance in these configurations as shown in the selection table.

Additionally, the output error can be reduced by using a serial resistor with the digipot, as shown in Figure 7, for the LDO.
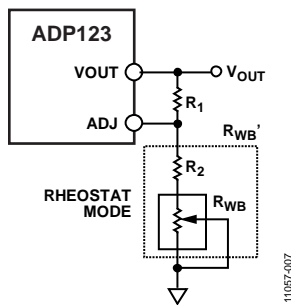

Figure 7. Reduced Tolerance Error with Series Resistance

In this case, to assume the 20% tolerance error is negligible $R_2 >> R_{WB}$; or, in other words, the output error can be improved by reducing the adjustable output gain and increasing the settling time. The final resistance is defined in Equation 3.

$$R_{WB}' = R_2 + R_{WB} \tag{3}$$

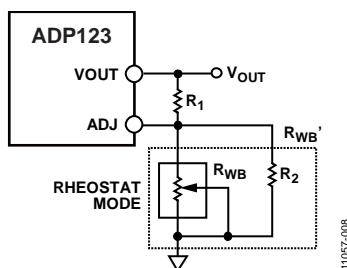A second way to reduce the error is by placing a parallel resistance with the digipot as shown in Figure 8.

Figure 8. Reduced Tolerance Error with Parallel Resistance

In this case, the assumption is that $R_2 << R_{WB}$ due to the nominal end-to-end resistor values, 10 kΩ, 50 kΩ and 100 kΩ.

The consequences are similar to the previous approach, that is, the adjustable output gain is reduced, but, in this case, the settling time is reduced due to the lower R_{WB}' value, as defined in Equation 4.

$$R_{WB}' = \frac{R_2 \times R_{WB}}{R_2 + R_{WB}} \tag{4}$$

The overall parallel resistance value is smaller, thus the resistor noise is lower than the series resistance approach.

As a precaution, remember that the digipot has internal leakage current. If you choose the parallel resistor, R_2, to be small enough to force not enough current through the digipot, the linearity errors, R-INL and R-DNL, could be considerable higher than specified in the data sheet.

Linearize the Potentiometer

Configuring the digipot as a vernier DAC, as shown in Figure 9, the voltages in the Terminal A and Terminal B are limited by the placement of the in-series resistors, R_1 and R_2.
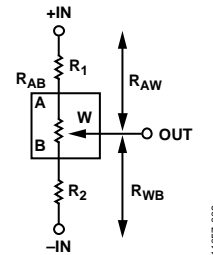

Figure 9. Vernier DAC

The idea of this approach is to reduce the output range resulting in a more linear output, as shown in Figure 10, for two different configurations.
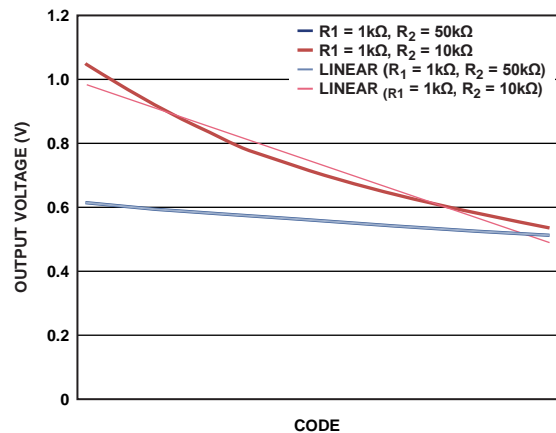

Figure 10. LDO Voltage with a Vernier DAC

This configuration provides lower linearity error than using the digipot in rheostat mode and it results in a lower tempco.

The final resistance between terminals is defined in Equation 5 and Equation 6.

$$R_1' = R_1 + R_{AW} \tag{5}$$

$$R_2' = R_2 + R_{WB} \tag{6}$$

It is recommended to use a low resistor tolerance error digipot, ±8% and ±1%. Note that the higher the tolerance, the greater the mismatch resistance error.

In this case, using a typical 20% resistance tolerance error, a parallel resistor should be used with the digipot to reduce the overall error as shown in Figure 11.
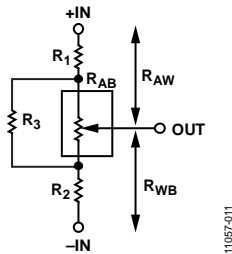

Figure 11. Reduced Tolerance Error in Vernier DAC

Again, it is important to consider the effect of the leakage current in this configuration. Selecting a low parallel value could force the current through R_3.

To calculate the final resistance between terminals can be quite complex, thus the best approach is to use a Y-Δ transform as shown in Figure 12.
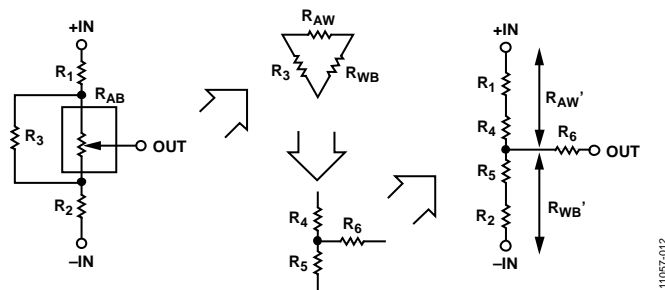

Figure 12. Y-Δ Transform

where:

$$R_4 = \frac{R_{AW} x R_3}{R_{AB} + R_3} \qquad (7)$$

$$R_5 = \frac{R_{WB} x R_3}{R_{AB} + R_3} \qquad (8)$$

$$R_{AW}' = R_1 + R_4 \qquad (9)$$

$$R_{BW}' = R_2 + R_5 \qquad (10)$$

R_6 should be connected to a high impedance input so that the effect of this resistance can be considered negligible.

Enable the Linear Gain Setting Mode

In linear gain setting mode, the internal resistors strings, R_{AW} and R_{WB}, are dependant. The newly patented architecture implemented in the AD5144, AD5142, AD5124A, and AD5141 improves flexibility, allowing independent programming of the value for each string, R_{AW} and R_{WB}, as shown in Figure 13.
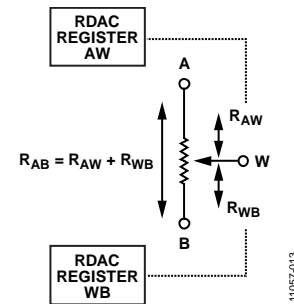

Figure 13. Linear Gain Setting Mode

Enabling this mode, the output voltage can be linear, fixing the value of one resistor string, that is, R_{WB}, and setting the other string, R_{AW}. The mode of operation is similar to using the digipot in rheostat mode in conjunction with a discrete resistor, but in this case the overall tolerance error is below 1% without using any external parallel or series resistance combination.

This is achieved because the gain is set by the resistance ratios, and the overall resistor tolerance error, as is common in both string arrays, can be disregarded.

Figure 14 shows an example of sweeping R_{AW} from zero scale to full scale, fixing R_{WB} at midscale for a 10 kΩ digipot. Analyzing the plot in detail, at lower codes when the resistances, R_{AW} or R_{WB}, are small, the mismatch becomes higher than ±1%. This is due to an error added by the non-negligible effect in the internal CMOS switches resistance.

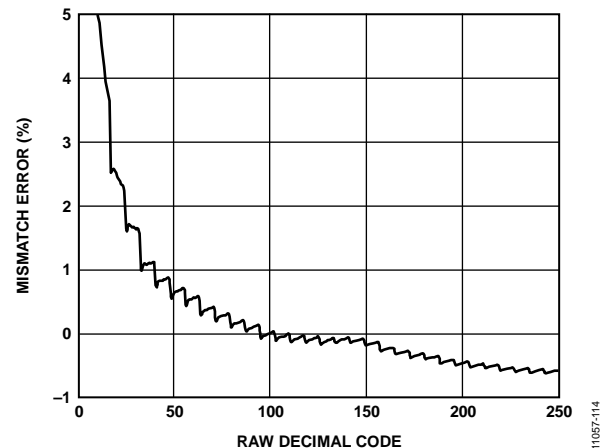*Figure 14. 10 kΩ Resistance Match Error*

The switches effect can be cancelled by selecting codes higher than quarter scale.

Enabling linear setting mode, the maximum resistance between Terminal A and Terminal B can be set to double the nominal digipot resistance. In other words, if the R_{AB} resistance is 10 kΩ in potentiometer mode, in lineal setting mode when programming both string resistors at full scale, the R_{AB} = 20 kΩ.

Similar performance can be achieved by using a dual channel digipot, but this solution increases the cost and size with degradation in the settling time.

Another additional benefit of using this configuration is the reduced temperature coefficient, as shown in Figure 14. In this case, the importance is not the absolute tempco for each string resistor, but the difference between the tempco for the specific codes that define the ratio.
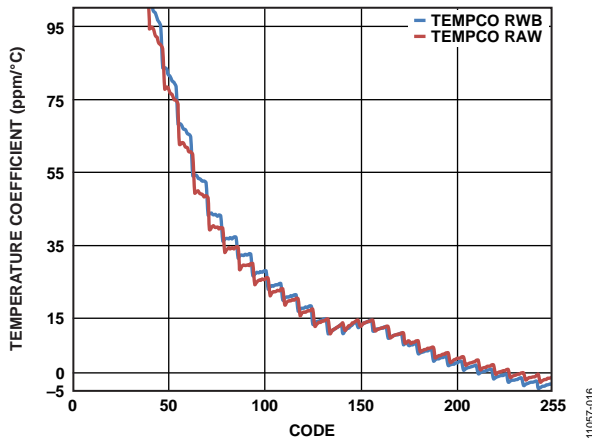

Figure 15. 10 kΩ Resistance Tempco

Take, for example, the circuit in Figure 16. Choosing a gain of 3, the codes ratio is defined in equation 11.
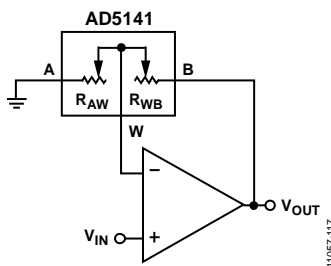

Figure 16. Noninverting Amplifier and AD5141 in Linear Gain Setting Mode

$$Gain = 1 + \frac{R_{WB}}{R_{AW}} \Rightarrow 2 \times R_{AW} = R_{WB} \qquad (11)$$

Fixing the R_{WB} code to 250, the R_{AW} code is 125. As a rough estimate, the overall error due tempco over the full temperature range is defined as,

R_{AW} at code 125 is 20 ppm/C

R_{WB} at code 250 is −2 ppm/C

The gain error due to R_{AW} is

$$Error_{RAW} = \frac{\left| Gain - Gain_{RAW} \right|}{Gain} =$$

$$= \frac{\left| 3 - \left(1 + \dfrac{R_{WB}(250)}{R_{AW}(125) + \dfrac{20 \times R_{AW}(125) \times 100}{1e6}} \right) \right|}{3} =$$

$$= \frac{\left| 3 - \left(1 + \dfrac{9765.625}{4882.8125 + 9.765} \right) \right|}{3} = 0.13\%$$

The gain error due to R_{WB} is

$$Error_{RBW} = 0.04\%$$

Thus, the total error is defined as,

$$GAIN_{ERROR} = Error_{RAW} + Error_{RWB} = 0.17\%$$

Similar to the resistance match error, at lower codes the switch resistance tempco is dominant, but the effect is minimizing at higher codes.

If a lower error vs. temperature is required, a higher end-to-end resistance value needs to be used as shown in Figure 17 for 100 kΩ. In this particular case, the tempco is much more flat in all the code range, so the error expected should be smaller.
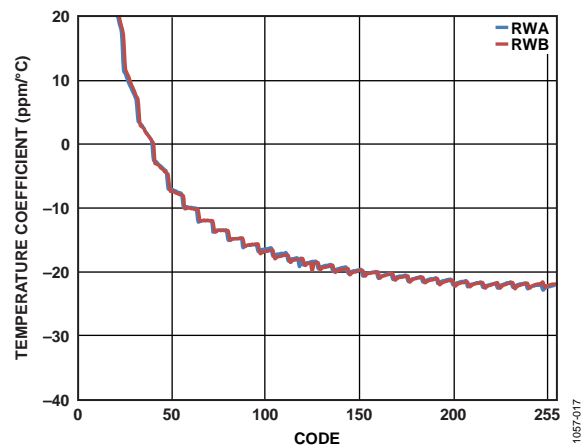

Figure 17. 100 kΩ Resistance Tempco

REVISION HISTORY

8/13—Rev. 0 to Rev. A

12/12—Revision 0: Initial Version

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