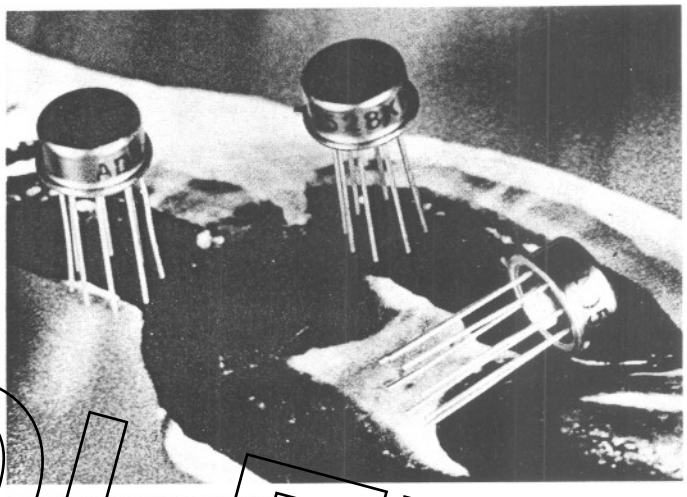
High Speed, Precision, FET-Input Operational Amplifier

AD528

FEATURES
- High Slew Rate: 70V/μs
- Wide Bandwidth: 10MHz
- Low Bias Current: 15pA max (AD528K, S)
- Low Offset Voltage: 1mV max (AD528K, S)
- Inverting and Non-Inverting Operation



PRODUCT DESCRIPTION

The AD528J, AD528K and AD528S are high speed, precision FET-input operational amplifiers combining the advantages of very high slew rate and wide bandwidth with the ultra-low input currents only available with FET-input designs. The devices are internally compensated for unity gain applications with a 60° phase margin to insure stability, a minimum unity gain slew rate of 50V/μs, and a typical bandwidth of 10MHz. In addition, in inverting applications external feed forward compensation may be added to increase the slew rate to over 100V/μs, and nearly double the bandwidth. If desired, settling time to 0.1% can be reduced to under 1μs with a single external capacitor.

The AD528 offers the user dc performance previously unavailable in conventional high speed designs. The devices offer maximum bias currents under 15pA, laser-trimmed offset voltages below 1mV, and offset voltage drifts below 25μV/°C.

The high slew rate, wide bandwidth, and low input currents of the AD528 make it ideal for use in sample-hold circuits, A/D, D/A and sampled data systems, and high speed integrators. The AD528 is supplied in the TO-99 package. The AD528J and AD528K are specified for operation over the 0 to +70°C temperature range; the AD528S for operation from −55°C to +125°C.

PRODUCT HIGHLIGHTS

1. The AD528, guaranteeing bias currents of 15pA, offers the user the lowest input current available in a high speed design. In addition, at Analog Devices.....
   - all IC FET op amps meet their published input bias current specs after full warm-up. Conventional high speed IC testing does not allow for self-heating of the chip due to internal power dissipation under operating conditions;
   - all IC FET op amps meet their published input bias current specs at either input. Conventional IC FET op amps generally specify bias current as the average of the two input currents.
2. The AD528 offers the user excellent high speed performance and flexibility.
   - Internal compensation for all gains.
   - Capability to increase slew rate to over 100V/μs and double the bandwidth by an external feed forward technique.
   - Capability to reduce settling time to under 1μs to 0.1% with a single external capacitor.
   - Differential input capability.
3. The phase margin of the AD528, uncompensated at the unity gain crossover frequency, is 60° providing unconditional stability for all applications.

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SPECIFICATIONS (typical @ +25°C and ±15V dc unless otherwise specified)

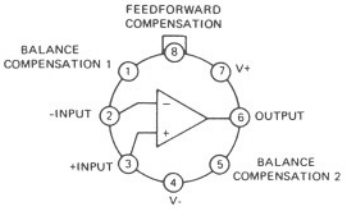
MODEL	AD528JH	AD528KH	AD528SH
OPEN LOOP GAIN			
$R_L \geq 2k\Omega$, $V_O = \pm 10V$	25,000 min (100,000 typ)	50,000 min (100,000 typ)	**
@ T_A = min to max	25,000 min	25,000	**
OUTPUT CHARACTERISTICS			
Voltage @ $R_L \geq 2k\Omega$, T_A = min to max	±10V min	*	*
Current @ $V_O = \pm 10V$	±10mA	*	*
Short Circuit Current	25mA	*	*
FREQUENCY RESPONSE			
Unity Gain, Small Signal	10MHz	*	*
Slew Rate, Unity Gain	50V/μs min (70V/μs typ)	*	*
Settling Time to 0.1% (Single Capacitor Compensation)	800ns	*	*
Phase Margin, Uncompensated at Unity Gain Crossover Frequency	60°	*	*
INPUT OFFSET VOLTAGE			
Initial, $R_S \leq 10k\Omega$	3mV max (1mV typ)	1mV max (0.3mV typ)	**
@ T_A = min to max	5mV max	2mV max	3mV max
Avg vs Temp, T_A = min to max	50μV/°C max (25μV/°C typ)	25μV/°C max (10μV/°C typ)	**
Avg vs Supply, T_A = min to max	70dB min (90dB typ)	80dB min (90dB typ)	**
INPUT BIAS CURRENT			
Warmed up at 25°C	30pA max (10pA typ)	15pA max (5pA typ)	**
INPUT OFFSET CURRENT			
Warmed up at 25°C	5pA max	2pA max	**
INPUT NOISE			
Voltage, 0.1 to 10Hz	5μV(p-p)	*	*
INPUT IMPEDANCE			
Differential	$10^{12}\Omega \| 6pF$	*	*
INPUT VOLTAGE RANGE			
Differential (Note 1)	±20V	*	*
Common Mode, max safe	$\pm V_S$	*	*
Common Mode Rejection Ratio	70dB min (90dB typ)	80dB min (90dB typ)	*
POWER SUPPLY			
Rated Performance	±15V	*	*
Operating	±(5 to 20)V	*	*
Current, Quiescent	7mA max (5mA typ)	*	*
TEMPERATURE RANGE			
Rated Performance	0 to +70°C	*	−55°C to +125°C
Storage	−65°C to +150°C	*	*

*Specifications same as AD528J.
**Specifications same as AD528K.

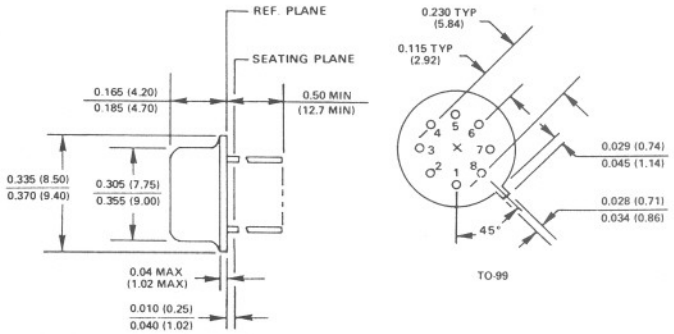
NOTE 1. Defined as voltage between inputs such that neither exceeds ±10V from ground.

Specifications and prices subject to change without notice.

PIN CONFIGURATION
Top View



OUTLINE DIMENSIONS
Dimensions shown in inches and (mm).



USING THE AD528

When designing with the AD528, the user should be aware of the necessity to adhere to the precautions normally observed when using FET op amps, as well as those observed when using fast bipolar designs.

THE AD528 AS A HIGH SPEED OP AMP

Phase Margin. The AD528 is internally compensated for unconditional stability at all gains. Perhaps one of the most meaningful ways to express the stability of a closed loop amplifier is in terms of its phase margin. Phase margin is measured at the frequency where the open loop gain of the amplifier becomes unity or 0dB. It is the additional amount of phase shift that, if introduced in the loop, would make the loop unstable. The AD528 has been designed for a 60° phase margin at the unity gain crossover frequency for absolute stability and absence of ringing and overshoot. Note the transient response of the AD528 in Figure 1. Note also in Figure 2 that the phase shift at 10MHz, the unity gain crossover frequency, is 120°, representing 60° of phase margin.

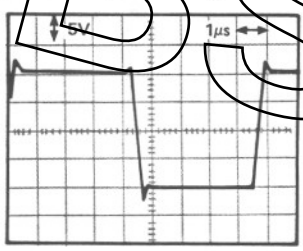


Figure 1. Transient Response of the AD528

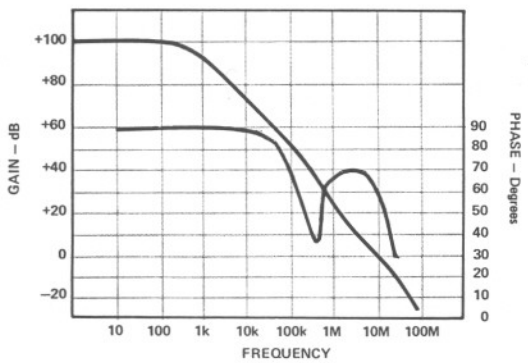


Figure 2a. Small Signal Amplitude and Phase Response

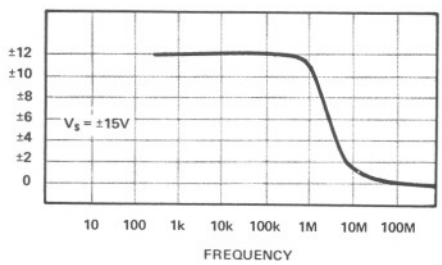


Figure 2b. Large Signal Amplitude Response

Connecting the AD528. The connection scheme employed when using the AD528 is considerably more important than for low frequency, general purpose amplifiers. The primary purpose of the 0.1µF bypass capacitors shown in Figure 3 is to convert the distributed high frequency ground to a lumped single point (the V+ point). The V+ to V– 0.1µF capacitor equalizes the supply grounds, while the 0.1µF capacitor from V+ to signal ground should be returned to signal common. This signal common, which is bypassed to pin 7, is defined as that point at which the input signal source, the feedback network, and the return side of the load are joined to the power common.

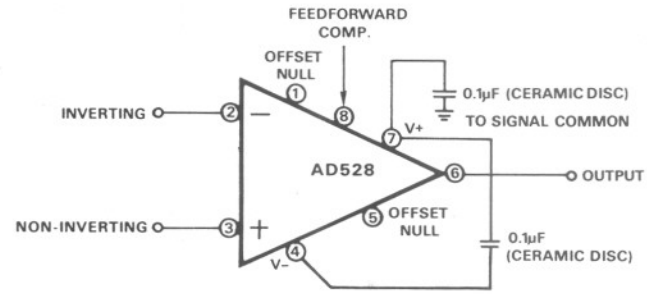


Figure 3. General Purpose Connection Diagram

Note that the diagram shows each individual capacitor directly connected to the appropriate terminal. In addition, it is suggested that all connections be made short and direct, and as physically close to the can as possible, so that the length of any conducting path shared by external components will be minimized.

Neutralizing Input Capacitance. The common mode capacitance at each input is approximately 6pF. If large input or feedback resistors are used, as is often the case with FET op amps, a 6–10pF capacitor should be added in parallel with the larger resistor to cancel the pole which is introduced by the input capacitance. For precision, fast settling applications, it may be desirable to use a trimmer capacitor to optimize the response.

Capacitive Loading. The AD528 can drive 100pF capacitive loads; for larger capacitive loads, an isolation resistor, as shown in Figure 4 is recommended.

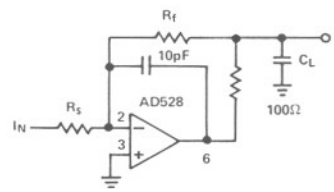


Figure 4. Isolating a Capacitive Load Up To 500pF

THE AD528 AS A FET OP AMP

1. The AD528 meets its published input bias current and offset voltage spec after full warm-up. Conventional IC testing does not pick up self-heating of the chip due to internal power dissipation. This can cause up to an 8X increase in bias and offset currents.
2. The input bias current of the AD528 is specified as a maximum at either input, not as an average of the bias current at both terminals.
3. The gain of many IC FET op amps decreases by an order of magnitude when nulled. The AD528 guarantees a minimum gain with V_{OS} nulled and unnulled.

4. The laser-trimmed offset voltages below 1mV preclude the necessity for further nulling in most applications. If any small adjustments are required, there will be a very minimal effect on the offset drift coefficient.

THE FLEXIBILITY OF THE AD528

MINIMUM SETTLING TIME APPLICATIONS

For applications where a minimum settling time is desired, the settling time of the AD528 may be reduced significantly by employing the compensation scheme suggested in Figure 5.

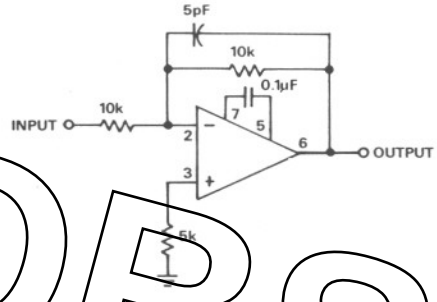


Figure 5. Minimum Settling Time Configuration

Using the 0.1µF capacitor from Pin 5 to V+ (Pin 7), the settling time to 0.1% is reduced from 2µs to 800ns.

HIGHER BANDWIDTH OR HIGHER SLEW RATE APPLICATIONS

For applications where higher bandwidth is desired, the bandwidth of the AD528 may be increased to nearly 25MHz by using the feedforward technique shown in Figure 6.

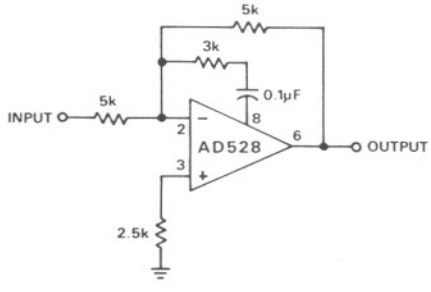


Figure 6. High Bandwidth Configuration

For applications where higher slew rate is desired, the slew rate of the AD528 may be nearly doubled using the technique shown in Figure 7.

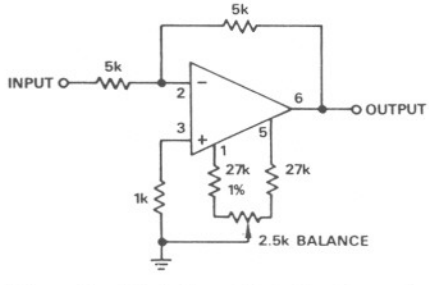


Figure 7. High Slew Rate Configuration

Note that the techniques in Figures 6 and 7 may be used in conjunction with each other to both double the bandwidth to 25MHz and increase the slew rate to 100–140V/µs.

NOISE PERFORMANCE OF THE AD528

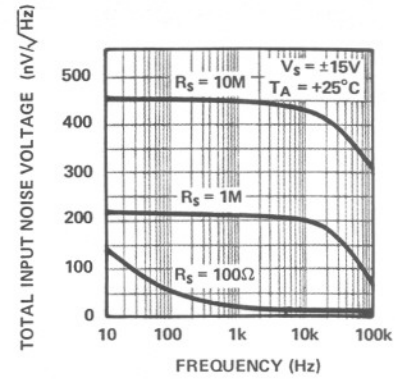


Figure 8. Total Input Noise Voltage vs. Frequency

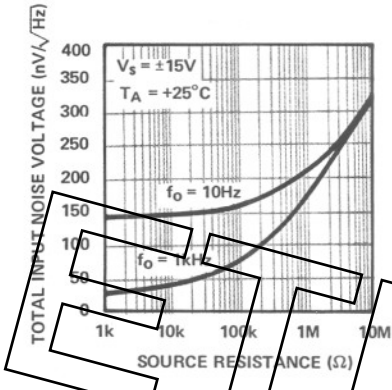
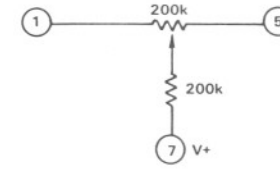


Figure 9. Total Input Noise vs. Source Resistance

NULLING THE AD528



OTHER IC HIGH SPEED AMPLIFIERS AVAILABLE

AD507	35MHz Gain Bandwidth Slew Rate of 25V/µs min Bias Current of 15nA max Offset Voltage Drift of 15µV/°C max
AD509	Settles to 0.01% in 1µs Settles to 0.1% in 200ns Slew Rate of 100V/µs min
AD518	Slew Rate of 50V/µs min Internally Compensated For All Gains Low Cost
AD544	Slew Rate of 13V/µs Bias Current of 25pA max Offset Voltage of 0.5mV max Offset Voltage Drift of 5µV/°C max