Dual, Current Output, Serial Input, 16-Bit DAC

Known Good Die

AD5545-KGD

FEATURES

- 16-bit resolution
- ±1 LSB DNL monotonic
- ±1 LSB INL
- 2 mA full-scale current ± 20%, with V_{REF} = 10 V
- 0.5 µs settling time
- 2-quadrant reference multiplying 6.9 MHz bandwidth
- Zero or midscale power-up reset
- Zero or midscale dynamic reset
- 3-wire interface
- 23-pad bare die package

APPLICATIONS

- Automatic test equipment
- Instrumentation
- Digitally controlled calibration
- Industrial control programmable logic controllers (PLCs)
- Programmable attenuator

GENERAL DESCRIPTION

The AD5545-KGD is a 16-bit, current output, digital-to-analog converter (DAC) designed to operate from a 4.5 V to 5.5 V supply range.

An external reference is needed to establish the full-scale output current. An internal feedback resistor (R_{FB}) enhances the resistance and temperature tracking when combined with an external op amp to complete the current to voltage (I to V) conversion.

A serial data interface offers high speed, 3-wire microcontroller compatible inputs using serial data input (SDI), clock (CLK), and chip select ($\overline{CS}$). The $\overline{LDAC}$ function allows simultaneous update operation. The internal reset logic allows power-on reset and dynamic reset at either zero or midscale, depending on the state of the MSB pin.

The AD5545-KGD is packaged in a 23-pad bare die package and can be operated from −40°C to +85°C.

Known Good Die (KGD): these die are fully guaranteed to data sheet specifications.

Additional application and technical information can be found in the AD5545 data sheet.

FUNCTIONAL BLOCK DIAGRAM

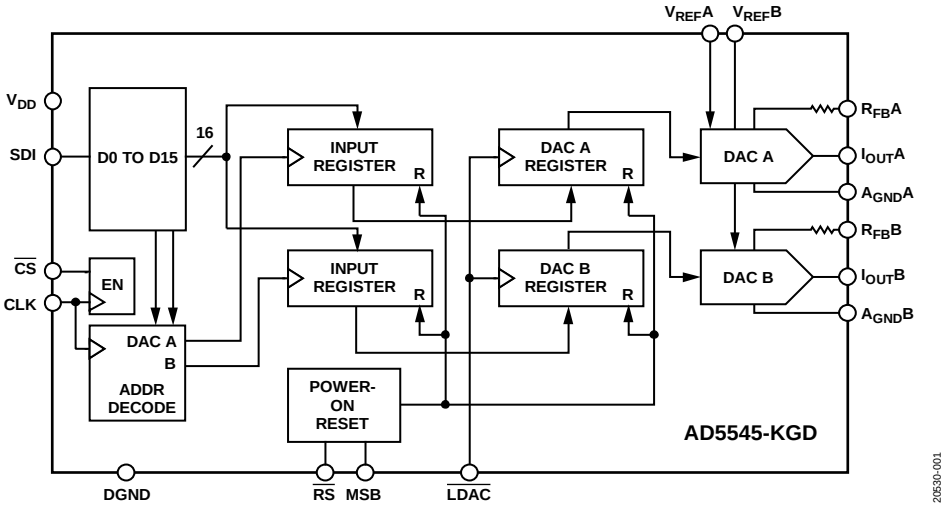

Figure 1.

Rev. 0

Document Feedback

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TABLE OF CONTENTS

REVISION HISTORY

11/2019—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

V_{DD} = 5 V ± 10%, I_{OUTx} = virtual GND, GND = 0 V, reference voltage (V_{REF}) = 10 V, T_A = full operating temperature range, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
STATIC PERFORMANCE[1]						
Resolution	N	1 LSB = $V_{REF}/2^{16}$ = 153 µV when V_{REF} = 10 V			16	Bits
		1 LSB = $V_{REF}/2^{14}$ = 610 µV when V_{REF} = 10 V			14	Bits
Relative Accuracy	INL				±1	LSB
Differential Nonlinearity	DNL	Monotonic			±1	LSB
Output Leakage Current	I_{OUT}	Data = 0x0000, T_A = 25°C			10	nA
		Data = 0x0000, T_A = T_A maximum			20	nA
Full-Scale Gain Error	G_{FSE}	Data = full scale		±1	±4	mV
Full-Scale Temperature Coefficient[2]	TCV_{FS}			1		ppm/°C
REFERENCE INPUT						
Reference Voltage Range	V_{REF}		−12		+12	V
Input Resistance	R_{REF}			5		kΩ
Input Capacitance[2]	C_{REF}			5		pF
ANALOG OUTPUT						
Output Current	I_{OUT}	2 mA full-scale current ± 20%, with V_{REF} = 10 V		2		mA
Output Capacitance[2]	C_{OUT}	Code dependent		200		pF
LOGIC INPUTS AND OUTPUT						
Logic Input Low Voltage	V_{IL}				0.8	V
Logic Input High Voltage	V_{IH}		2.4			V
Input Leakage Current	I_{IL}				10	µA
Input Capacitance[2]	C_{IL}				10	pF
INTERFACE TIMING[2, 3]		See Figure 2				
Clock Input Frequency	f_{CLK}				50	MHz
Clock Width High	t_{CH}		10			ns
Clock Width Low	t_{CL}		10			ns
$\overline{CS}$ to Clock Setup	t_{CSS}		0			ns
Clock to $\overline{CS}$ Hold	t_{CSH}		10			ns
Data Setup	t_{DS}		5			ns
Data Hold	t_{DH}		10			ns
$\overline{LDAC}$ Setup	t_{LDS}		5			ns
Hold	t_{LDH}		10			ns
$\overline{LDAC}$ Width	t_{LDAC}		10			ns
SUPPLY CHARACTERISTICS						
Power Supply Range	V_{DD}		4.5		5.5	V
Positive Supply Current	I_{DD}	Logic inputs = 0 V			10	µA
Power Dissipation	P_{DISS}	Logic inputs = 0 V			0.055	mW
Power Supply Sensitivity	PSS	ΔV_{DD} = ±5%			0.006	%/%

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
AC CHARACTERISTICS[4]						
Output Voltage Setting Time	t_S	To ±0.1% full scale, data = zero scale to full scale to zero scale		0.5		µs
Reference Multiplying Bandwidth[5]		V_{REF} = 100 mV rms, data = full scale, C1 = 5.6 pF		6.9		MHz
DAC Glitch Impulse	Q	V_{REF} = 0 V, data = midscale minus 1 to midscale		–2		nV-sec
Feedthrough Error	V_{OUT}/V_{REF}	Data = zero scale, V_{REF} = 100 mV rms, f = 1 kHz, same channel		–81		dB
Digital Feedthrough	Q	$\overline{CS}$ = logic high and f_{CLK} = 1 MHz		7		nV-sec
Total Harmonic Distortion	THD	V_{REF} = 5 V p-p, data = full scale, f = 1 kHz to 10 kHz		–104		dB
Analog Crosstalk	C_{TA}	V_{REF}B = 0 V, measure DAC B voltage output (V_{OUTB}) with V_{REF}A = 5 V p-p sine wave, data = full scale, f = 1 kHz to 10 kHz		–95		dB
Output Spot Noise Voltage	e_N	f = 1 kHz, bandwidth = 1 Hz		12		nV/√Hz

[1] All static performance tests (except I_{OUT}) are performed in a closed-loop system using an external precision OP1177 I to V converter amplifier. The AD5545-KGD R_{FB}x pad is tied to the amplifier output. Typical values represent average readings measured at 25°C.
[2] These parameters are guaranteed by design and not subject to production testing.
[3] All input control signals are specified with $t_R = t_F$ = 2.5 ns (10% to 90% of 3 V) and timed from a voltage level of 1.5 V.
[4] All ac characteristic tests are performed in a closed-loop system using an AD8038 I to V converter amplifier and the AD8065 for the THD specification. {see note on previous page}
[5] C1 is an optional compensation capacitor. See the AD5545 data sheet for more information.

Timing Diagram

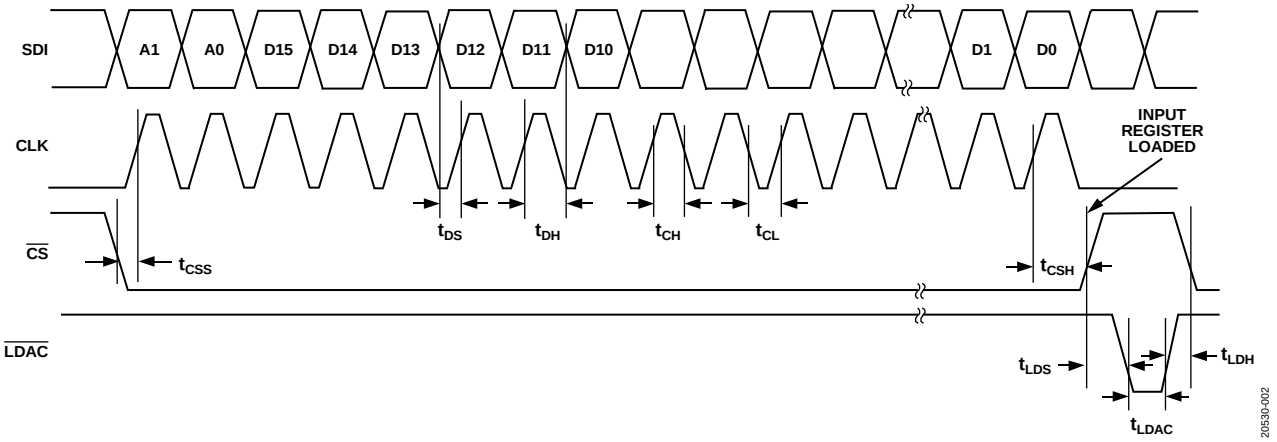

Figure 2. 18-Bit Data Word Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
V_{DD} to GND	−0.3 V to +8 V
$V_{REF}x$ to GND	−18 V to +18 V
Logic Inputs to GND	−0.3 V to +8 V
V_{IOUTx}[1] to GND	−0.3 V to V_{DD} + 0.3 V
Input Current to Any Pin except Supplies	±50 mA
Maximum Junction Temperature (T_J max)	150°C
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature	JEDEC industry standard
Soldering	J-STD-020

[1] V_{IOUTx} is the voltage at the I_{OUTx} pin.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

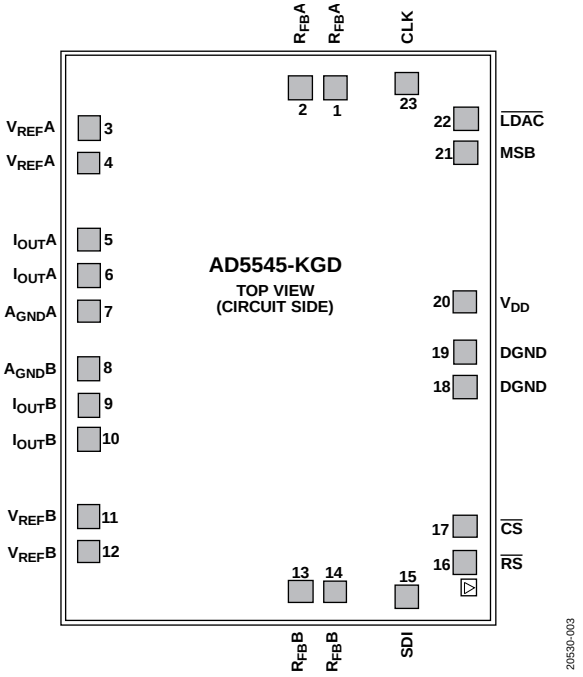

Figure 3. Pad Configuration

Table 3. Pad Function Descriptions

Pad No.	X-Axis (µm)	Y-Axis (µm)	Mnemonic	Description
1	232	1003	$R_{FB}A$	DAC A Feedback Resistor Connection. Establish the voltage output for DAC A by connecting this pin to an external amplifier output.
2	92	1003	$R_{FB}A$	DAC A Feedback Resistor Connection. Establish the voltage output for DAC A by connecting this pin to an external amplifier output.
3	−745	702	$V_{REF}A$	DAC A Reference Voltage Input Terminal. $V_{REF}A$ establishes the DAC A full-scale output voltage. This pin can be tied to the V_{DD} pin.
4	−745	842	$V_{REF}A$	DAC A Reference Voltage Input Terminal. $V_{REF}A$ establishes the DAC A full-scale output voltage. This pin can be tied to the V_{DD} pin.
5	−745	257	$I_{OUT}A$	DAC A Current Output.
6	−745	397	$I_{OUT}A$	DAC A Current Output.
7	−745	115	$A_{GND}A$	DAC A Analog Ground.
8	−745	−115	$A_{GND}B$	DAC B Analog Ground.
9	−745	−397	$I_{OUT}B$	DAC B Current Output.
10	−745	−257	$I_{OUT}B$	DAC B Current Output.
11	−745	−702	$V_{REF}B$	DAC B Reference Voltage Input Terminal. $V_{REF}B$ establishes DAC B full-scale output voltage. This pin can be tied to the V_{DD} pin.
12	−745	−842	$V_{REF}B$	DAC B Reference Voltage Input Terminal. $V_{REF}B$ establishes DAC B full-scale output voltage. This pin can be tied to the V_{DD} pin.
13	232	−1003	$R_{FB}B$	DAC B Feedback Resistor Connection. Establish the voltage output for DAC B by connecting this pin to an external amplifier output.
14	92	−1003	$R_{FB}B$	DAC B Feedback Resistor Connection. Establish the voltage output for DAC B by connecting this pin to an external amplifier output.
15	513	−1022	SDI	Serial Data Input. Input data loads directly into the shift register.
16	745	−881	$\overline{RS}$	Reset Pin, Active Low Input. Input registers and DAC registers are set to all 0s or midscale. Register data = 0x0000 when MSB = 0. Register data = 0x8000 when MSB = 1.

Pad No.	X-Axis (µm)	Y-Axis (µm)	Mnemonic	Description
17	745	−741	$\overline{CS}$	Chip Select, Active Low Input. $\overline{CS}$ disables the shift register loading when high. The AD5545-KGD transfers serial register data to the input register when $\overline{CS}$ or $\overline{LDAC}$ returns high, which does not affect $\overline{LDAC}$ operation.
18	745	−46	DGND	Digital Ground Pin.
19	745	−186	DGND	Digital Ground Pin.
20	745	152	V_{DD}	Positive Power Supply Input. The specified range of operation is 5 V ± 10%.
21	745	741	MSB	Zero Scale or Midscale Output Setting. MSB sets the output to either 0 or midscale during a reset pulse ($\overline{RS}$) or at system power-on. The output equals zero scale when MSB = 0 and midscale when MSB = 1. The MSB pin can also be tied permanently to ground or V_{DD}.
22	745	881	$\overline{LDAC}$	Load DAC Register Strobe, Level Sensitive Active Low. $\overline{LDAC}$ transfers all input register data to DAC registers. $\overline{LDAC}$ is an asynchronous active low input. See the AD5545 data sheet for operation.
23	513	1022	CLK	Clock Input. The positive edge clocks data into the shift register.

OUTLINE DIMENSIONS

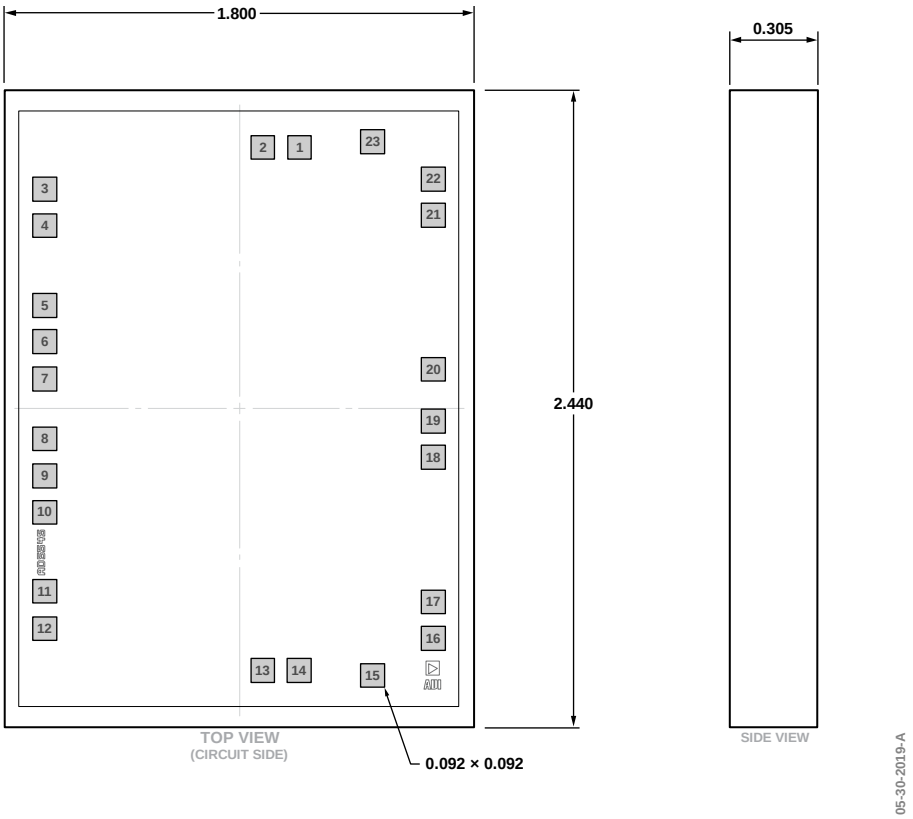

Figure 4. 23-Pad Bare Die [CHIP]
(C-23-2)
Dimensions shown in millimeters

DIE SPECIFICATIONS AND ASSEMBLY RECOMMENDATIONS

Table 4. Die Specifications

Die Specifications Parameter	Value	Unit
Chip Size	1690 × 2280	µm
Scribe Line Width	110 × 160	µm
Die Size	1800 × 2440	µm
Thickness	305	µm
Backside	Backside adhesion/backside bias	Not applicable
Passivation	Polyimide	Not applicable
Thickness	18	µm
Bond Pads (Minimum)	92 × 92	µm
Bond Pad Composition	Aluminum silicon (AlSi) (1.0%), copper (Cu) (0.5%)	Not applicable

Table 5. Assembly Recommendations

Assembly Component	Recommendation
Die Attach	Epoxy dispense
Bonding Method	Thermosonic gold ball bonding
Bonding Sequence	Bond Pad 1 ($R_{FB}A$) first

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD5545-KGD-WP	−40°C to +85°C	23-Pad Bare Die [CHIP], Waffle Pack	C-23-2