ANALOG DEVICES

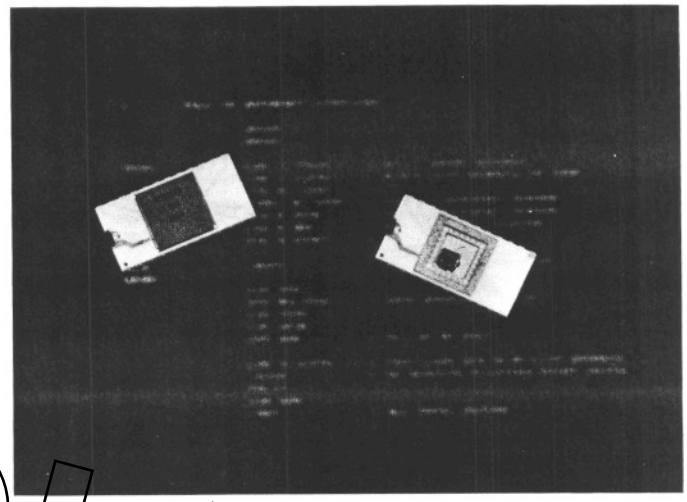
OLD

Complete High Speed 12-Bit Monolithic D/A Converter

AD565

FEATURES

- Single Chip Construction
- Very High Speed: Settles to 1/2LSB in 200ns
  Full Scale Switching Time: 30ns
- High Stability Buried Zener Reference on Chip
- Monotonicity Guaranteed Over Temperature
- Linearity Guaranteed Over Temperature: 1/2LSB max (AD565K, T)
- Low Power: 225mW Including Reference
- Pin-Out Compatible with AD563
- Low Cost ($16.00 in 100's AD565JN)



PRODUCT DESCRIPTION

The AD565 is a fast 12-bit digital-to-analog converter combined with a high stability voltage reference on a single monolithic chip. The AD565 chip uses 12 precision, high speed bipolar current steering switches, control amplifier, laser-trimmed thin film resistor network, and buried Zener voltage reference to produce a very fast, high accuracy analog output current.

The combination of performance and flexibility in the AD565 has resulted from major innovations in circuit design, an important new high-speed bipolar process, and continuing advances in laser-wafer-trimming techniques (LWT). The AD565 has a 10 – 90% full scale transition time under 35 nanoseconds and settles to within ±1/2LSB in 200 nanoseconds. AD565 chips are laser-trimmed at the wafer level to ±1/8LSB typical linearity and are specified to ±1/4LSB max error (K and T grades) at +25°C. This high speed and accuracy make the AD565 the ideal choice for high speed display drivers as well as fast analog-to-digital converters.

The subsurface (buried) Zener diode on the chip provides a low-noise voltage reference which has long-term stability and temperature drift characteristics comparable to the best discrete reference diodes. The laser trimming process which provides the excellent linearity is also used to trim both the absolute value of the reference as well as its temperature coefficient. The AD565 is thus well suited for wide temperature range performance with maximum linearity error ±1/2LSB and guaranteed monotonicity over the full temperature range. Typical full scale gain T.C. is 10ppm/°C.

The AD565 is available in four performance grades and two package types. The AD565J and K are specified for use over the 0 to 70°C temperature range and are both available in either a 24-pin, hermetically-sealed, side-brazed ceramic DIP, or a 24 pin plastic DIP. The AD565S and T grades are specified for the −55°C to +125°C range and are available in the ceramic package.

***Covered by patent numbers: 3,803,590; 3,890,611; 3,932,863; 3,978,473; 4,020,486; and other patents pending.**

PRODUCT HIGHLIGHTS

1. The AD565 is a self-contained current output DAC and voltage reference fabricated on a single IC chip.
2. The device incorporates a newly developed* fully differential, non-saturating precision current switching cell structure which combines the dc accuracy and stability first developed in the AD562 with very fast switching times and an optimally-damped settling characteristic.
3. The internal buried zener reference is laser-trimmed to 10.00 volts with a ±1% maximum error. The reference voltage is available externally and can supply up to 1.5mA beyond that required for the reference and bipolar offset resistors.
4. The chip also contains SiCr thin film application resistors which can be used either with an external op amp to provide a precision voltage output or as input resistors for a successive approximation A/D converter. The resistors are matched to the internal ladder network to guarantee a low gain temperature coefficient and are laser-trimmed for minimum full scale and bipolar offset errors.
5. The pin-out of the AD565 is compatible with the industry-standard AD563 so that a system can easily be upgraded to higher speed performance without board changes.
6. The single-chip construction makes the AD565 inherently more reliable than hybrid multi-chip designs. The AD565S and T grades with guaranteed linearity and monotonicity over the −55°C to +125°C range are especially recommended for high reliability needs in harsh environments. These units are available fully processed to MIL-STD-883, Level B.

SPECIFICATIONS (T_A = +25°C, V_{CC} = +15V, V_{EE} = −15V, unless otherwise specified)

MODEL	AD565J MIN	AD565J TYP	AD565J MAX	AD565K MIN	AD565K TYP	AD565K MAX	UNITS
DATA INPUTS (Pins 13 to 24)							
TTL or 5 Volt CMOS (T_{min} to T_{max})							
Input Voltage							
Bit ON Logic "1"	+2.0		+5.5	+2.0		+5.5	V
Bit OFF Logic "0"			+0.8			+0.8	V
Logic Current (each bit)							
Bit ON Logic "1"		+120	+300		+120	+300	μA
Bit OFF Logic "0"		+35	+100		+35	+100	μA
RESOLUTION			12			12	Bits
OUTPUT							
Current							
Unipolar (all bits on)	−1.6	−2.0	−2.4	−1.6	−2.0	−2.4	mA
Bipolar (all bits on or off)	±0.8	±1.0	±1.2	±0.8	±1.0	±1.2	mA
Resistance (exclusive of span resistors)	6k	8k	10k	6k	8k	10k	Ω
Offset							
Unipolar		0.01	0.05		0.01	0.05	% of F.S.
Bipolar (Figure 5, R_1 = 50Ω fixed)		0.05	0.15		0.05	0.1	% of F.S.
Capacitance		25			25		pF
Compliance Voltage							
T_{min} to T_{max}	−1.5		+10	−1.5		+10	V
ACCURACY (error relative to full scale) +25°C		±1/4	±1/2		±1/8	±1/4	LSB
		(0.006)	(0.012)		(0.003)	(0.006)	% of F.S.
T_{min} to T_{max}		±1/2	±3/4		±1/4	±1/2	LSB
		(0.012)	(0.018)		(0.006)	(0.012)	% of F.S.
DIFFERENTIAL NONLINEARITY							
+25°C		±1/2	±3/4		±1/4	±1/2	LSB
T_{min} to T_{max}	MONOTONICITY GUARANTEED			MONOTONICITY GUARANTEED			
TEMPERATURE COEFFICIENTS							
With Internal Reference							
Unipolar Zero		1	2		1	2	ppm/°C
Bipolar Zero		5	10		5	10	ppm/°C
Gain (Full Scale)		15	30		10	20	ppm/°C
Differential Nonlinearity		2			2		ppm/°C
SETTLING TIME TO 1/2LSB							
All Bits ON-to-OFF or OFF-to-ON		200	400		200	400	ns
FULL SCALE TRANSITION							
10% to 90% Delay plus Rise Time		15	30		15	30	ns
90% to 10% Delay plus Fall Time		30	50		30	50	ns
TEMPERATURE RANGE							
Operating	0		+70	0		+70	°C
Storage (D Package)	−65		+150	−65		+150	°C
Storage (N Package)	−25		+100	−25		+100	°C
POWER REQUIREMENTS							
V_{CC}, +13.5 to +16.5V dc		3	5		3	5	mA
V_{EE}, −13.5 to −16.5V dc		−12	−18		−12	−18	mA
POWER SUPPLY GAIN SENSITIVITY							
V_{CC} = +15V, ±10%		3	10		3	10	ppm of F.S./%
V_{EE} = −15V, ±10%		15	25		15	25	ppm of F.S./%
PROGRAMMABLE OUTPUT							
RANGE (see Figures 4,5,6)		0 to +5			0 to +5		V
		−2.5 to +2.5			−2.5 to +2.5		V
		0 to +10			0 to +10		V
		−5 to +5			−5 to +5		V
		−10 to +10			−10 to +10		V
EXTERNAL ADJUSTMENTS							
Gain Error with Fixed 50Ω Resistor for R2 (Fig. 4)		±0.1	±0.25		±0.1	±0.25	% of F.S.
Bipolar Zero Error with Fixed 50Ω Resistor for R1 (Fig. 5)		±0.05	±0.15		±0.05	±0.1	% of F.S.
Gain Adjustment Range (Fig. 4)	±0.25			±0.25			% of F.S.
Bipolar Zero Adjustment Range	±0.15			±0.15			% of F.S.
REFERENCE INPUT							
Input Impedance	15k	20k	25k	15k	20k	25k	Ω
REFERENCE OUTPUT							
Voltage	9.90	10.00	10.10	9.90	10.00	10.10	V
Current (available for external loads)	1.5	2.5		1.5	2.5		mA
POWER DISSIPATION		225	345		225	345	mW

Specifications subject to change without notice.

MODEL	AD565S MIN	AD565S TYP	AD565S MAX	AD565T MIN	AD565T TYP	AD565T MAX	UNITS
DATA INPUTS (Pins 13 to 24)							
TTL or 5 Volt CMOS (T_{min} to T_{max})							
Input Voltage							
Bit ON Logic "1"	+2.0		+5.5	+2.0		+5.5	V
Bit OFF Logic "0"			+0.8			+0.8	V
Logic Current (each bit)							
Bit ON Logic "1"		+120	+300		+120	+300	μA
Bit OFF Logic "0"		+35	+100		+35	+100	μA
RESOLUTION			12			12	Bits
OUTPUT							
Current							
Unipolar (all bits on)	−1.6	−2.0	−2.4	−1.6	−2.0	−2.4	mA
Bipolar (all bits on or off)	±0.8	±1.0	±1.2	±0.8	±1.0	±1.2	mA
Resistance (exclusive of span resistors)	6k	8k	10k	6k	8k	10k	Ω
Offset							
Unipolar		0.01	0.05		0.01	0.05	% of F.S.
Bipolar (Figure 5, R_2 = 50Ω fixed)		0.05	0.15		0.05	0.1	% of F.S.
Capacitance		25			25		pF
Compliance Voltage							
T_{min} to T_{max}	−1.5		+10	−1.5		+10	V
ACCURACY (error relative to full scale) +25°C		±1/4	±1/2		±1/8	±1/4	LSB
		(0.006)	(0.012)		(0.003)	(0.006)	% of F.S.
T_{min} to T_{max}		±1/2	±3/4		±1/4	±1/2	LSB
		(0.012)	(0.018)		(0.006)	(0.012)	% of F.S.
DIFFERENTIAL NONLINEARITY							
+25°C		±1/2	±3/4		±1/4	±1/2	LSB
T_{min} to T_{max}	MONOTONICITY GUARANTEED			MONOTONICITY GUARANTEED			
TEMPERATURE COEFFICIENTS							
With Internal Reference							
Unipolar Zero		1	2		1	2	ppm/°C
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Gain (Full Scale)		15	30		10	15	ppm/°C
Differential Nonlinearity		2			2		ppm/°C
SETTLING TIME TO 1/2LSB							
All Bits ON-to-OFF or OFF-to-ON		200	400		200	400	ns
FULL SCALE TRANSITION							
10% to 90% Delay plus Rise Time		15	30		15	30	ns
90% to 10% Delay plus Fall Time		30	50		30	50	ns
TEMPERATURE RANGE							
Operating	−55		+125	−55		+125	°C
Storage (D Package)	−65		+150	−65		+150	°C
POWER REQUIREMENTS							
V_{CC}, +13.5 to +16.5V dc		3	5		3	5	mA
V_{EE}, −13.5 to −16.5V dc		−12	−18		−12	−18	mA
POWER SUPPLY GAIN SENSITIVITY							
V_{CC} = +15V, ±10%		3	10		3	10	ppm of F.S./%
V_{EE} = −15V, ±10%		15	25		15	25	ppm of F.S./%
PROGRAMMABLE OUTPUT							
RANGE (see Figures 4,5,6)		0 to +5			0 to +5		V
		−2.5 to +2.5			−2.5 to +2.5		V
		0 to +10			0 to +10		V
		−5 to +5			−5 to +5		V
		−10 to +10			−10 to +10		V
EXTERNAL ADJUSTMENTS							
Gain Error with Fixed 50Ω Resistor for R2 (Fig. 4)		±0.1	±0.25		±0.1	±0.25	% of F.S.
Bipolar Zero Error with Fixed 50Ω Resistor for R1 (Fig. 5)		±0.05	±0.15		±0.05	±0.1	% of F.S.
Gain Adjustment Range (Fig. 4)	±0.25			±0.25			% of F.S.
Bipolar Zero Adjustment Range	±0.15			±0.15			% of F.S.
REFERENCE INPUT							
Input Impedance	15k	20k	25k	15k	20k	25k	Ω
REFERENCE OUTPUT							
Voltage	9.90	10.00	10.10	9.90	10.00	10.10	V
Current (available for external loads)	1.5	2.5		1.5	2.5		mA
POWER DISSIPATION		225	345		225	345	mW

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