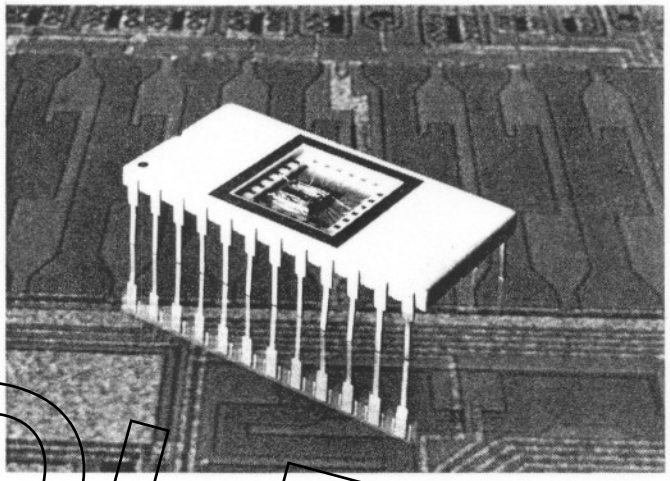
Low Cost High Speed 12-Bit Monolithic D/A Converter

AD566

PRELIMINARY TECHNICAL DATA

FEATURES

- Single Chip Construction
- Very High Speed: Settles to 1/2LSB in 200ns
  Full Scale Switching Time: 30ns
- Single Supply Operation
- Monotonicity Guaranteed Over Temperature
- Linearity Guaranteed Over Temperature — 1/2LSB max (AD566K, T)
- Low Power: 180mW
- Pin-Out Compatible with AD562
- Low Cost ($15.00 in 100's — AD566JN)



PRODUCT DESCRIPTION

The AD566 is a fast 12-bit digital-to-analog converter which incorporates the latest advances in analog circuit design into a low power monolithic chip.

The AD566 chip uses 12 precision, high speed bipolar current steering switches, control amplifier and a laser-trimmed thin film resistor network to produce a very fast, high accuracy analog output current.

The combination of performance and flexibility in the AD566 has resulted from major innovations in circuit design, an important new high-speed bipolar process, and continuing advances in laser-wafer-trimming techniques (LWT). AD566 has a 10 — 90% full scale transition time under 35 nanoseconds and settles to within ±1/2LSB in 200 nanoseconds. The AD566 chips are laser-trimmed at the wafer level to ±1/8LSB typical linearity and are specified to ±1/4LSB max error (K and T grades) at +25°C. This high speed and accuracy make the AD566 the ideal choice for high speed display drivers as well as fast analog-to-digital converters.

The AD566 is available in four performance grades and two package types. The AD566J and K are specified for use over the 0 to +70°C temperature range and are available in either a 24-pin, hermetically-sealed, side-brazed ceramic DIP, or a 24-pin plastic DIP. The AD566S and T grades are specified for the −55°C to +125°C range and are available in the ceramic package.

PRODUCT HIGHLIGHTS

1. The combination of single supply operation with wide output compliance range allows optimum versatility in fast, low noise, accurate voltage output configurations without an output amplifier.
2. The device incorporates a newly developed* fully differential, non-saturating precision current switching cell structure which combines the dc accuracy and stability first developed in the AD562 with very fast switching times and an optimally-damped settling characteristic.
3. The chip also contains SiCr thin film application resistors which can be used with with an external op amp to provide a precision voltage output or as input resistors for a successive approximation A/D converter. The resistors are matched to the internal ladder network to guarantee a low gain temperature coefficient and are laser-trimmed for minimum full scale and bipolar offset errors.
4. The pin-out of the AD566 is compatible with the industry-standard AD562 so that a system can easily be upgraded to provide higher speed performance.
5. The single-chip construction makes the AD566 inherently more reliable than hybrid multi-chip designs. The AD566S and T grades with guaranteed linearity and monotonicity over the −55°C to +125°C range are especially recommended for high reliability needs in harsh environments. These units are available fully processed to MIL-STD-883, Level B.

*Covered by patent numbers: 3,803,590; 3,890,611; 3,932,863; 3,978,473; 4,020,486; and other patents pending.

SPECIFICATIONS (T_A = +25°C, V_{EE} = −15V, unless otherwise specified)

MODEL	AD566J MIN	AD566J TYP	AD566J MAX	AD566K MIN	AD566K TYP	AD566K MAX	UNITS
DATA INPUTS (Pins 13 to 24)							
TTL or 5 Volt CMOS (T_{min} to T_{max})							
Input Voltage							
Bit ON Logic "1"	+2.0		+5.5	+2.0		+5.5	V
Bit OFF Logic "0"	0		+0.8	0		+0.8	V
Logic Current (each bit)							
Bit ON Logic "1"		+120	+300		+120	+300	μA
Bit OFF Logic "0"		+35	+100		+35	+100	μA
RESOLUTION			12			12	Bits
OUTPUT							
Current							
Unipolar (all bits on)	−1.6	−2.0	−2.4	−1.6	−2.0	−2.4	mA
Bipolar (all bits on or off)	±0.8	±1.0	±1.2	±0.8	±1.0	±1.2	mA
Resistance (exclusive of span resistors)	6k	8k	10k	6k	8k	10k	Ω
Offset							
Unipolar (adjustable to zero per Figure 5)		0.01	0.05		0.01	0.05	% of F.S.
Bipolar (Figure 6 R_1 and R_2 = 50Ω fixed)		0.05	0.15		0.05	0.1	% of F.S.
Capacitance		20			20		pF
Compliance Voltage							
T_{min} to T_{max}	−1.5		+10	−1.5		+10	V
ACCURACY (error relative to full scale) +25°C		±1/4	±1/2		±1/8	±1/4	LSB
		(0.006)	(0.012)		(0.003)	(0.006)	% of F.S.
T_{min} to T_{max}		±1/2	±3/4		±1/4	±1/2	LSB
		(0.012)	(0.018)		(0.006)	(0.012)	% of F.S.
DIFFERENTIAL NONLINEARITY							
+25°C		±1/2	±3/4		±1/4	±1/2	LSB
T_{min} to T_{max}	MONOTONICITY GUARANTEED			MONOTONICITY GUARANTEED			
TEMPERATURE COEFFICIENTS							
Unipolar Zero		1	2		1	2	ppm/°C
Bipolar Zero		5	10		5	10	ppm/°C
Gain (Full Scale)		7	10		2	3	ppm/°C
Differential Nonlinearity		2			2		ppm/°C
SETTLING TIME TO 1/2LSB							
All Bits ON-to-OFF or OFF-to-ON		200	400		200	400	ns
FULL SCALE TRANSITION							
10% to 90% Delay plus Rise Time		15	30		15	30	ns
90% to 10% Delay plus Fall Time		30	50		30	50	ns
POWER REQUIREMENTS							
V_{EE}, −13.5 to −16.5V dc		−12	−20		−12	−20	mA
POWER SUPPLY GAIN SENSITIVITY							
V_{EE} = −15V, ±10%		15	25		15	25	ppm of F.S./%
PROGRAMMABLE OUTPUT							
RANGE (see Figures 5, 6, 7)		0 to +5			0 to +5		V
		−2.5 to +2.5			−2.5 to +2.5		V
		0 to +10			0 to +10		V
		−5 to +5			−5 to +5		V
		−10 to +10			−10 to +10		V
EXTERNAL ADJUSTMENTS							
Gain Error with Fixed 50Ω Resistor for R2 (Fig. 5)		±0.1	±0.25		±0.1	±0.25	% of F.S.
Bipolar Zero Error with Fixed 50Ω Resistor for R1 (Fig. 6)		±0.05	±0.15		±0.05	±0.1	% of F.S.
Gain Adjustment Range (Fig. 5)	±0.25			±0.25			% of F.S.
Bipolar Zero Adjustment Range	±0.15			±0.15			% of F.S.
REFERENCE INPUT							
Input Impedance	15k	20k	25k	15k	20k	25k	Ω
POWER DISSIPATION		180	300		180	300	mW

MULTIPLYING MODE PERFORMANCE (All Models)	
Quadrants	Two(2): Bipolar Operation at Digital Input Only
Reference Voltage	+1V to +10V, Unipolar.
Reference Feedthrough (unipolar mode, all bits OFF, and 0 to +10V [p-p], sinewave frequency for 1/2LSB [p-p] feedthrough)	40kHz typ
Output Slew Rate 10%–90%	5mA/μs
90%–10%	1mA/μs
FULL POWER BANDWIDTH	300kHz
Control Amplifier Small-Signal Closed-Loop Bandwidth	1.8MHz

Specifications subject to change without notice.

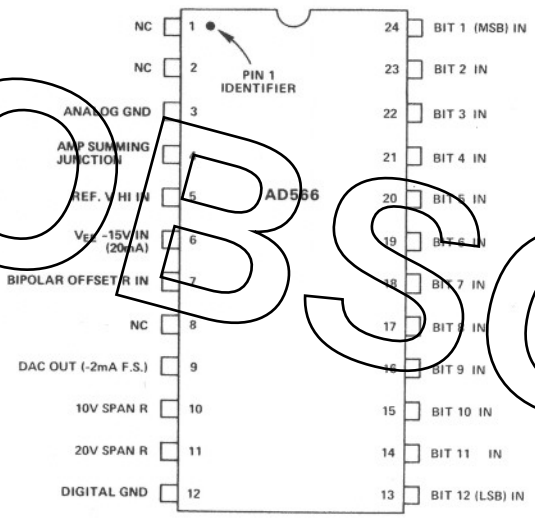
MODEL	AD566S MIN	AD566S TYP	AD566S MAX	AD566T MIN	AD566T TYP	AD566T MAX	UNITS
DATA INPUTS (Pins 13 to 24)							
TTL or 5 Volt CMOS (T_{min} to T_{max})							
Input Voltage							
Bit ON Logic "1"	+2.0		+5.5	+2.0		+5.5	V
Bit OFF Logic "0"	0		+0.8	0		+0.8	V
Logic Current (each bit)							
Bit ON Logic "1"		+120	+300		+120	+300	μA
Bit OFF Logic "0"		+35	+100		+35	+100	μA
RESOLUTION			12			12	Bits
OUTPUT							
Current							
Unipolar (all bits on)	-1.6	-2.0	-2.4	-1.6	-2.0	-2.4	mA
Bipolar (all bits on or off)	±0.8	±1.0	±1.2	±0.8	±1.0	±1.2	mA
Resistance (exclusive of span resistors)	6k	8k	10k	6k	8k	10k	Ω
Offset							
Unipolar (adjustable to zero per Figure 5)		0.01	0.05		0.01	0.05	% of F.S.
Bipolar (Figure 6 R_1 and R_2 = 50Ω fixed)		0.05	0.15		0.05	0.1	% of F.S.
Capacitance		25			25		pF
Compliance Voltage							
T_{min} to T_{max}	-1.5		+10	-1.5		+10	V
ACCURACY (error relative to full scale) +25°C		±1/8	±1/2		±1/8	±1/4	LSB
		(0.003)	(0.006)		(0.003)	(0.006)	% of F.S.
T_{min} to T_{max}		±1/2	±3/4		±1/4	±1/2	LSB
		(0.012)	(0.018)		(0.006)	(0.012)	% of F.S.
DIFFERENTIAL NONLINEARITY							
+25°C		±1/2	±3/4		±1/4	±1/2	LSB
T_{min} to T_{max}	MONOTONICITY GUARANTEED			MONOTONICITY GUARANTEED			
TEMPERATURE COEFFICIENTS							
Unipolar Zero		1	2		1	2	ppm/°C
Bipolar Zero		5	10		5	10	ppm/°C
Gain (Full Scale)		7	10		2	3	ppm/°C
Differential Nonlinearity		2			2		ppm/°C
SETTLING TIME TO 1/2LSB							
All Bits ON-to-OFF or OFF-to-ON		200	400		200	400	ns
FULL SCALE TRANSITION							
10% to 90% Delay plus Rise Time		15	30		15	30	ns
90% to 10% Delay plus Fall Time		30	50		30	50	ns
POWER REQUIREMENTS							
V_{EE}, -13.5 to -16.5V dc		-12	-20		-12	-20	mA
POWER SUPPLY GAIN SENSITIVITY							
V_{EE} = -15V, ±10%		15	25		15	25	ppm of F.S./%
PROGRAMMABLE OUTPUT							
RANGE (see Figures 5, 6, 7)		0 to +5			0 to +5		V
		-2.5 to +2.5			-2.5 to +2.5		V
		0 to +10			0 to +10		V
		-5 to +5			-5 to +5		V
		-10 to +10			-10 to +10		V
EXTERNAL ADJUSTMENTS							
Gain Error with Fixed 50Ω Resistor for R2 (Fig. 5)		±0.1	±0.25		±0.1	±0.25	% of F.S.
Bipolar Zero Error with Fixed 50Ω Resistor for R1 (Fig. 6)		±0.05	±0.15		±0.05	±0.1	% of F.S.
Gain Adjustment Range (Fig. 5)	±0.25			±0.25			% of F.S.
Bipolar Zero Adjustment Range	±0.15			±0.15			% of F.S.
REFERENCE INPUT							
Input Impedance	15k	20k	25k	15k	20k	25k	Ω
POWER DISSIPATION		180	300		180	300	mW
MULTIPLYING MODE PERFORMANCE (All Models)							
Quadrants		Two(2): Bipolar Operation at Digital Input Only					
Reference Voltage		+1V to +10V, Unipolar.					
Reference Feedthrough (unipolar mode, all bits OFF, and 0 to +10V [p-p], sinewave frequency for 1/2LSB [p-p] feedthrough)		40kHz typ					
Output Slew Rate 10%-90%		5mA/μs					
90%-10%		1mA/μs					
FULL POWER BANDWIDTH		300kHz					
Control Amplifier Small-Signal Closed-Loop Bandwidth		1.8MHz					

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

V_{EE} to Digital Common . . . . . 0 to −18V
Analog Common to Digital Common. . . . . ±1V
Voltage on DAC Output (Pin 9) . . . . . −3 to +12V
Digital Inputs (Pins 13 to 24) to Digital Com . . −1.0 to +7.0V
Ref In to Analog Common . . . . . ±12V
Bipolar Offset to Analog Common . . . . . ±12V
10V Span R to Analog Common . . . . . ±12V
20V Span R to Analog Common . . . . . ±24V
Power Dissipation 1000mW

TOP VIEW



MIL-STD-883B

The rigors of the military/aerospace environment, temperature extremes, humidity, mechanical stress, etc., demand the utmost in electronic circuits. The AD566, with the inherent reliability of integrated circuit construction, was designed with these applications in mind. The hermetically-sealed, low profile DIP package takes up a fraction of the space required by equivalent modular designs and protects the chip from hazardous environments. To further insure reliability, the AD566 is offered with 100% screening to MIL-STD-883, method 5004.

Table 1 details the test procedures of MIL-STD-883. Analog Devices subjects each part ordered with 883 screening to these tests on a 100% basis.

TABLE I

TEST*	METHOD
1) Internal Visual (Pre cap)	2010, Test Condition B
2) Stabilization Bake	Method 1008, 24 hours @ +150°C
3) Temperature Cycling	Method 1010, Test Condition C, 10 Cycles, -65°C to +150°C
4) Constant Acceleration	Method 2001, Test Condition E, Y1 plane, 30kg
5) Seal, Fine and Gross	Method 1014, Test Condition A and C
6) Burn-in Test	Method 1015, Test Condition B, 160 hours @ +125°C min.
7) Final Electrical Tests	Performed 100% to all min and max specifications on data pages
8) External Visual	Method 2009

*Test performed in accordance with MIL-STD-883, Level B, Method 5004.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

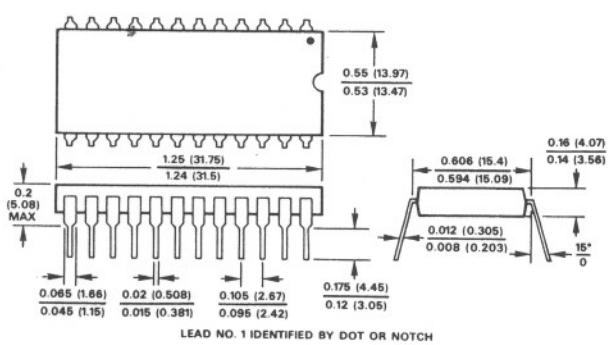


Figure 1. Molded Plastic Package (Type N) 24-Lead Dual-In-Line

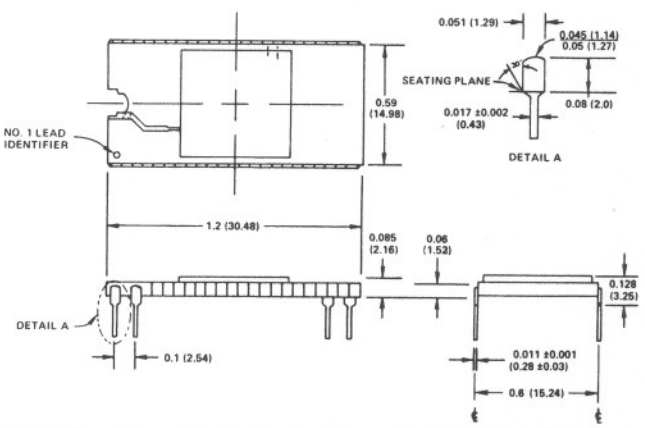


Figure 2. Hermetically-Sealed Ceramic Side-Brazed Package (Type D) 24-Lead Dual-In-Line

AD566 ORDERING GUIDE

MODEL	PACKAGE	TEMP RANGE	LINEARITY ERROR MAX @ 25°C	MAX GAIN T.C. (ppm of F.S./°C)	PRICE 1–24	25–99	100–999
AD566JN/BIN	Plastic	0 to +70°C	±1/2LSB	10	$ 22.50	$18.75	$15.00
AD566JD/BIN	Ceramic	0 to +70°C	±1/2LSB	10	$ 24.95	$21.50	$17.50
AD566KN/BIN	Plastic	0 to +70°C	±1/4LSB	3	$ 29.50	$26.00	$22.50
AD566KD/BIN	Ceramic	0 to +70°C	±1/4LSB	3	$ 38.00	$31.50	$25.75
AD566SD/BIN	Ceramic	−55°C to +125°C	±1/2LSB	10	$ 77.50	$63.50	$50.00
AD566TD/BIN	Ceramic	−55°C to +125°C	±1/4LSB	3	$105.00	$90.00	$77.50

Contact factory for pricing on units screened to MIL-STD-883.

THE AD566 OFFERS TRUE 12-BIT PERFORMANCE

ACCURACY: Analog Devices defines accuracy as the maximum deviation of the actual, adjusted DAC output (see page 6) from the ideal analog output (a straight line drawn from 0 to F.S. − 1LSB) for any bit combination. The AD566 is laser trimmed to 1/4LSB (0.025% of F.S.) maximum error at +25°C for the K and T version and to 1/2LSB for the J and S versions.

MONOTONICITY: A DAC is said to be monotonic if the output either increases or remains constant for increasing digital inputs such that the output will always be a non-decreasing function of the input. All versions of the AD566 are monotonic over their entire operating temperature range.

DIFFERENTIAL NONLINEARITY: Monotonic behavior requires that the differential nonlinearity error be less than 1LSB both at +25°C and over the temperature range of interest. Differential nonlinearity is the measure of the variation in analog value, normalized to full scale, associated with a 1LSB change in digital input code. For example, if a 1LSB change in the input code results in a change of only 0.61mV (1/4LSB) in analog output, the differential nonlinearity error would be 1.83mV, or 3/4LSB. The AD566K and T have a max differential linearity error of 1/2LSB, which is a tighter specification than simply guaranteed monotonicity.

ANALYZING DEVICE ACCURACY OVER THE TEMPERATURE RANGE

For the purposes of temperature drift analysis, the major device components are shown in Figure 3.

The input reference current to the DAC, I_{REF}, is developed from the external reference and will show the same drift rate as the reference voltage. The DAC output current, I_{DAC} which is a function of the digital input code, is designed to track I_{REF}; if there is a slight mismatch in these currents over temperature, it will contribute to the gain T.C. The bipolar offset resistor, R_{BP}, and gain setting resistor, R_{GAIN}, also have temperature coefficients which contribute to system drift errors.

There are three types of drift errors over temperature: offset, gain, and linearity. Offset drift causes a vertical translation of the entire transfer curve; gain drift is a change in the slope of the curve; and linearity drift represents a change in the shape of the curve. The combination of these three drifts results in the complete specification for total error over temperature.

Total error is defined as the deviation from a true straight line transfer characteristic from exactly zero at a digital input which calls for zero output to a point which is defined as full scale. A specification for total error over temperature assumes that both the zero and full scale points have been trimmed for zero error at +25°C. Total error is normally expressed a percentage of the full scale range. In the bipolar situation, this means the total range from $-V_{FS}$ to $+V_{FS}$.

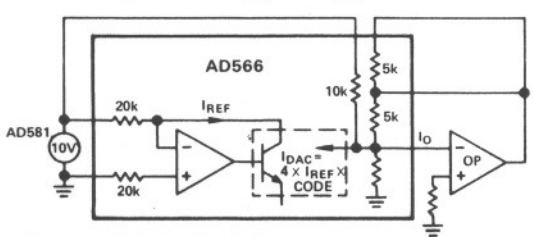


Figure 3. Bipolar Configuration

MONOTONICITY AND LINEARITY

The initial linearity error of ±1/2LSB max and the differential linearity error of ±3/4LSB max guarantee monotonic performance over the range of −55°C to +125°C. It can, therefore, be assumed that linearity errors are insignificant in computation of total temperature errors.

UNIPOLAR ERRORS

Temperature error analysis in the unipolar mode is straightforward: there is an offset drift and a gain drift. The offset drift of 2ppm/°C max (which comes from leakage currents) causes a linear shift in the transfer curve as shown in Figure 4. The gain drift causes a change in the slope of the curve which results from reference drift and the device gain drift. The device gain drift is the DAC drift and drift in R_{GAIN} relative to the DAC resistors for a total of 10ppm/°C max. Total absolute error due to all of these effects is guaranteed to be less than ±0.018% of full scale from −55°C to +125°C.

BIPOLAR RANGE ERRORS

The analysis is slightly more complex in the bipolar mode. In this mode R_{BP} is connected to V_{REF} (see Figure 3) to generate a current which exactly balances the current of the MSB so that the output voltage is zero with the MSB on.

Note that if the DAC and application resistors track perfectly, the bipolar offset drift will be zero even if the reference drifts. A change in the reference voltage, which causes a shift in the bipolar offset, will also cause an equivalent change in I_{REF} and thus I_{DAC}, so that I_{DAC} will always be exactly balanced by I_{BP} with the MSB turned on. This effect is shown in Figure 4. The net effect of the reference drift then is simply to cause a rotation in the transfer around bipolar zero. However, consideration of second order effects (which are often overlooked) reveals the errors in the bipolar mode. The unipolar offset drifts discussed before will have the same effect on the bipolar offset. A mismatch of R_{BP} to the DAC resistors is usually the largest component of bipolar drift, but in the AD566 this error is held to 10ppm max. The total of all these errors is held to ±0.39% of full scale from −55°C to +125°C. Note that, in the bipolar ranges, full scale is defined as the total range from $-V_{FS}$ to $+V_{FS}$.

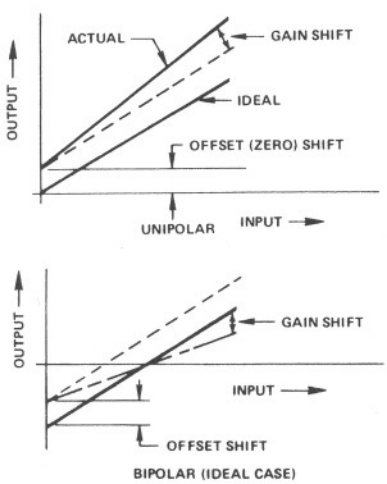


Figure 4. Unipolar and Bipolar Drifts

CONNECTING THE AD566 FOR BUFFERED VOLTAGE OUTPUT

The standard current-to-voltage conversion connections using an operational amplifier are shown here with the preferred trimming techniques. If a low offset operational amplifier (AD510L, AD517L, AD741L, AD301AL) is used, excellent performance can be obtained in many situations without trimming (an op amp with less than 0.5mV max offset voltage should be used to keep offset errors below 1/2LSB). If a 50Ω fixed resistor is substituted for the 100Ω trimmer, unipolar zero will typically be within ±1/2LSB (plus op amp offset), and full scale accuracy will be within 0.1% (0.25% max). Substituting a 50Ω resistor for the 100Ω bipolar offset trimmer will give a bipolar zero error typically within ±2LSB (0.05%).

The AD509 is recommended for buffered voltage-output applications which require a settling time to ±1/2LSB of one microsecond. The feedback capacitor is shown with the optimum value for each application; this capacitor is required to compensate for the 25 picofarad DAC output capacitance.

FIGURE 5 UNIPOLAR CONFIGURATION

This configuration will provide a unipolar 0 to +10 volt output range. In this mode, the bipolar terminal, pin 7, should be grounded if not used for trimming.

STEP I . . . ZERO ADJUST

Turn all bits OFF and adjust zero trimmer, R1, until the output reads 0.000 volts (1LSB = 2.44mV). In most cases this trim is not needed, but pin 7 should then be connected to pin 3.

STEP II . . . GAIN ADJUST

Turn all bits ON and adjust 100Ω gain trimmer, R2, until the output is 9.9976 volts. (Full scale is adjusted to 1LSB less than nominal full scale of 10.000 volts.) If a 10.2375V full scale is desired (exactly 2.5mV/bit), insert a 120Ω resistor in series with the gain resistor at pin 10 to the op amp output.

FIGURE 6. BIPOLAR CONFIGURATION

This configuration will provide a bipolar output voltage from −5.000 to +4.9976 volts, with positive full scale occurring with all bits ON (all 1's).

STEP 1. . . OFFSET ADJUST

Turn OFF all bits. Adjust 100Ω trimmer R1, to give −5.000 output volts.

STEP II . . . GAIN ADJUST

Turn ON all bits, adjust 100Ω gain trimmer R_2 to give a reading of +4.9976 volts.

Please note that it is not necessary to trim the op amp to obtain full accuracy at room temperature. In most bipolar situations, an op amp trim is unnecessary unless the untrimmed offset drift of the op amp is excessive.

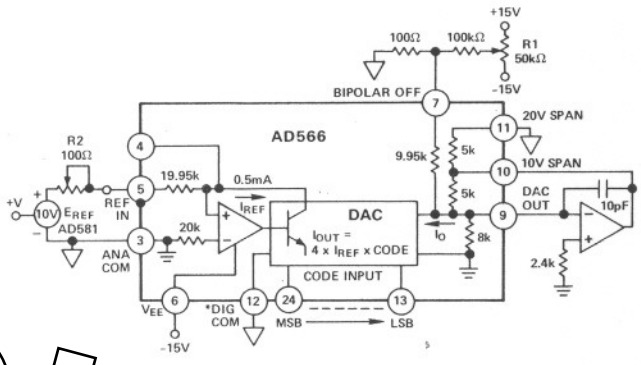
FIGURE 7. OTHER VOLTAGE RANGES

The AD566 can also be easily configured for a unipolar 0 to +5 volt range or ±2.5 volt and ±10 volt bipolar ranges by using the additional 5k application resistor provided at the 20 volt span R terminal, pin 11. For a 5 volt span (0 to +5V or +2.5V), the two 5k resistors are used in parallel by shorting pin 11 to pin 9 and connecting pin 10 to the op amp output and the bipolar offset resistor either to ground for unipolar or to V_{REF} for the bipolar range. For the ±10 volt range (20 volt span) use the 5k resistors in series by connecting only pin 11 to the op amp output and the bipolar offset connected as shown. The ±10 volt option is shown in Figure 7.

DIGITAL INPUT		ANALOG OUTPUT		
MSB	LSB	Straight Binary	Offset Binary	Two's Compl.*
0 0 0 0 0 0 0 0 0 0 0 0		Zero	−Full Scale	Zero
0 1 1 1 1 1 1 1 1 1 1 1		Mid Scale −1LSB	FS −1LSB	+FS −1LSB
1 0 0 0 0 0 0 0 0 0 0 0		+1/2 FS	Zero	−FS
1 1 1 1 1 1 1 1 1 1 1 1		+FS −1LSB	+ Full Scale −1LSB	+FS −1LSB

*Invert the MSB of the offset binary code with an external inverter to obtain two's complement.

Table 2. Digital Input Codes



*DIGITAL AND ANALOG COMMON MUST HAVE A COMMON CURRENT RETURN PATH. SEE NEXT PAGE FOR PROPER CONNECTIONS.

Figure 5. 0 to +10V Unipolar Voltage Output

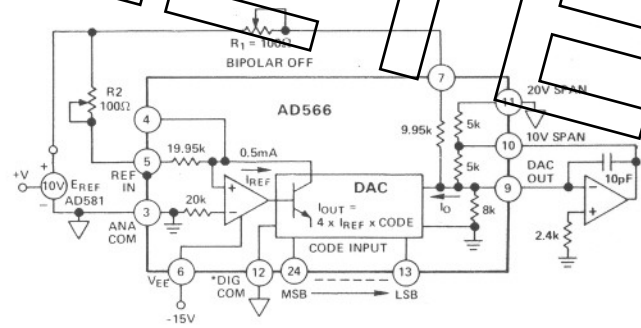
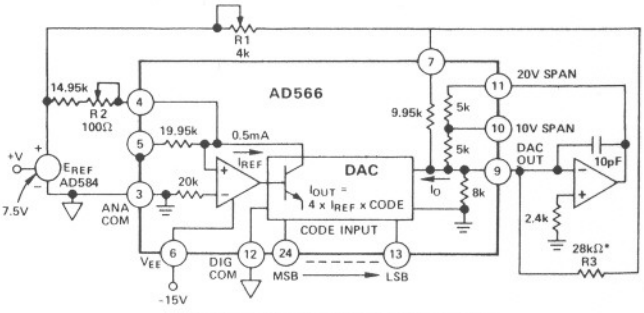


Figure 6. ±5V Bipolar Voltage Output



*THE PARALLEL COMBINATION OF THE BIPOLAR OFFSET RESISTOR AND R3 ESTABLISH A CURRENT TO BALANCE THE MSB CURRENT. THE EFFECT OF TEMPERATURE COEFFICIENT MISMATCH BETWEEN THE BIPOLAR RESISTOR COMBINATION AND DAC RESISTORS IS EXPLAINED ON PREVIOUS PAGE.

Figure 7. ±10V Voltage Output

DIGITAL INPUT CONSIDERATIONS

The threshold of the digital input circuitry is set at 2.0 volts and does not vary with supply voltage. The input lines can interface with any type of 5 volt logic, TTL/DTL or CMOS, and have sufficiently low input currents to interface easily with unbuffered CMOS logic. The configuration of the input circuit is shown in Figure 8. The input line can be modelled as a 30kΩ resistance connected to a −0.7V rail.

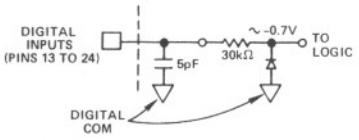


Figure 8. Equivalent Digital Input Circuit

APPLICATION OF ANALOG AND DIGITAL COMMONS

The AD566 brings out separate analog and digital grounds to allow optimum connections for low noise and high speed performance. The two ground lines can be separated by up to 200 millivolts without any loss in performance. There may be some loss in linearity beyond that level. Up to ±1 volt can be tolerated between the ground lines without damage to the device, If the AD566 is to be used in a system in which the two grounds will be ultimately connected at some distance from the device, it is recommended that parallel back-to-back diodes be connected between the ground lines near the device to prevent a fault condition.

The analog common at pin 3 is the ground reference point for the internal reference and is thus the "high quality" ground for the AD566; it should be connected directly to the analog reference point of the system. The digital common at pin 12 can be connected to the most convenient ground reference point; analog power return is preferred, but digital ground is acceptable. If digital common contains high frequency noise in excess of 200mV, this noise may feed through to the output of the converter, therefore some caution is required in applying these grounds.

OUTPUT VOLTAGE COMPLIANCE

The AD566 has a typical output compliance range of −2 to +10 volts. The current-steering output stages will be unaffected by changes in the output terminal voltage over that range. However, there is an equivalent output impedance of 8kΩ in parallel with 25pF at the output terminal which produces an equivalent error current if the voltage deviates from analog common. This is a linear effect which does not change with input code. Operation beyond the compliance limits may cause either output stage saturation or breakdown which results in nonlinear performance. Compliance limits are a function of output current and negative supply, as shown in Figure 9.

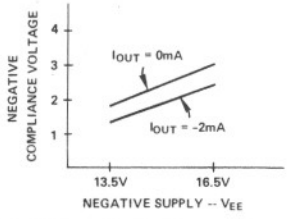


Figure 9. Typical Neg. Compliance Range vs. Neg. Supply

HIGH SPEED SYSTEM DESIGN

Full realization of the AD566 high speed capabilities requires strict attention to detail by the user in all areas of application and testing.

The settling time for the AD566 is specified for the current output, an inherently high speed DAC operating mode. However, most DAC applications require a current-to-voltage conversion at some point in the signal path, although an unbuffered voltage level (not using an op amp) is suitable for use in a successive-approximation A/D converter (see next page), or in many display applications. With proper design this form of current-to-voltage conversion can give very fast operation. The fastest voltage conversion is achieved by connecting a low value resistor directly to the output, as shown in Figure 10. In this case, the settling time is primarily determined by the cell switching time and by the RC time constant of the AD566 output capacitance of 25 picofarads (plus stray capacitance) combined with the output resistor value. Settling to 0.01% of full scale (for a full scale transition) requires 9 time constants. This effect is important for an equivalent resistance over 1kΩ.

If an op amp is used to provide a low impedance output signal, some loss in settling time will be seen due to op amp dynamics. The normal current-to-voltage converter op amp circuits, based on the fast settling AD509 are shown in the applications circuits on Performance page. The unipolar or bipolar circuits shown settle to ±1/2LSB in 1μs. The DAC output capacitance, which acts as a stray capacitance at the op amp inverting input, must be compensated by a feedback capacitor, as shown. The value should be chosen carefully for each application and each op amp type.

Fastest operation will be obtained by minimizing lead lengths, stray capacitance and impedance levels. The supply should be bypassed near the device; 0.1μF will be sufficient since the AD566 runs at constant supply current regardless of input code. Output capacitance can be minimized by grounding pin 11 in 10V span applications.

DIRECT UNBUFFERED VOLTAGE OUTPUT FOR CABLE DRIVING

The wide compliance range allows direct current-to-voltage conversion with just an output resistor. Figure 10 shows a connection using the gain and bipolar output resistors to give a ±1.60 volt bipolar swing. In this situation, the digital code is complementary binary. Other combinations of internal and external output resistors (R_X) can be used to scale to alternate voltage ranges, simply by appropriately scaling the 0 to -2mA unipolar output current and using the 10.0 volt reference voltage for bipolar offset. For example, setting R_X = 2.67kΩ gives a ±1 volt range with a 1kΩ equivalent output impedance.

This connection is especially useful for directly driving a long cable at high speed. A 50Ω R_X resistor drives a 50Ω cable with a ±50mV full scale swing; settling time is very fast as discussed in the section above.

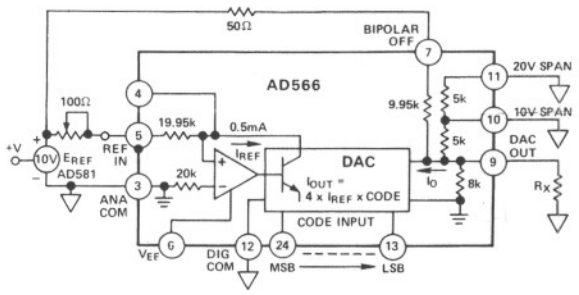


Figure 10. Unbuffered Bipolar Voltage Output

MICROPROCESSOR CONTROL FOR A 12-BIT DAC

A common I/O interface is the Digital-to-Analog Converter output, which provides a voltage corresponding to a data word from a microprocessor.

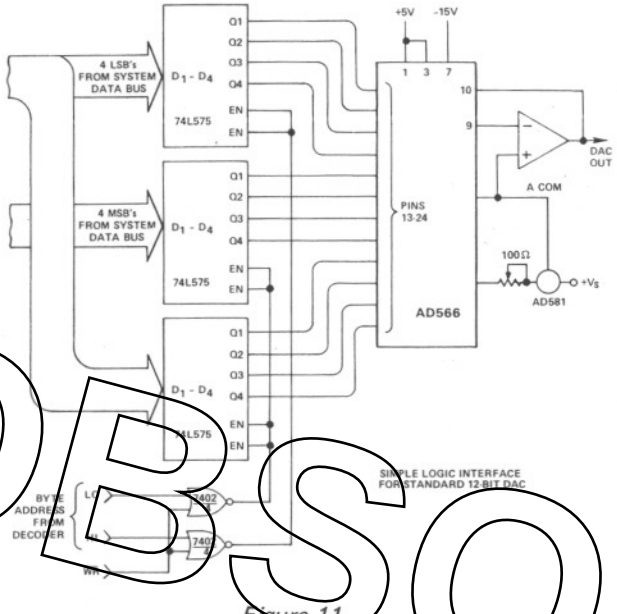


Figure 11.

A complex situation arises when the data for the DAC needs more bits of resolution than the system data bus can carry in 1 byte. For example, applications using an 8-bit microprocessor is often required to drive a 12-bit DAC. Several hardware formats are possible; the most convenient one depends on the desired data format. If the most significant 8 bits are in one byte of memory, they can be transferred into an 8-bit latch in one memory-or I/O-write cycle. An adjacent cycle can be used to transfer the 4 most-significant bits of another data word into a latch controlling the 4 least-significant bits of the DAC. The most-significant bits of the data bus drive two separately controlled 4-bit latches which are controlled by two separate addresses. The Hi Byte address allows the microprocessor to write in the 8 most significant data bits and the Lo Byte address allows the microprocessor to write in the 4 remaining bits. When all 12 bits are latched, the DAC output will assume its proper new value. An intermediate value will be momentarily present at the DAC terminals between Hi and Lo Byte write cycles. For applications such as CRT displays where this intermediate value cannot be tolerated, double buffering can be effectively employed. This could be implemented with a separately-controlled 12-bit latch at the DAC inputs.

D/A CONVERTERS IN DISPLAYS

In Figure 12, a counter-driven AD566 is shown as a sawtooth sweep generator. When used for displays, this scheme provides a highly-repeatable, controllable linear sweep.

Raster displays are usually generated by a fast horizontal scan and a slower vertical scan which is derived from the horizontal scan. Intensity modulation during each horizontal scan provides the pictorial information. The picture resolution is expressed in terms of the number of discernible data points per line multiplied by the number of lines. The minimum frame period is the time allowed for the horizontal scan-plus-retrace multiplied by the number of lines, plus vertical retrace time.

A family of monolithic D/A converters is available from Analog Devices that are suitable for verticle sweeps. The line-spacing uniformity depends on linearity while maximum number of lines depends on DAC resolution. A display of 1024 lines would require 10 bits of resolution and 12 bits of linearity (0.012% of linearity provides less than 12% of spaci error). Switching transients created within the vertical sweep DAC are blanked because they occur during the horizontal retrace interval.

For horizontal sweeps, the DAC requirements are more severe For example, to resolve 500 points per line, at 500 lines per frame, at a 30Hz frame rate, requires that each digital horizontal step settle within 100ns (typical full scale settling time is 200ns), and that there be no "glitches". Even if the display is blanked between horizontal steps, large glitches at major carriers can cause deflection-amplifier transients, which distor the pattern.

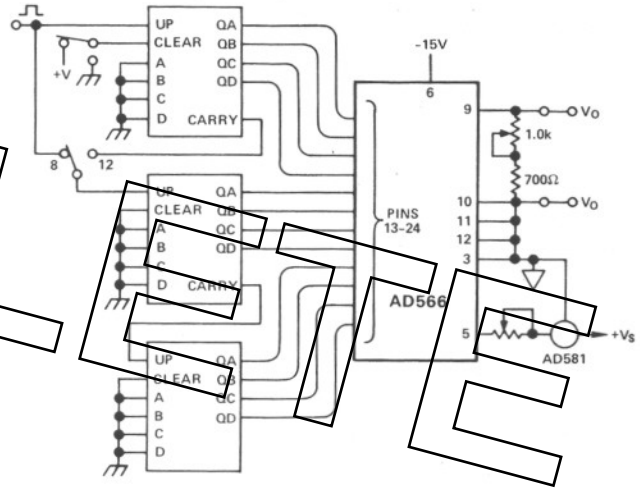


Figure 12.

The excellent high speed performance of the AD566 is demonstrated in the oscilloscope photograph of Figure 13. This measurement is made with the AD566 driving directly into an equivalent 50Ω load, amplified with a low capacitance MOS-input, UHF amplifier. The figure shows the worst case situation, which is full scale transition from switching all bits OFF to ON. The equipment and circuitry used to make the measurements adds about 50ns to the actual device performance.

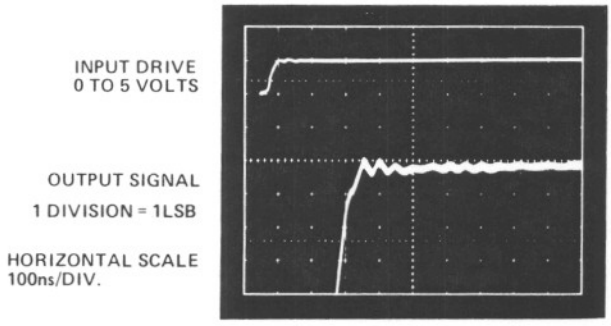


Figure 13. Settling Characteristic Detail