AN-1289
APPLICATION NOTE

One Technology Way • P.O. Box 9106 • Norwood, MA 02062-9106, U.S.A. • Tel: 781.329.4700 • Fax: 781.461.3113 • www.analog.com

Using the AD5755 and Similar Dynamic Power Control DACs in Applications Without Dynamic Power Control

by David Rice

INTRODUCTION

This application note describes using the AD5755 and other similar industrial DACs in applications that do not require the dynamic power control (DPC) feature.

This group of products consists of five industrial DACs, which have multiple options to suit various applications. Table 1 lists and highlights the features of each DAC.

DPC operates by sensing the load on the current output pin and supplying only the power that is required. To achieve this, the AD5755, for example, controls a dc-to-dc converter to step up a 5 V supply to between 7.4 V and 29.5 V.

DPC is particularly useful in systems with wide load ranges including a short-circuit condition (0 Ω load to ground) where all power generated by the supply is dissipated on chip. In non-DPC systems, this results in higher IC temperatures that increase overall system temperatures.

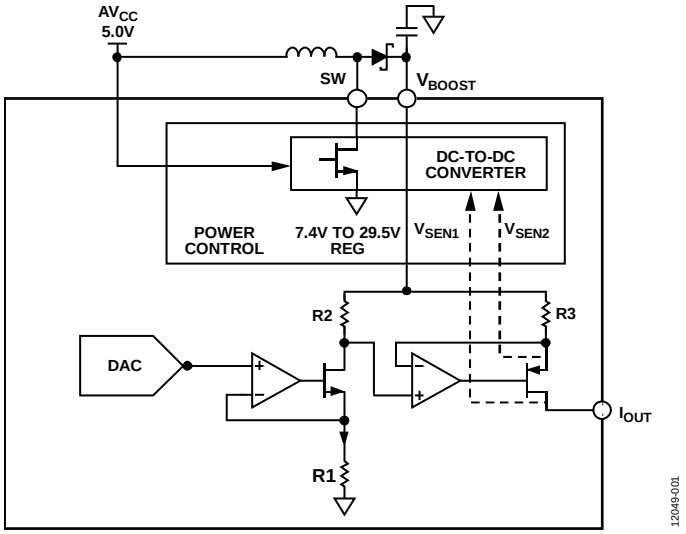

Figure 1. AD5755 with Dynamic Power Control

There are low power applications that may not require dynamic power control. In these cases, the dc-to-dc converter can be excluded from the design. This reduces the number of external components and is useful for applications with space-constraints that require the AD5755 quad-channel feature.

This application note describes two alternatives to using the dc-to-dc converter. The first method uses an external PMOS to limit on-chip power dissipation. The second method involves powering the DAC directly with all power dissipated directly on chip. Each method describes the setup and calculates total power dissipation both on and off chip.

Table 1. AD5755 and Similar Dynamic Power Control DACs

ADC	Features
AD5755	16-Bit, Quad Channel, Current and Voltage Output DAC
AD5755-1	16-Bit, Quad Channel, Current and Voltage Output DAC with HART Connectivity
AD5735	12-Bit, Quad Channel, Current and Voltage Output DAC
AD5757	16-Bit, Quad Channel, Current Output DAC with HART Connectivity
AD5737	12-Bit, Quad Channel, Current Output DAC with HART Connectivity

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REVISION HISTORY

3/14—Revision 0: Initial Version

METHOD 1—USING EXTERNAL PMOS

As an alternative to the dc-to-dc converter, an external PMOS transistor can be used to limit the on-chip power dissipation, though this does not reduce the power dissipation of the total system. On the AD5755, AD5735, and AD5755-1, the PMOS circuit is set up as shown in Figure 2.

V_{BOOST} must be powered for both voltage and current output ranges. V_{BOOST} can be tied to AV_{DD} as long as sufficient headroom is maintained between V_{BOOST} and the output per the formula shown in Table 2.

Leave the SWx and $COMP_{DCDC\_A}$ pins open circuit. Tie AV_{CC} to DV_{DD}. This maintains the voltage on the AV_{CC} pin above the most negative supply, AV_{SS} or 0 V (this applies only to the AD5755-1, AD5737, and AD5757). If the voltage on the AV_{CC} pin is equal to or below the most negative voltage, it can result in latch-up. See Table 2 for recommended supplies for the AV_{CC} and V_{BOOST} rails. All other pins are set up in the same manner as when the dynamic power control function is used. Details are outlined in the Pin Configuration section and Layout Guidelines section of the product data sheet.

V_{BOOST} is powered externally and the Zener diode holds the gate of the external PMOS at V_{BOOST} – Zener voltage. This means that the majority of the power dissipation of the channel takes place in the external PMOS transistor.

The power dissipated by PMOS is calculated as follows (using worst-case figures):

V_{BOOST} = 33 V

Zener Voltage = 5 V

R_{LOAD} = 0 Ω

I_{OUT} = 24 mA

One Channel

On-chip power

5 V × 0.024 A = 0.12 W

Off-chip power

28 V × 0.024 A = 0.672 W

Four Channels

On-chip power

0.12 W × 4 = 0.48 W

Off-chip power

0.672 W × 4 = 2.688 W

The calculations in this section do not factor in the quiescent currents of the AD5755; Table 3 includes these currents to calculate the maximum power and allowed ambient temperature for the AD5755. From the calculations, V_{BOOST} is 5 V in the equation. The remainder of the power is dissipated off chip on the PMOS.

When selecting R1, it is important that the power is kept low. In this example, R1 = 1 MΩ and 33 V is the voltage supplied. There is a 5 V drop across the Zener diode. This means that there is 28 µA flowing through the 1 MΩ resistor (0.784 mW dissipated). The PMOS chosen must be able to tolerate a V_{DS} voltage of $-V_{BOOST}$ and handle the power dissipation required. The PMOS typically has minimal effect on current output performance.

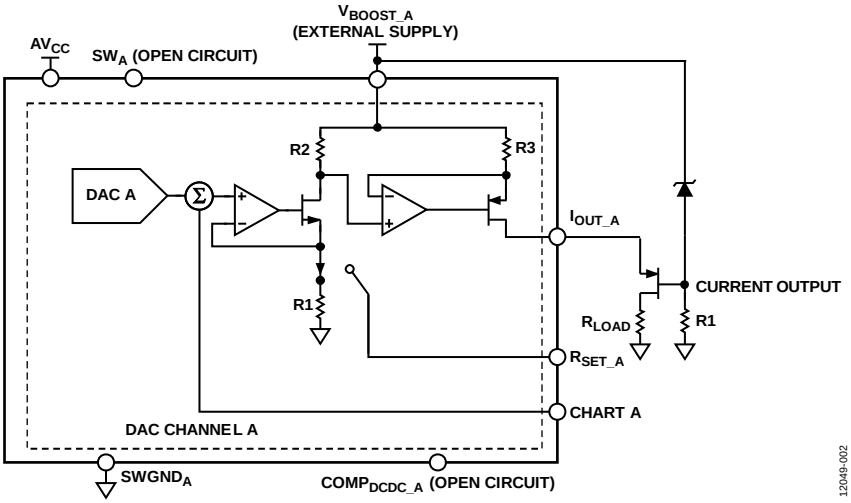

Figure 2. Configuration of a Channel using an External Zener Diode on the AD5755-1

Figure 3 shows the AD5757/AD5737 which have pins (IGATEx) dedicated to controlling an external PMOS. Therefore, a Zener diode is not required. The IGATEx pins are only used when the dynamic power control feature is not being used. It holds the gate of the external PMOS at V_{BOOST} – 5 V causing the majority of the power dissipation to take place on the external PMOS.

The PMOS chosen must be able to tolerate a V_{DS} voltage of $-V_{BOOST}$ and handle the power dissipation required. The PMOS typically has minimal effect on current output performance.

The setup and calculations are the same as in the PMOS/Zener diode configuration.

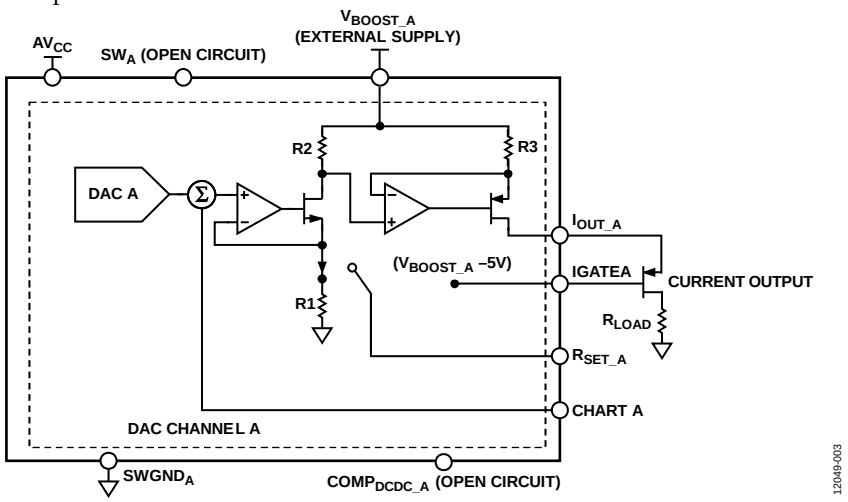

Figure 3. Configuration of a Channel using IGATE (AD5757 or AD5737)

METHOD 2—CONNECTING V_{BOOST} TO AV_{DD}

With Method 2, although no extra components are required, all power is dissipated on chip. Users must be aware of the maximum allowed power dissipation and ambient temperatures if this method is used. Exceeding the absolute maximum ratings specified in the data sheet can damage components.

V_{BOOST} must be powered for both voltage and current output ranges. V_{BOOST} can be tied to AV_{DD} as long as sufficient headroom is maintained between V_{BOOST} and the output per the formula in Table 2.

Leave the SWx and $COMP_{DCDC\_A}$ pins open circuit. Tie AV_{CC} to DV_{DD}. This maintains the voltage on the AV_{CC} pin above the most negative supply, AV_{SS} or 0 V (this applies only to the AD5755-1, AD5737, and AD5757). If the voltage on the AV_{CC} pin is equal to or below the most negative voltage, it can result in latch-up. See Table 2 for recommended supplies for the AV_{CC} and V_{BOOST} rails. All other pins are set up in the same manner as when the dynamic power control function is used. Details are outlined in the Pin Configuration section and Layout Guidelines section of the AD5755 data sheet.

Note that if dynamic power control is not used, then it is of even greater importance to understand the effects of power dissipation.

The AD5755 is packaged in a 64-lead, 9 mm × 9 mm LFCSP. The thermal impedance, θ_{JA}, is 28°C/W. It is important that the device is not operated under conditions that exceed the junction temperature limit (125°C).

Worst-case conditions occur when the AD5755 is at maximum V_{BOOST} (33 V) and driving the maximum current (24 mA) to ground (R_{LOAD} = 0Ω). The quiescent current of the AD5755 must also be taken into account.

The calculations in Table 3 estimate maximum power dissipation under these worst-case conditions, and determine maximum ambient temperature based on this information. These figures assume that proper layout and grounding techniques are followed to minimize power dissipation as outlined in the Layout Guidelines section of the AD5755 data sheet. It also refers to the operating currents as specified in the AD5755 data sheet.

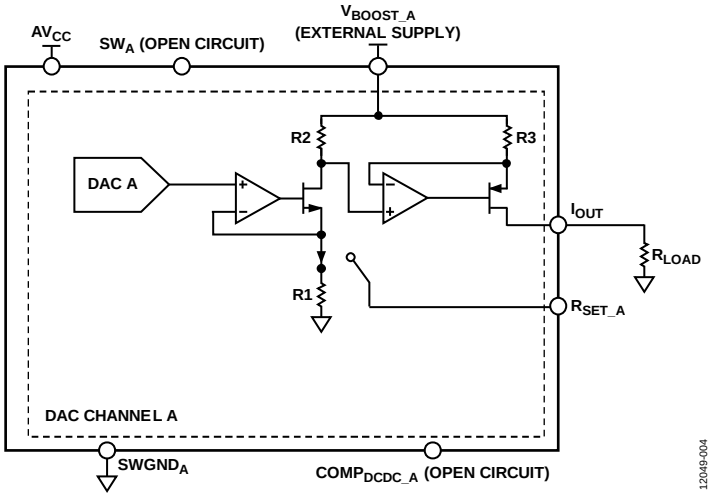

Figure 4. AD5755 without Dynamic Power Control on One Channel

Table 2. Changes in Power Supplies

Parameter	Recommended Minimum/Maximum Voltage
AV_{CC}	DV_{DD} to 5.5 V
V_{BOOST}	7.4 V (minimum) to 33 V (maximum) Current output ($I_{OUT} \times R_{LOAD}$) + Headroom Typically 2.4 V headroom, maximum 2.7 V headroom Voltage output Typically 15 V, maximum V_{OUT} + headroom Maximum 2.2 V headroom

Table 3. Thermal and Supply Conditions (Assuming AV_{SS} = −15 V, AV_{CC} = 5 V, and AV_{DD}/V_{BOOST} = 33 V)

Parameter	Calculation
Maximum Allowable Power Dissipation when Operating at an Ambient Temperature of 85°C	$\frac{T_{JMAX} - T_A}{\theta_{JA}} = \frac{125 - 85}{28} = 1.42\ W$
Maximum Allowable Ambient Temperature—One Channel	AV_{DD} 33 V × 0.0075 A = 0.2475 W AV_{SS} −15 V × 0.0017 A = 0.0255 W AV_{CC} 5 V × 0.001 A = 0.005 W V_{BOOST}[1] (1 channel) 33 V × 0.025 A = 0.825 W Total (1 channel) 1.103 W Temperature increase 1.103 × 28 = 30.9°C Maximum ambient temperature 125°C − 30.9°C = 94.1°C
Maximum Allowable Ambient Temperature—Four Channels	AV_{DD} 33 V × 0.0075 A = 0.2475 W AV_{SS} −15 V × 0.0017 A = 0.0255 W AV_{CC} 5 V × 0.001 A = 0.005 W V_{BOOST}[1] (4 channels) (33 V × 0.025 A) × 4 = 3.3 W Total (4 channels) 3.578 W Temperature increase 3.578W × 28 = 100.18°C Maximum ambient temperature 125°C − 100.18°C = 24.816°C

[1]Includes 1 mA V_{BOOST} quiescent current.

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