ANALOG DEVICES

Circuit Note
CN-0318

Circuits from the Lab™ Reference Circuits

Circuits from the Lab™ reference circuits are engineered and tested for quick and easy system integration to help solve today's analog, mixed-signal, and RF design challenges. For more information and/or support, visit www.analog.com/CN0318.

Devices Connected/Referenced	
AD5760	Ultra Stable, 16-Bit, Voltage Output DAC
AD8675/ AD8676	Ultra Precision, 36 V, 2.8 nV/√Hz, Single/Dual Rail-to-Rail Output Op Amp
ADR4550	Ultralow Noise, High Accuracy 5 V Voltage Reference

16-Bit, Linear, Ultra Stable, Low Noise, Bipolar ±10 V DC Voltage Source

EVALUATION AND DESIGN SUPPORT

Circuit Evaluation Boards

AD5760 Circuit Evaluation Board (EVAL-AD5760SDZ)

System Demonstration Platform (EVAL-SDP-CB1Z)

Design and Integration Files

Schematics, Layout Files, Bill of Materials

CIRCUIT FUNCTION AND BENEFITS

The circuit, shown in Figure 1, is a 16-bit, ultra stable, low noise, precision, bipolar (±10 V) voltage source requiring a minimum number of precision external components.

Maximum integral nonlinearity (INL) is ±0.5 LSB, and maximum differential nonlinearity (DNL) is ±0.5 LSB for the AD5760 voltage output DAC (B-grade).

The complete system has less than 0.1 LSB peak-to-peak noise and drift measured over a 100 second interval. The circuit is ideal for medical instrumentation, test and measurement, and industrial control applications where precision low drift voltage sources are required.

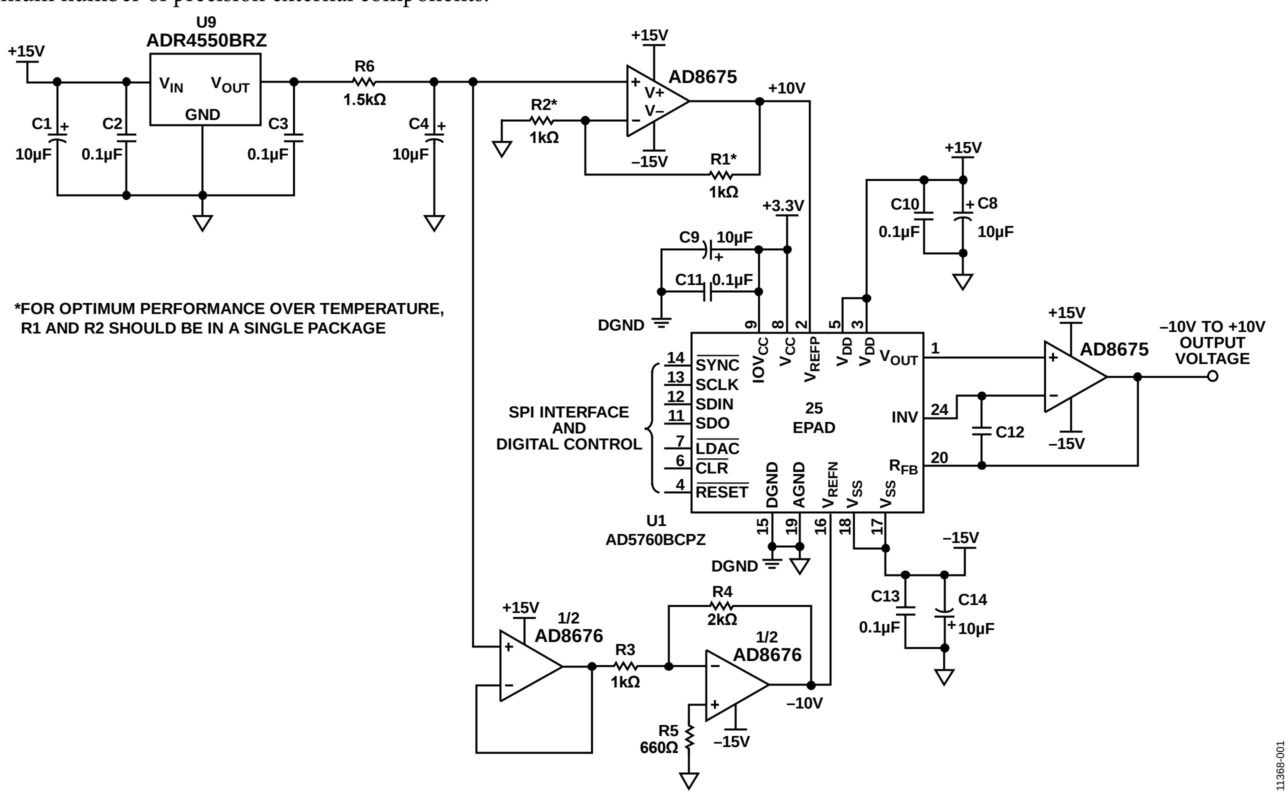

Figure 1. 16-Bit Accurate, ±10 V Voltage Source (Simplified Schematic: All Connections and Decoupling Not Shown)

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CIRCUIT DESCRIPTION

The circuit in Figure 1 is based on the AD5760, a true 16-bit, un-buffered voltage output DAC that operates from a bipolar supply of up to 33 V. The AD5760 accepts a positive reference input range of 5 V to V_{DD} − 2.5 V and a negative reference input range of V_{SS} + 2.5 V to 0 V. The AD5760 offers a relative accuracy specification of ±0.5 LSB maximum, and operation is guaranteed monotonic with a ±0.5 LSB DNL maximum specification. Output noise is 8 nV/√Hz, and the AD5760 also exhibits an extremely long term linearity error stability of 0.00625 LSB.

Figure 1 shows the AD5760 configured in the unity gain mode with amplifier input bias current compensation in order to generate a symmetrical bipolar output voltage range. This mode of operation uses an external output operational amplifier, as well as on-chip resistors (see AD5760 data sheet), to provide the input bias current compensation. These internal resistors are thermally matched to each other and to the DAC ladder resistance, resulting in ratiometric thermal tracking.

The AD8675 precision op amp has low offset voltage (75 µV maximum) and low noise (typical values are 2.8 nV/√Hz; and 0.1 µV p-p, 0.1 Hz to 10 Hz) and is an optimum output buffer for the AD5760. The AD5760 has two internal matched 6.8 kΩ feedforward and feedback resistors, which can either be connected to the AD8675 op amp to provide a 10 V offset voltage for a ±10 V output swing, or connected in parallel to provide bias current cancellation. In this example, a bipolar ±10 V output is shown, and the resistors are used for bias current cancellation. The internal resistor connection is controlled by setting a bit in the AD5760 control register (see the AD5760 data sheet).

The ADR4550 is a high precision voltage reference that offers excellent temperature stability (2 ppm/°C maximum , B-grade) and ultra-low output voltage noise (2.8 µV p-p, 0.1 Hz to 10 Hz). These features make it an ideal reference for the AD5760.

In order to obtain a ±10 V output voltage range, the +5 V reference voltage from the ADR4550 is amplified to ±10 V (as shown in Figure 1) by using the AD8675 and AD8676 (dual AD8675).

The output buffer is again the AD8675, used for its low noise and low drift. This amplifier in conjunction with the AD8676 (AD8675 dual) are used to amplify the +5 V reference voltage from the low noise ADR4550 to +10 V and −10 V respectively. R1, R2, R3 and R4 in this gain circuit are precision metal foil resistors with 0.01% tolerance and a temperature coefficient resistance of 0.6 ppm/°C. R6 and C4 form a low-pass filter with a cutoff frequency of approximately 10 Hz. The purpose of this filter is to attenuate voltage reference noise.

The two AD8675 op amps in the circuit can be replaced with a single AD8676 dual amplifier if desired. However the EVAL-AD5760SDZ board was designed for flexibility in the output stage, therefore two AD8675 op amps were chosen.

The digital input to the circuit is serial and is compatible with standard SPI, QSPI, MICROWIRE®, and DSP interface standards.

Linearity Measurements

The precision performance of the circuit shown in Figure 1 is demonstrated on the EVAL-AD5760SDZ evaluation board using an Agilent 3458A multimeter. Figure 2 shows that the integral nonlinearity as a function of DAC code is well within the specification of ± 0.5 LSB.

Figure 3 shows that the differential nonlinearity as a function of DAC code is within the ±0.5 LSB specification.

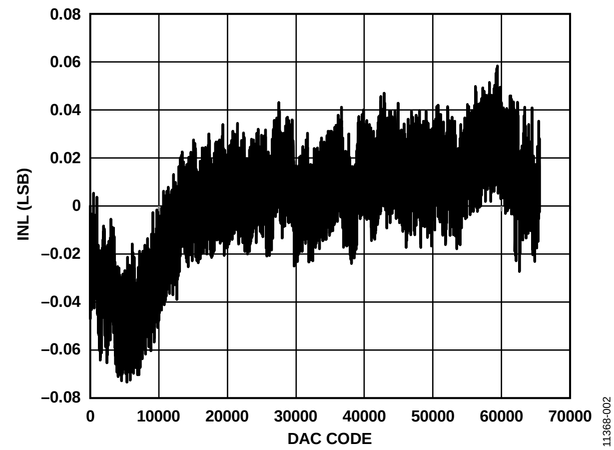

Figure 2. Integral Nonlinearity vs. DAC Code

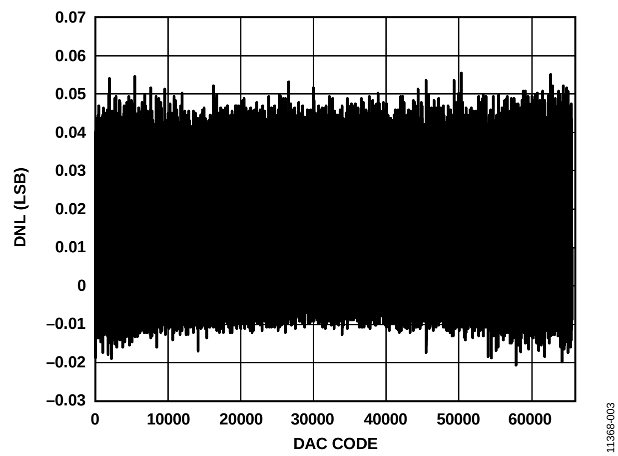

Figure 3. Differential Nonlinearity vs. DAC Code

Noise Drift Measurements

To realize high precision, the peak-to-peak noise at the circuit output must be maintained well below 1 LSB, which is 152 µV for 16-bit resolution and a +10 V unipolar voltage range, and 305 µV for a 20 V peak-to-peak voltage range.

A real world application will not have a high-pass cutoff at 0.1 Hz to attenuate the 1/f noise, but will include frequencies down to dc in its pass band. With this in mind, the measured peak-to-peak noise is shown in Figure 4 for a +10 V unipolar voltage range and in Figure 5 for a ±10 V bipolar voltage range. In both cases, the noise at the output of the circuit was measured over a period of 100 seconds, effectively including frequencies as low as 0.01 Hz in the measurement.

Figure 4 shows the noise performance of the signal chain for a 10 V output span (1 LSB = 152 µV). The 10 V range is obtained by grounding the V_{REFN} input of the AD5760.

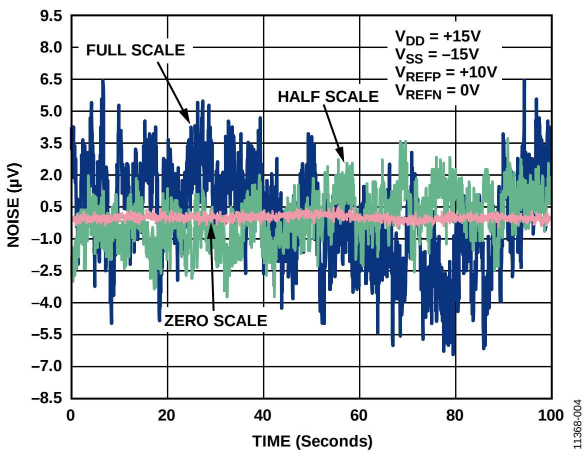

Figure 4. DAC Output Voltage Noise Measured Over 100 Second Period for Full Scale (Blue), Half Scale (Green), and Zero Scale (Red) with ADR4550 Voltage Reference for a 10 V Peak-to-Peak Unipolar Output Voltage Range

The peak-to-peak output noise for the 10 V range in Figure 4 is summarized below:

- Zero scale = 0.96 µV p-p = 0.006 LSB p-p
- Half scale = 7.46 µV p-p = 0.05 LSB p-p
- Full scale = 12.88 µV p-p = 0.08 LSB p-p

The zero-scale output voltage exhibits the lowest noise because it represents the noise from the DAC core only because the V_{REFN} input is connected to ground. The noise contribution from each voltage reference path is attenuated by the DAC when the zero-scale code is selected.

At low frequencies, temperature drift and thermocouple effects become contributors to noise. These effects can be minimized by choosing components with low thermal coefficients. In this circuit, the main contributor to low frequency 1/f noise is the voltage reference. It also exhibits the greatest temperature coefficient value in the circuit of 2 ppm/°C.

Figure 5 shows the noise performance of the signal chain for a 20 V output span (1 LSB = 305 µV).

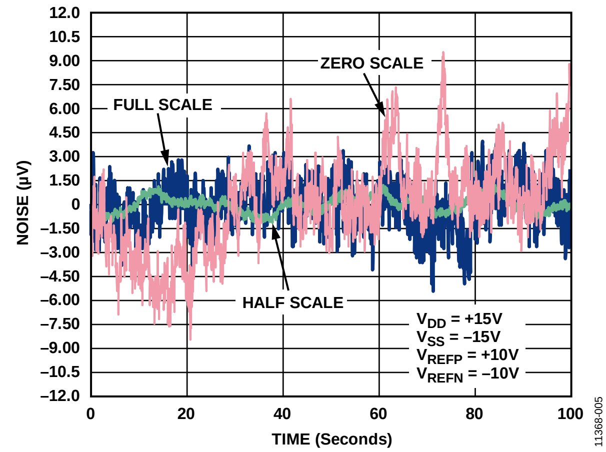

Figure 5. DAC Output Voltage Noise Measured Over 100 Second Period for Full Scale (Blue), Half Scale (Green), and Zero Scale (Red) with ADR4550 Voltage Reference for a 20 V Peak-to-Peak Bipolar Output Voltage Range

The peak-to-peak noise for the 20 V range in Figure 5 is summarized below:

- Zero scale = 18 µV p-p = 0.06 LSB p-p
- Half scale = 2.47 µV p-p = 0.008 LSB p-p
- Full scale = 9.22 µV p-p = 0.03 LSB p-p

The noise is lowest at half scale because the DAC core provided the most attenuation of the references at this point.

The noise at zero scale is larger than full scale because the negative reference passes through an additional buffer stage.

Complete schematics and layout of the printed circuit board can be found in the CN-0318 Design Support package: www.analog.com/CN0318-DesignSupport.

COMMON VARIATIONS

The AD5760 will support a wide variety of output ranges from 0 V to +5 V up to ±10 V, and values in between. The unity-gain mode with amplifier input bias compensation, as shown in Figure 1, can be used for symmetrical or asymmetrical output ranges by applying the required references at V_{REFP} and V_{REFN}. These unity-gain modes are selected by setting the RBUF bit of the AD5760 internal control register to a Logic 1. The gain-of-2 configuration, can be used if a symmetrical output range is required from a single-ended reference input, with V_{REFN} = 0 V. This mode is selected by setting the RBUF bit of the AD5760 internal control register to a Logic 0.

The two AD8675 op amps can be replaced with the dual AD8676 if desired.

CIRCUIT EVALUATION AND TEST

Equipment Required

- System Demonstration Platform (EVAL-SDP-CB1Z)
- EVAL-AD5760SDZ evaluation board and software
- Agilent 3458A multimeter
- PC (Windows 32-bit or 64-bit OS)
- National Instruments GPIB to USB-B interface cable
- SMB cable (1)

Software Installation

The AD5760 evaluation kit includes self-installing software on a CD. The software is compatible with Windows XP (SP2) and Vista (32-bit and 64-bit). If the setup file does not run automatically, run the **setup.exe** file from the CD. The complete hardware and software setup procedure is contained in User Guide UG-436.

Install the evaluation software before connecting the evaluation board and SDP board to the USB port of the PC to ensure that the evaluation system is correctly recognized when connected to the PC.

1. After installation from the CD is complete, power up the AD5760 evaluation board as described in User Guide UG-436. Connect the SDP board (via either Connector A or Connector B) to the AD5760 evaluation board and then to the USB port of your PC using the supplied cable.
2. When the evaluation system is detected, proceed through any dialog boxes that appear. This completes the installation.

Functional Diagram

A functional diagram of the test setup is shown in Figure 7.

Power Supplies

The following external supplies must be provided:

- 3.3 V between the VCC and DGND inputs on Connector J1 for the digital supply of the AD5760. Alternatively, place Link 1 in Position A to power the digital circuitry from the USB port via the SDP board (default).
- +12 V to +16.5 V between the VDD and AGND inputs of J2 for the positive analog supply of the AD5760.
- −12 V to −16.5 V between the VSS and AGND inputs of J2 for the negative analog supply of the AD5760.

Figure 6. Evaluation Software Main Window

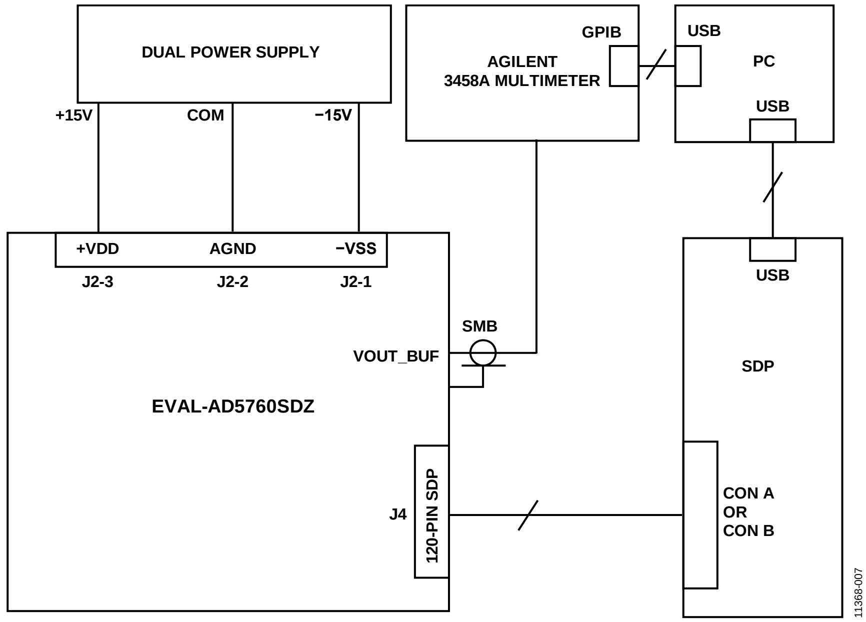

Figure 7. Functional Block Diagram of Test Setup

Default Link Option Setup

The default link options are listed in Table 1. By default, the board is configured with V_{REFP} = +10 V and V_{REFN} = −10 V for a ±10 V output range.

Table 1. Default Link Options

Link No.	Option
LK1	A
LK2	B
LK3	A
LK4	Removed
LK5	Removed
LK6	Removed
LK7	Removed
LK8	C
LK9	Inserted
LK11	Inserted

In order to configure the board for the circuit shown in Figure 1, the following changes must be made to the default link configuration in Table 1:

1. Place LK3 in position B.
2. Insert LK4.
3. Place LK8 in position C.

These changes configure the output buffer amplifier for a gain of 1 and compensate the amplifier input bias current. Refer to User Guide UG-436 for more information on the EVAL-AD5760SDZ test setup.

Test

The VOUT_BUF SMB connector is connected to the Agilent 3458A multimeter. The linearity measurements are run using the Measure DAC Output Tab on the AD5760 GUI.

The noise drift measurement is measured on the VOUT_BUF SMB connector also. The output voltage is set using the Program Voltage tab in the AD5760 GUI. The peak-to-peak noise drift is measured over 100 seconds.

For more details on the definitions and how to calculate the INL, DNL, and noise from the measured data, see the AD5760 data sheet and also the following reference: *Data Conversion Handbook*, "Testing Data Converters," Chapter 5, Analog Devices.

LEARN MORE

CN0318 Design Support Package: www.analog.com/CN0318-DesignSupport

Egan, Maurice. "The 20-Bit DAC Is the Easiest Part of a 1-ppm-Accurate Precision Voltage Source," *Analog Dialogue*, Vol. 44, April 2010.

Kester, Walt. 2005. *The Data Conversion Handbook*. Analog Devices. Chapters 3, 5, and 7.

MT-015 Tutorial, *Basic DAC Architectures II: Binary DACs*. Analog Devices.

MT-016 Tutorial, *Basic DAC Architectures III: Segmented DACs*. Analog Devices.

MT-031 Tutorial, *Grounding Data Converters and Solving the Mystery of AGND and DGND*. Analog Devices.

MT-035 Tutorial, *Op Amp Inputs, Outputs, Single-Supply, and Rail-to-Rail Issues.* Analog Devices.

MT-101 Tutorial, *Decoupling Techniques*. Analog Devices. Voltage Reference Wizard Design Tool.

CN-0177 Circuit Note, *18-Bit, Linear, Low Noise, Precision Bipolar ±10 V DC Voltage Source.*

CN-0191 Circuit Note, *20-Bit, Linear, Low Noise, Precision, Bipolar ±10V DC Voltage Source.*

CN-0200 Circuit Note, *18-Bit, Linear, Low Noise, Precision Bipolar ±10 V DC Voltage Source.*

CN-0257 Circuit Note, *20-Bit, Linear, Low Noise, Precision Unipolar +10 V DC Voltage Source.*

User Guide UG-436, *Evaluation Board for a 16-Bit Serial Input, Voltage Output DAC with Integrated Precision Reference Buffer Amplifiers.*

Data Sheets and Evaluation Boards

AD5760 Data Sheet and Evaluation Board

AD8675 Data Sheet

AD8676 Data Sheet

ADR4550 Data Sheet

REVISION HISTORY

5/13—Revision 0: Initial Version

CN11368-0-5/13(0)