

## Low Noise, Dual-Supply Solution Using the **ADP5070** for the Precision **AD5761R** Bipolar DAC in Single-Supply Systems

by Estibaliz Sanz Obaldia and James Jasper Macasaet

### INTRODUCTION

This application note describes how a system with a single unipolar supply can be used to power components requiring dual (bipolar) power supplies. The **AD5761R**, a bipolar digital-to-analog converter (DAC), requires dual supplies to provide bipolar output voltage ranges. The examples shown in this application note use the **ADP5070** dc-to-dc switching regulator with the **ADP7142** and **ADP7182** complementary metal-oxide semiconductor (CMOS) low dropout (LDO) linear regulators, LC filters, and resistor dividers to generate dual supplies from a 5 V single voltage supply to power the **AD5761R**.

Together, the 5 V power supply and combination of the **ADP5070**, **ADP7142**, **ADP7182**, and/or LC filters provide a power supply solution for DACs that output unipolar and bipolar voltage ranges. This solution provides noise performance similar to that of a DAC being supplied by a dual bench power supply.

The power spectrum analysis, voltage output noise, and ac performance data included in this application note support the performance of this solution.

The proposed supply configurations yield different results depending on which tests a user performs on the system. For instance, a configuration that incorporates the **ADP5070** supply and additional LC filters is optimal for reducing the spectral noise from 10 Hz to 10 kHz when the internal reference of the DAC is used. An external supply, on the other hand, provides the best result for a spectral analysis using an external reference. Results gathered with the external supply were used as the baseline measurement for all the supply configurations. For a higher frequency bandwidth (10 kHz to 10 MHz), adding CMOS LDO linear regulators to the **ADP5070** supply offers the best spectral noise performance. The resulting output spectrum of the DAC for an LC filter and LDO configuration, which is used to reduce the switching noise from the **ADP5070**, is comparable to an external supply configuration.

The sensitivity to noise of the system determines the amount of circuitry required to reduce the noise to acceptable levels. No significant difference is observable between the output noise measurements at 0.1 Hz to 10 Hz due to the inherent noise rejection capabilities of the **AD5761R**. Using additional LDOs significantly reduces the **AD5761R** output noise, resulting in a performance comparable to the baseline measurement.

For the ac performance tests, the **AD5761R** performs within the data sheet specifications under all presented supply configurations.

The **AD5761R** is a 16-bit DAC that integrates an output amplifier, a reference buffer, and a maximum 5 ppm/°C temperature coefficient internal reference. The **AD5761R** operates from a unipolar supply of up to 30 V or a bipolar supply of  $-16.5$  V to 0 V for  $V_{SS}$  and 4.75 V to 16.5 V for  $V_{DD}$ . The **AD5761R** offers eight programmable output ranges, 35 nV/√Hz noise, and a 7.5 μs settling time on selected ranges.

The **ADR4525**, a 2.5 V voltage reference, is used across the tests presented in this application note as an external reference to cover applications that require ultralow noise voltage references.

The **ADP5070** is a dual, high performance, dc-to-dc regulator that generates independently regulated positive and negative rails. The input voltage range of 2.85 V to 15 V supports a wide variety of applications. The integrated main switch in both regulators enables generation of an adjustable positive output voltage up to +39 V and a negative output voltage down to  $-39$  V below input voltage. The **ADP5070** operates at a pin selected 1.2 MHz/2.4 MHz switching frequency. In addition, the regulator has slew rate control circuitry for the metal-oxide semiconductor field effect transistor (MOSFET) driver stage to reduce electromagnetic interference (EMI).

The **ADP7142** is an LDO linear regulator that operates from 2.7 V to 40 V and provides up to 200 mA of output current. This high input voltage LDO linear regulator is ideal for regulating high performance analog and mixed-signal circuits operating rails from 40 V down to 1.2 V. Using a proprietary architecture, the device provides high power supply rejection, low noise, and achieves excellent line and load transient response. The **ADP7142** regulator output noise is 11 μV rms at 5 V or less with the ability to adjust the output voltage on the 5 V option to 15 V.

The **ADP7182** is an LDO linear regulator that operates from  $-2.7$  V to  $-28$  V and provides up to  $-200$  mA of output current. This high negative input voltage LDO linear regulator is ideal for regulating high performance analog and mixed-signal circuits operating rails from  $-27$  V down to  $-1.2$  V.

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## REVISION HISTORY

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### 12/15—Revision 0: Initial Version

# BIPOLAR DACs

## BIPOLAR RANGE GENERATION

Applications such as test and measurement, data acquisition, actuator control, and industrial automation require a variety of voltage ranges because the voltage range can vary during operation. Single-supply DACs, such as multiplying DACs or nanoDACs, can be used to generate bipolar output ranges. However, generating bipolar output ranges using these DACs requires the addition of external discrete components such as op amps or resistors. In this type of solution, the basic configuration consists of a general-purpose DAC followed by an amplifying stage and an offset stage. Figure 1 shows an example of a discrete solution using a single-supply DAC. A discrete solution is acceptable in applications for which minimum board area, overall system high performance, and low cost are not essential. An estimated area of 23 mm<sup>2</sup> is required to implement the circuit in Figure 1. This estimate takes into account any errors resulting from the increasing number of external components that degrade the quality of the final output signal. Adding expensive precision resistors to optimize the system performance increases cost. Bipolar DACs are capable of generating bipolar outputs but require bipolar power supplies to do so. Additionally, not all bipolar DACs integrate a reference, an

output buffer, or a reference buffer to provide a complete solution. In these cases, design time, factor form, and the selection process of the correct devices increase the complexity of the application. For example, selecting a voltage reference for a bipolar DAC that meets the required specifications increases design and evaluation time. Selecting an integrated solution removes this overhead.

The **AD5761R** is a complete solution that provides all the required functionality and integrates a buffered reference and an output buffer. Decoupling capacitors are the only external components required. The proposed configurations support applications in which only a single 5 V supply is available. A dc-to-dc switching regulator, LC filters, LDO linear regulators, and/or resistor dividers are used to support the operation of the **AD5761R**. Figure 2 shows the **AD5761R**, which integrates the external components required in Figure 1 to generate the bipolar ranges. The **AD5761R** is available in a small, 3 mm × 3 mm LFCSP.

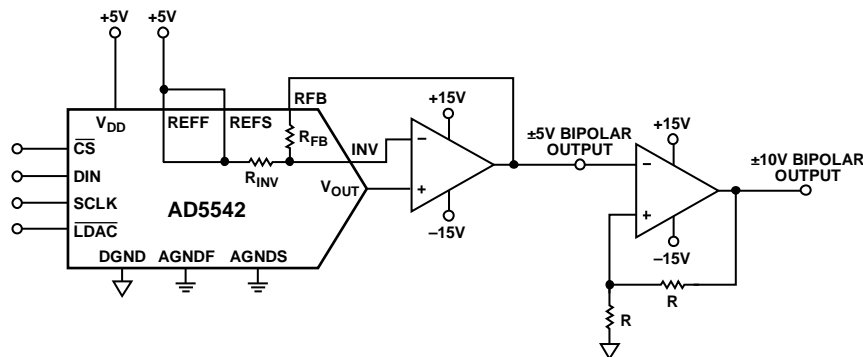
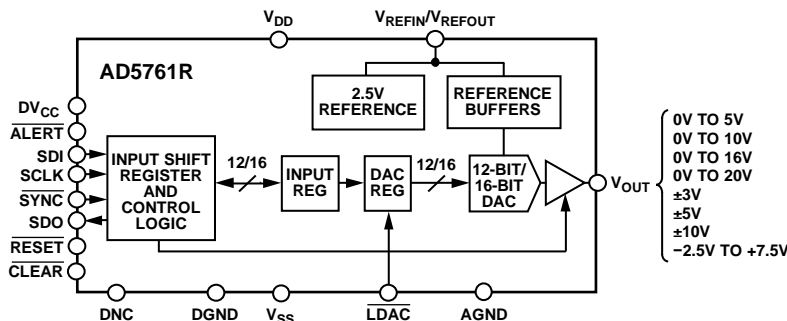


Figure 1. Single-Supply DAC Configured in ±10 V



NOTES  
1. DNC = DO NOT CONNECT. DO NOT CONNECT TO THIS PIN.

Figure 2. **AD5761R** Functional Block Diagram

# SINGLE-SUPPLY SYSTEMS CONFIGURED TO SUPPORT THE AD5761R

## CIRCUIT DESCRIPTION

The AD5761R DAC shown in Figure 2 provides four unipolar output ranges (0 V to 5 V, 0 V to 10 V, 0 V to 16 V, and 0 V to 20 V) and four bipolar output ranges ( $\pm 3$  V,  $\pm 5$  V,  $\pm 10$  V, and  $-2.5$  V to  $+7.5$  V).

In this application note, the AD5761R is powered up with specific supply voltages to cover all eight possible output ranges. Because the AD5761R requires a minimum 1 V headroom/footroom in addition to the voltage supply, apply a minimum  $V_{DD}$  of 21 V and maximum  $V_{SS}$  of  $-11$  V to the DAC. When the DAC is used to output lower output ranges, lower supply voltages can be supplied.

This application note presents two supply configurations that provide the required  $V_{DD}$  and  $V_{SS}$  voltages. The level of acceptable noise in the system determines the best approach for supplying the DAC. The two configurations comprise the following:

- The ADP5070 in conjunction with the resistor ladders. In this case, insert the LK1, LK2, LK7, and LK8 links.
- The ADP5070 in conjunction with the resistor ladders and the linear regulators (ADP7142 and ADP7182). In this case, remove the LK1, LK2, LK7, and LK8 links.

The LK1 and LK2 links bypass the linear regulators in the circuit, and the LK7 and LK8 links determine the voltage available right before these linear regulators. Table 1 lists the voltages available at Test Point A and Test Point B for the LK7 and LK8 link configurations.

Figure 3 shows the power supply configuration for the AD5761R, where  $V_{DD}$  and  $V_{SS}$  are generated by different means from an initial unipolar 5 V single supply.

Table 1. Link Details for Supply Configuration Selection

Link	Link Inserted	Link Removed	Test Conditions/ Comments
LK7	21.1 V	23.2 V	Voltage measured at Test Point A
LK8	$-11$ V	$-13$ V	Voltage measured at Test Point B

The ADR4525 can also externally supply the 2.5 V reference voltage. Refer to Figure 6.

### DC-to-DC Switching Regulator

The ADP5070 output voltages are adjusted to  $+21.1$  V and  $-11$  V when LK7 and LK8 are inserted, respectively. These supply voltages are required for the AD5761R to cover all eight possible programmable output ranges from the DAC.

Figure 3 shows two filter components mainly intended for switching ripple reduction. Inductor L1 and Capacitors C14, C16, and C19 form an LC filter for the positive output, whereas Inductor L2 and Capacitors C15, C17 and C20 are configured on the negative output. These LC filters, located inside the control loop of the regulator, contain values that result in a considerable attenuation at the ripple frequency. Optional second-stage LDO linear regulators are available at the output stage of the switching regulator for further ripple reduction. With the LC filter alone, the AD5761R performs within the data sheet specifications. For applications that require better noise performance, an LDO can be used at the output stage.

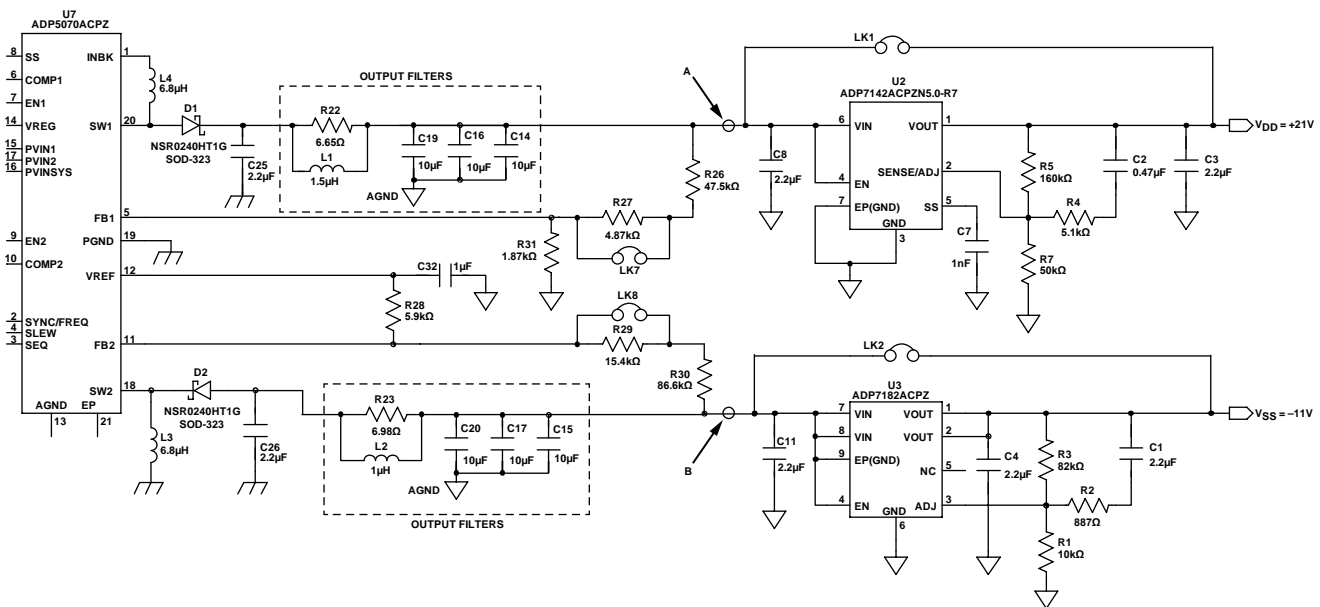


Figure 3. AD5761R Power Supply Configuration

**Linear Regulators**

The ADP5070, in conjunction with the ADP7182 and ADP7142 linear regulators, provides the lowest noise +21 V and -11 V voltage supplies. Note that for this approach, LK1, LK2, LK7, and LK8 are removed.

The ADP5070 provides a positive output voltage of +39 V and a negative output voltage of -39 V. Figure 4 shows the value of the resistors forming the resistor dividers (R26, R27, and R31; and R28, R29, and R30) needed to adjust these voltages to acceptable input voltages for the ADP7142 and ADP7182. Note that a minimum headroom/footroom of 2 V is needed on top of the desired output voltage of the linear regulators.

Both linear regulators, the ADP7142 and the ADP7182, are configured to achieve an output voltage signal with noise as low as possible. As explained in the ADP7182 and ADP7142 data

sheets, two additional components need to be added to the output voltage setting resistor divider to obtain ultralow output noise. C<sub>NR</sub> (C1, C2) and R<sub>NR</sub> (R2, R4) are connected in parallel with R<sub>FB1</sub> (R3, R5) to reduce the ac gain of the error amplifier.

Adding linear regulators to the output stage of the switching regulator helps to reduce noise in the DAC output due to the switching regulator that is not removed by the passive filter.

**Resistor Dividers**

Figure 5 shows, by means of resistor dividers, the option to adjust the positive and negative output voltages of the ADP5070 to the required +21 V V<sub>DD</sub> and -11 V V<sub>SS</sub> voltage supplies for the AD5761R. There are no linear regulators involved in this configuration, for which the LK1, LK2, LK7, and LK8 links are inserted.

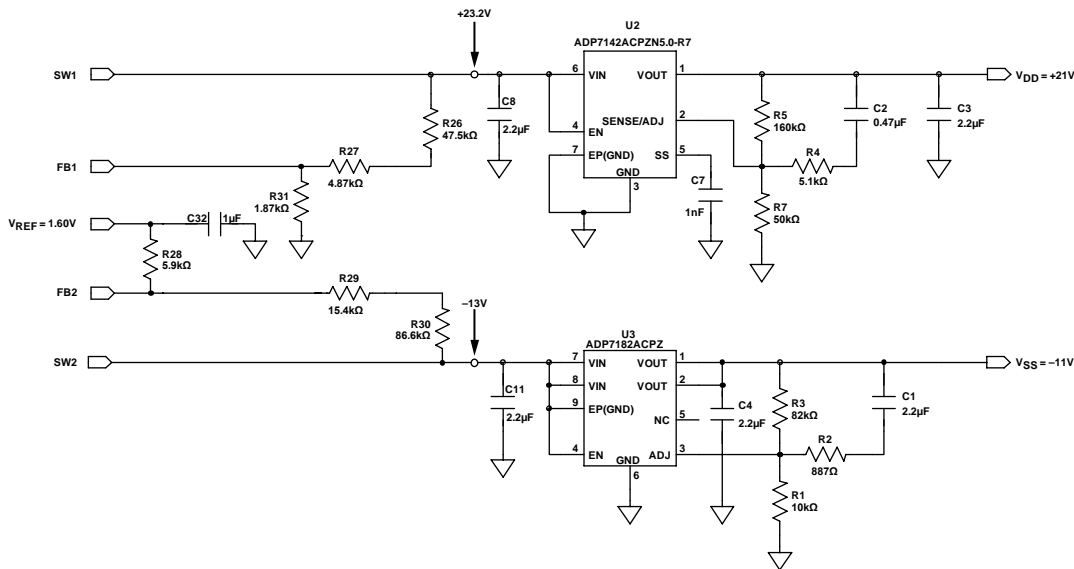


Figure 4. AD5761R Supply Configuration with ADP5070 and Linear Regulators

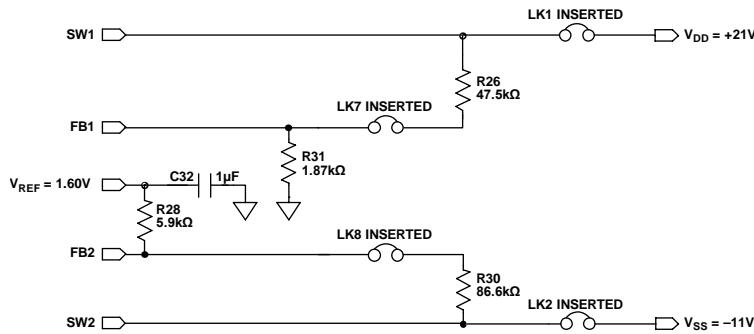


Figure 5. AD5761R Supply Configuration with ADP5070 and Resistor Dividers

**DV<sub>CC</sub> Digital Supply**

Figure 6 shows how to digitally supply the AD5761R from the external 5 V voltage signal. A less noisy voltage signal generated by the ADP5070 and adjusted by an ADP7142 regulator can also be considered.

**Reference Voltage**

The AD5761R offers a 2.5 V, 5 ppm/°C internal voltage reference, which is on by default. Alternatively, Figure 6 shows two possible

external sources to supply the DAC depending on the position of LK4.

LK4 can be shorted to Position A, where an external voltage is input to the V<sub>REFIN</sub>/V<sub>REFOUT</sub> SMB connector. When using the internal reference, 2.5 V is available in this connector for external use.

If LK4 is shorted to Position C, the reference voltage is sourced by the ADR4525 ultralow noise, high accuracy voltage reference.

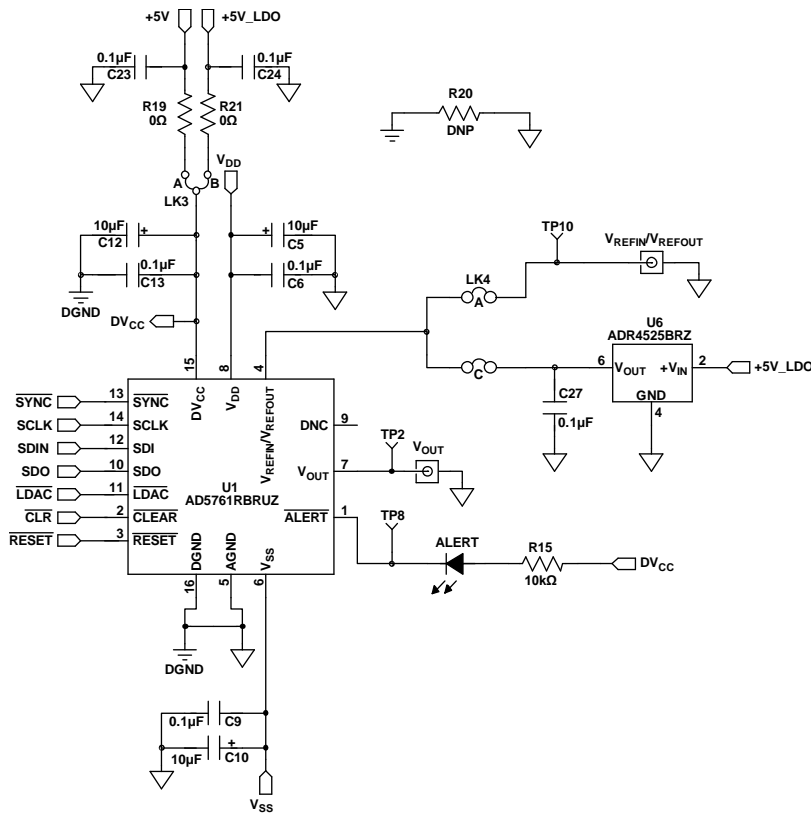


Figure 6. AD5761R Connections

13102-006

## MEASUREMENTS AND RESULTS

### ADP5070 CONFIGURATION

To provide the highest possible ripple amplitude and obtain results for the worst case scenario, the switching frequency of the [ADP5070](#) is set to 1.2 MHz with a fast slew mode.

### AD5761R POWER SUPPLY CONFIGURATIONS

The series of measurements presented in this section show the [AD5761R](#) DAC tested at three data codes (zero-scale, half-scale, and full-scale) for a  $\pm 10$  V output voltage range, which is a representative output range for this bipolar DAC. The [AD5761R](#) is powered up under four different supply configurations across the series of measurements.

- External supply
- DC-to-dc switching regulator ([ADP5070](#)) and LC output filter
- DC-to-dc switching regulator ([ADP5070](#)) followed by CMOS LDO linear regulators ([ADP7142](#) and [ADP7182](#)) (this supply configuration is not included on the ac performance test)
- DC-to-dc switching regulator ([ADP5070](#)) with LC output filter, followed by CMOS LDO linear regulators ([ADP7142](#) and [ADP7182](#))

The performance of the [AD5761R](#) is also tested with the internal reference of the DAC and with the [ADR4525](#).

### DAC OUTPUT SPECTRAL RESPONSE

The results detailed in this section show how the DAC output noise spectrum varies depending on the supply configuration selected. Table 2 and Table 3 show the maximum output spectral response level from the spectral analysis presented in Figure 7 to Figure 20.

Table 4 shows the maximum DAC output spectral response level at a 1.2 MHz switching frequency over a 10 kHz to 10 MHz frequency range. Adding an LC filter to the supply configuration maintains the [AD5761R](#) within the set specification of 20.6 dB $\mu$ V, which represents a 0.1 LSB level. Adding an LDO as a second-stage filter further reduces the ripple to a level comparable to an external supply operation, allowing the DAC to perform with a minimal noise output.

Table 2. [AD5761R](#) Maximum Output Spectral Response Level per DAC Data Code (dB $\mu$ V), 10 Hz to 10 kHz

Power Supply Configuration	Internal Reference			External Reference		
	Zero-Scale	Half-Scale	Full-Scale	Zero-Scale	Half-Scale	Full-Scale
External Supply	8.00	3.63	7.04	2.60	3.39	1.45
<a href="#">ADP5070</a> and LC Output Filters	6.57	2.41	8.01	2.58	3.34	3.59
<a href="#">ADP5070</a> , LC Output Filters, and CMOS LDO Linear Regulators	7.4	3.91	5.96	1.68	2.49	3.32

Table 3. [AD5761R](#) Maximum Output Spectral Response Level per DAC Code (dB $\mu$ V), 10 kHz to 10 MHz

Power Supply Configuration	Internal Reference			External Reference		
	Zero-Scale	Half-Scale	Full-Scale	Zero-Scale	Half-Scale	Full-Scale
External Supply	2.23	-1.57	0.58	9.33	-1.55	10.55
<a href="#">ADP5070</a> and LC Output Filters	1.19	-0.62	4.37	10.27	1.73	9.64
<a href="#">ADP5070</a> and CMOS LDO Linear Regulators	1.85	-0.93	0.69	9.89	-0.98	9.22
<a href="#">ADP5070</a> , LC Output Filters, and CMOS LDO Linear Regulators	1.94	-2.20	-0.06	9.99	-1.60	10.03

Table 4. [AD5761R](#) 1.2 MHz Maximum Spectral Output Response Level per DAC Data Code (dB $\mu$ V), 10 kHz to 10 MHz

Power Supply Configuration	Internal Reference			External Reference		
	Zero-Scale	Half-Scale	Full-Scale	Zero-Scale	Half-Scale	Full-Scale
External Supply	-17.07	-17.06	-16.96	-16.49	-17.48	-17.5
<a href="#">ADP5070</a> and LC Output Filters	-14.99	-11.47	-2.44	-15.69	-10.34	-3.62
<a href="#">ADP5070</a> and CMOS LDO Linear Regulators	-16.78	-17.93	-16.68	-17.51	-18.37	-16.63
<a href="#">ADP5070</a> , LC Output Filters, and CMOS LDO Linear Regulators	-17.07	-18.39	-17.64	-16.53	-16.43	-17.01

**External Supply and AD5761R Configuration**

The spectral traces shown in Figure 7 to Figure 10 are used as baseline plots for the subsequent AD5761R DAC and ADP5070 direct switching regulator evaluations. The red dashed line in Figure 7 to Figure 10 represents a threshold limit for the spectral levels. The threshold level is set at 20.6 dB $\mu$ V, which represents a value of approximately 0.1 LSB. In Figure 7 to Figure 20, RBW is the resolution bandwidth, VBW is the video bandwidth, and REF is the reference value. The VBW, generally associated with the video filter of the measurement equipment, leads to better display of the signals of interest; it reduces the noise on the trace while maintaining the floor noise.

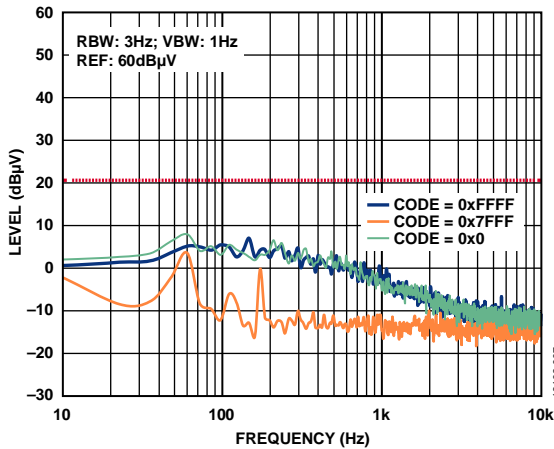


Figure 7. External Supply and AD5761R Configuration Output Spectral Response, Internal Reference (10 Hz to 10 kHz)

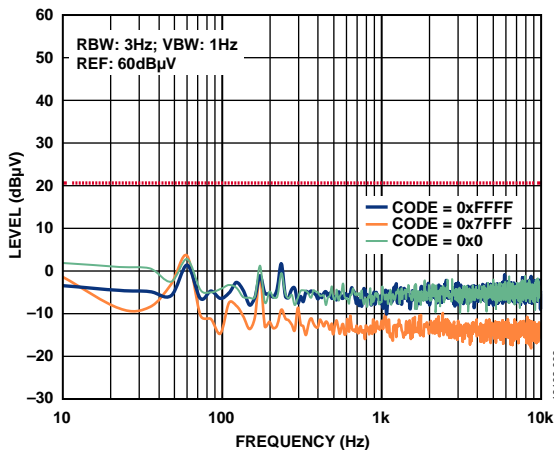


Figure 8. External Supply and AD5761R Configuration Output Spectral Response, External Reference (10 Hz to 10 kHz)

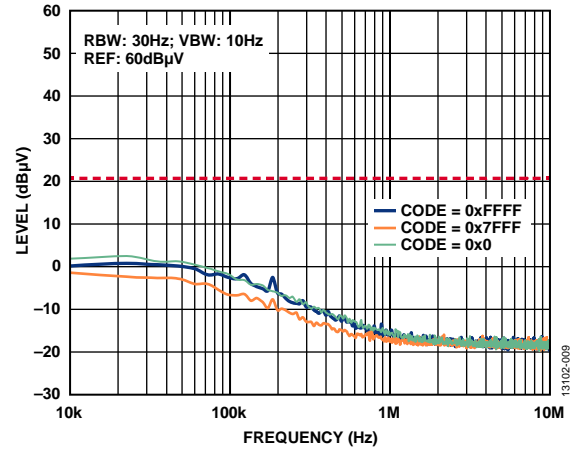


Figure 9. External Supply and AD5761R Configuration Output Spectral Response, Internal Reference (10 kHz to 10 MHz)

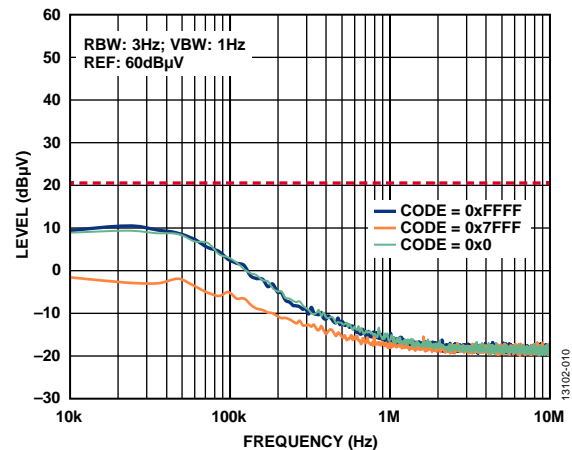


Figure 10. External Supply and AD5761R Configuration Output Spectral Response, External Reference (10 kHz to 10 MHz)



### DC-to-DC Switching Regulator and LC Output Filters Supply Configuration

In this supply configuration, LC filters are used for initial ripple rejection in addition to the [ADP5070](#) direct switching regulator used to generate the bipolar supply ranges. Figure 11 and Figure 12 show the ripple level for a frequency bandwidth of 10 Hz to 10 kHz, and Figure 13 and Figure 14 show the ripple level for a frequency bandwidth of 10 kHz to 10 MHz.

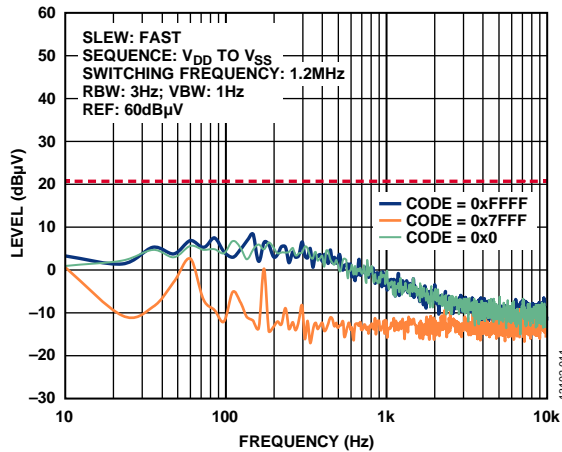


Figure 11. [ADP5070](#), LC Filters, and [AD5761R](#) Supply Configuration Output Spectral Response, Internal Reference (10 Hz to 10 kHz)

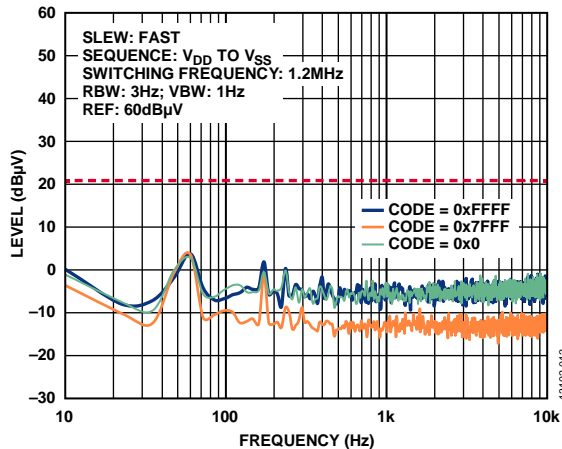


Figure 12. [ADP5070](#), LC Filters, and [AD5761R](#) Supply Configuration Output Spectral Response, External Reference (10 Hz to 10 kHz)

Figure 13 and Figure 14 show a frequency spike at 1 MHz in the frequency bandwidth of 10 kHz to 10 MHz. The LC filter does not sufficiently reduce the amplitude of this ripple coming from the [ADP5070](#) dc-to-dc regulator; therefore, the performance of this power supply solution is not ideal from a spectrum analysis point of view.

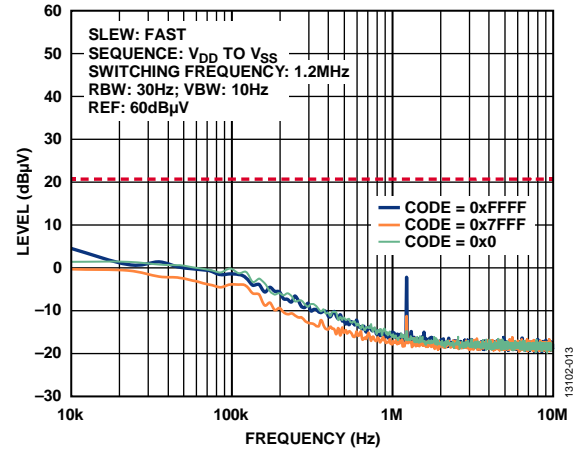


Figure 13. [ADP5070](#), LC Filters, and [AD5761R](#) Supply Configuration Output Spectral Response, Internal Reference (10 kHz to 10 MHz)

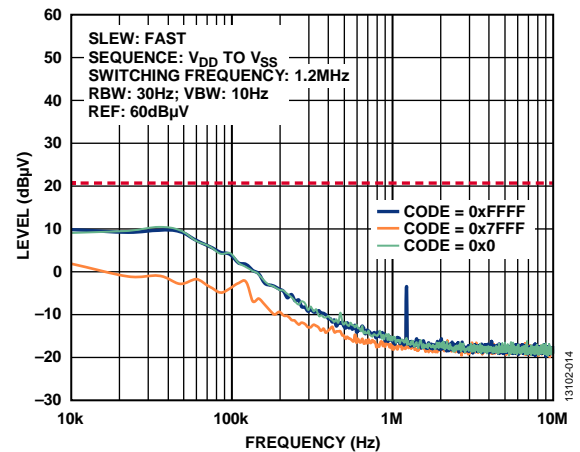


Figure 14. [ADP5070](#), LC Filters, and [AD5761R](#) Supply Configuration Output Spectral Response, External Reference (10 kHz to 10 MHz)

### DC-to-DC Switching Regulator and CMOS LDO Linear Regulators Supply Configuration

Adding LDOs to the output of the [ADP5070](#) dc-to-dc regulator considerably reduces the spike observed at a 1 MHz frequency (see the DC-to-DC Switching Regulator and LC Output Filters Supply Configuration section). This reduction demonstrates that adding an LC filter to the supply circuit is not necessary to obtain an improved performance.

Figure 15 and Figure 16 show the performance of the [ADP5070](#), LDOs, and [AD5761R](#) supply configuration at high frequency.

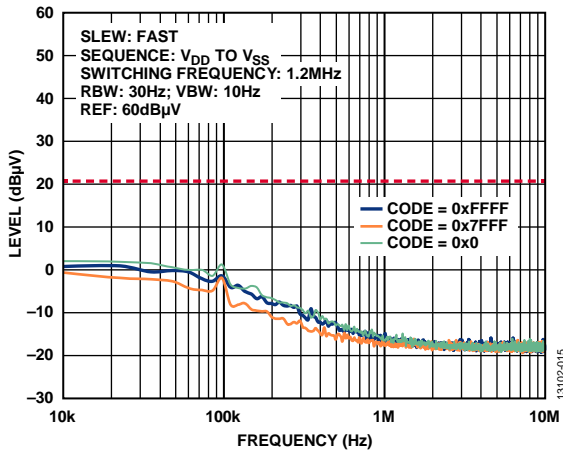


Figure 15. ADP5070, LDOs, and AD5761R Supply Configuration Output Spectral Response, Internal Reference (10 kHz to 10 MHz)

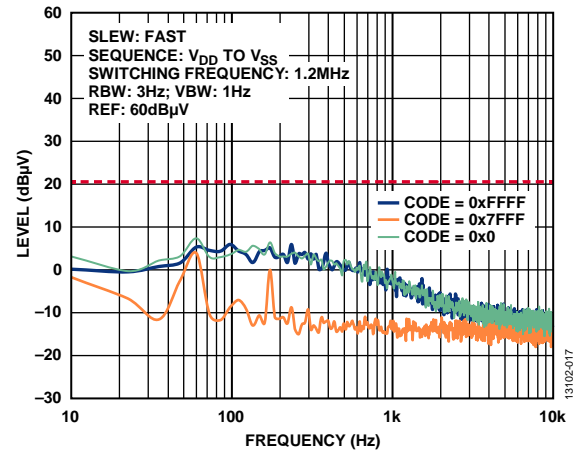


Figure 17. ADP5070, LC Filters, LDOs, and AD5761R Supply Configuration Output Spectral Response, Internal Reference (10 Hz to 10 kHz)

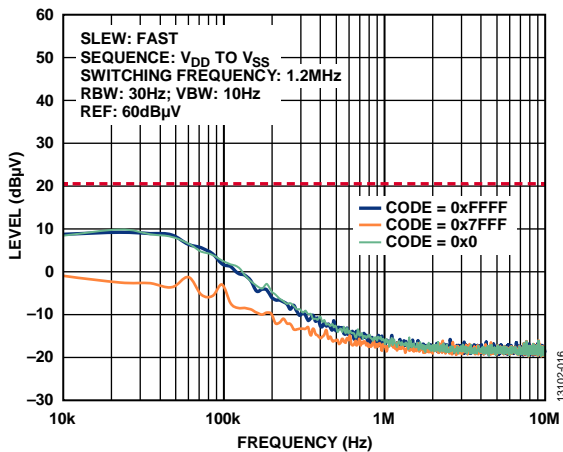


Figure 16. ADP5070, LDOs, and AD5761R Supply Configuration Output Spectral Response, External Reference (10 kHz to 10 MHz)

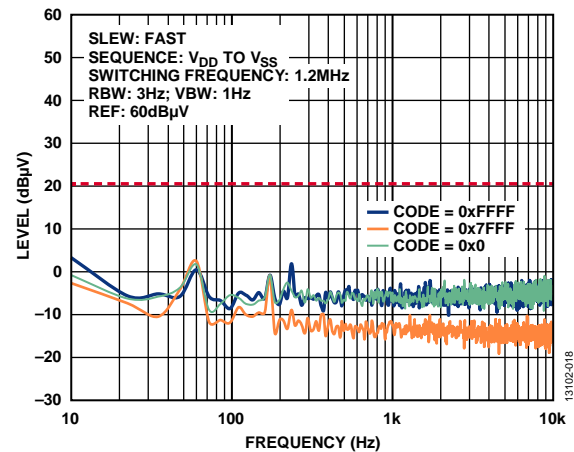


Figure 18. ADP5070, LC Filters, LDOs, and AD5761R Supply Configuration Output Spectral Response, External Reference (10 Hz to 10 kHz)

**DC-to-DC Switching Regulator, LC Output Filters, and CMOS LDO Linear Regulators Supply Configuration**

Adding two LDOs to the dc-to-dc switching regulator and LC output filters supply configuration further filters the ripple at the analog supplies of the AD5761R. The ADP7142 is used on the analog positive supply ( $V_{DD}$ ), while the ADP7182 is placed at the analog negative supply ( $V_{SS}$ ).

As explained in the DC-to-DC Switching Regulator and CMOS LDO Linear Regulators Supply Configuration section, adding LDOs to the ADP5070 dc-to-dc switch output when working at high frequencies is enough to obtain a good DAC output spectral response performance with no added spikes at any undesired frequency. The LC filters can still contribute to output noise rejection, but the LDO is the most significant factor in reducing the output noise. However, the LC filter is still a recommended option for sufficient high frequency ripple filtering.

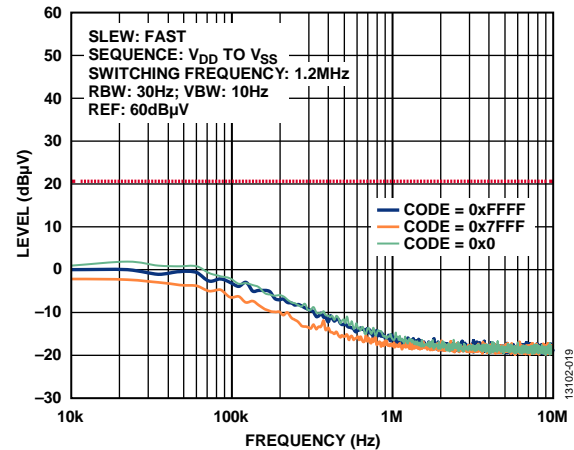


Figure 19. ADP5070, LC Filters, LDOs, and AD5761R Supply Configuration Output Spectral Response, Internal Reference (10 kHz to 10 MHz)

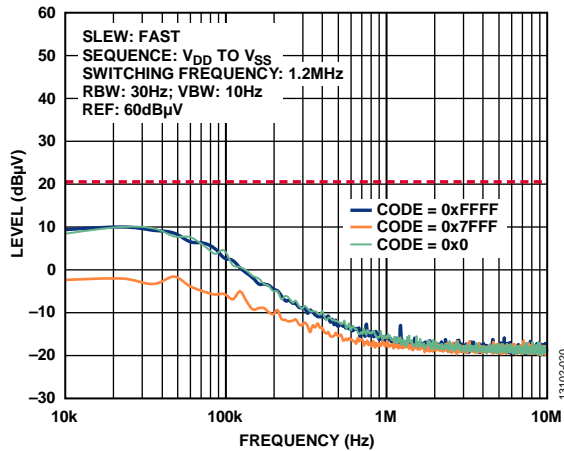


Figure 20. ADP5070, LC Filters, LDOs, and AD5761R Supply Configuration Output Spectral Response, External Reference (10 kHz to 10 MHz)

### AD5761R OUTPUT VOLTAGE NOISE

To provide a high precision response, it is recommended to maintain the peak-to-peak noise obtained at the output of the DAC below 1 LSB, which is 305.17  $\mu\text{V}$  for 16-bit resolution and a 20 V peak-to-peak voltage range. The AD5761R offers a typical output noise of 15  $\mu\text{V}$  p-p for the 0.1 Hz to 10 Hz frequency bandwidth and 35  $\mu\text{V}$  rms (which is equivalent to approximately 100  $\mu\text{V}$  p-p) for the 100 kHz frequency bandwidth. The noise at the output of the AD5761R for a  $\pm 10$  V range is measured over a period of 100 seconds, across the 0.1 Hz to 10 Hz frequency range and a 100 kHz bandwidth.

The test results for the three different configurations show the DAC performing within the specifications of the AD5761R data sheet. Figure 21 to Figure 34 show the noise at the output of the DAC for each configuration and frequency bandwidth, and Table 5 to Table 11 summarize the maximum peak-to-peak noise on the output of the DAC for the available power configurations.

The data in Table 2 to Table 12 and Figure 7 to Figure 37 show a common trend for all power supply configurations detailed in this application note. At the lower frequency bandwidth, the ADR4525 external reference produces a lower DAC output noise compared to using the AD5761R internal reference. In contrast, the DAC output noise is lower when the internal reference is used at a higher frequency bandwidth. This behavior correlates with the DAC output spectral response results previously presented.

Adding LDOs to the supply configuration affects performance slightly at a low frequency bandwidth for the DAC output noise presented in Figure 31 and Figure 32.

In contrast, at a high frequency bandwidth, adding an LDO to the supply configuration helps maintain a low noise overall performance. Figure 29 and Figure 30 show the AD5761R output noise when the DAC is powered by the ADP5070 and LDOs for a high frequency bandwidth of up to 100 kHz.

Table 5. External Supply and AD5761R Maximum Peak-to-Peak Output Noise ( $\mu\text{V}$  p-p), 0.1 Hz to 10 Hz Frequency Bandwidth

Code	Maximum Peak-to-Peak Output Noise	
	AD5761R Internal Reference	ADR4525
Zero-Scale	41 $\mu\text{V}$ p-p, 0.13 LSB p-p	12 $\mu\text{V}$ p-p, 0.04 LSB p-p
Half-Scale	6.2 $\mu\text{V}$ p-p, 0.02 LSB p-p	4.8 $\mu\text{V}$ p-p, 0.016 LSB p-p
Full-Scale	40 $\mu\text{V}$ p-p, 0.13 LSB p-p	14 $\mu\text{V}$ p-p, 0.04 LSB p-p

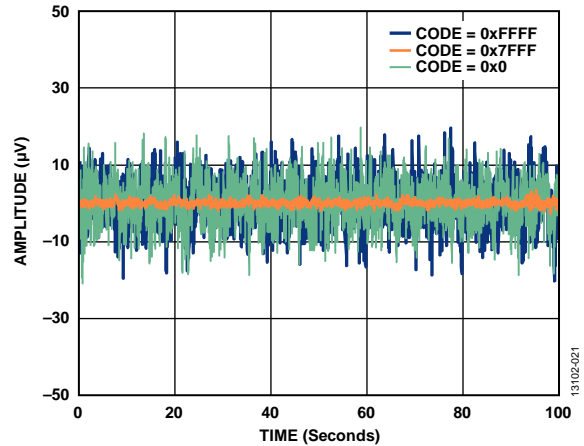


Figure 21. External Supply and AD5761R Peak-to-Peak Noise (Voltage Output Noise), 0.1 Hz to 10 Hz Bandwidth, Internal Reference

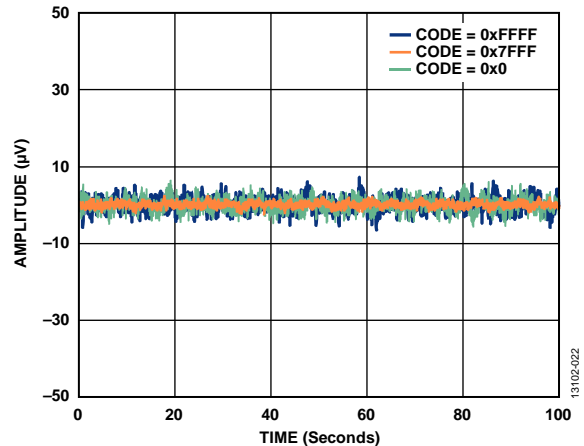


Figure 22. External Supply and AD5761R Peak-to-Peak Noise (Voltage Output Noise), 0.1 Hz to 10 Hz Bandwidth, External Reference

Table 6. External Supply and AD5761R Maximum Peak-to-Peak Output Noise ( $\mu\text{V p-p}$ ), 100 kHz Frequency Bandwidth

Code	Maximum Peak-to-Peak Output Noise	
	AD5761R Internal Reference	ADR4525
Zero Scale	33.6 $\mu\text{V p-p}$ , 0.11 LSB p-p	63.2 $\mu\text{V p-p}$ , 0.21 LSB p-p
Half-Scale	21 $\mu\text{V p-p}$ , 0.07 LSB p-p	22 $\mu\text{V p-p}$ , 0.07 LSB p-p
Full-Scale	32 $\mu\text{V p-p}$ , 0.10 LSB p-p	58.4 $\mu\text{V p-p}$ , 0.19 LSB p-p

Table 7. ADP5070, LC Filters, and AD5761R Maximum Peak-to-Peak Output Noise ( $\mu\text{V p-p}$ ), 0.1 Hz to 10 Hz Frequency Bandwidth

Code	Maximum Peak-to-Peak Output Noise	
	AD5761R Internal Reference	ADR4525
Zero-Scale	41 $\mu\text{V p-p}$ , 0.13 LSB p-p	13 $\mu\text{V p-p}$ , 0.04 LSB p-p
Half-Scale	6.6 $\mu\text{V p-p}$ , 0.02 LSB p-p	4.4 $\mu\text{V p-p}$ , 0.014 LSB p-p
Full-Scale	38 $\mu\text{V p-p}$ , 0.12 LSB p-p	13 $\mu\text{V p-p}$ , 0.04 LSB p-p

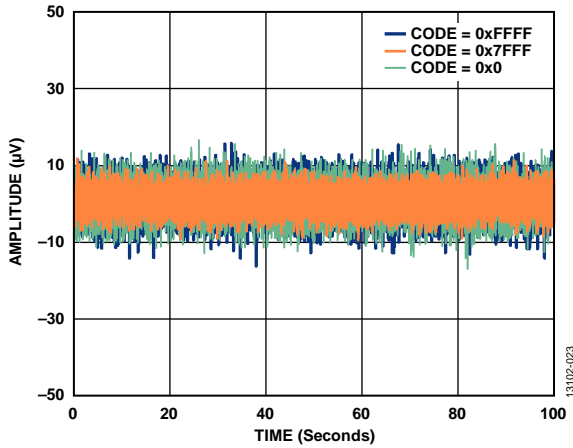


Figure 23. External Supply and AD5761R Peak-to-Peak Noise (Voltage Output Noise), 100 kHz Bandwidth, Internal Reference

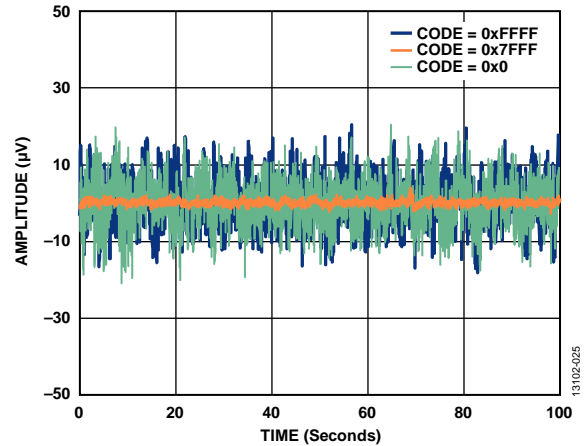


Figure 25. ADP5070, LC Filters, and AD5761R Peak-to-Peak Noise (Voltage Output Noise), 0.1 Hz to 10 Hz Bandwidth, Internal Reference

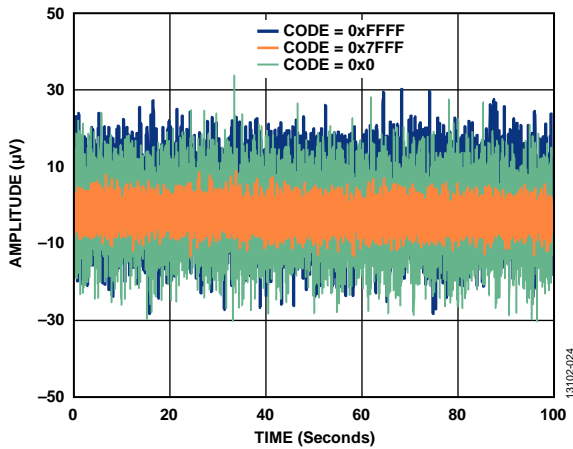


Figure 24. External Supply and AD5761R Peak-to-Peak Noise (Voltage Output Noise), 100 kHz Bandwidth, External Reference

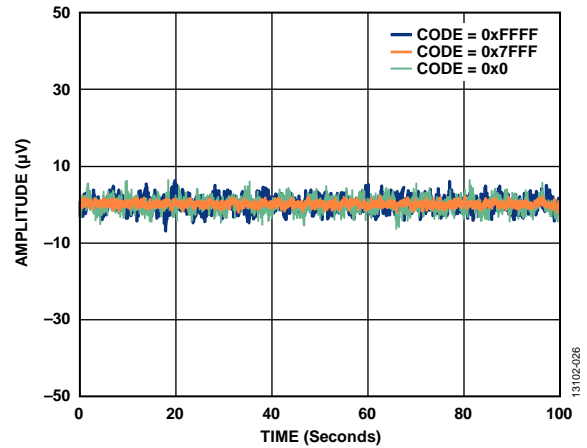


Figure 26. ADP5070, LC Filters, and AD5761R Peak-to-Peak Noise (Voltage Output Noise), 0.1 Hz to 10 Hz Bandwidth, External Reference

Table 8. ADP5070, LC Filters, and AD5761R Maximum Peak-to-Peak Output Noise ( $\mu\text{V p-p}$ ), 100 kHz Frequency Bandwidth

Code	Maximum Peak-to-Peak Output Noise	
	AD5761R Internal Reference	ADR4525
Zero-Scale	44.4 $\mu\text{V p-p}$ , 0.15 LSB p-p	68.2 $\mu\text{V p-p}$ , 0.22 LSB p-p
Half-Scale	30.8 $\mu\text{V p-p}$ , 0.10 LSB p-p	30.4 $\mu\text{V p-p}$ , 0.10 LSB p-p
Full-Scale	75.2 $\mu\text{V p-p}$ , 0.25 LSB p-p	88.8 $\mu\text{V p-p}$ , 0.29 LSB p-p

Table 9. ADP5070, LDOs, and AD5761R Maximum Peak-to-Peak Output Noise ( $\mu\text{V p-p}$ ), 100 kHz Frequency Bandwidth

Code	Maximum Peak-to-Peak Output Noise	
	AD5761R Internal Reference	ADR4525
Zero-Scale	35.2 $\mu\text{V p-p}$ , 0.12 LSB p-p	60.4 $\mu\text{V p-p}$ , 0.20 LSB p-p
Half-Scale	22.8 $\mu\text{V p-p}$ , 0.07 LSB p-p	22.4 $\mu\text{V p-p}$ , 0.07 LSB p-p
Full-Scale	31.2 $\mu\text{V p-p}$ , 0.10 LSB p-p	67.6 $\mu\text{V p-p}$ , 0.22 LSB p-p

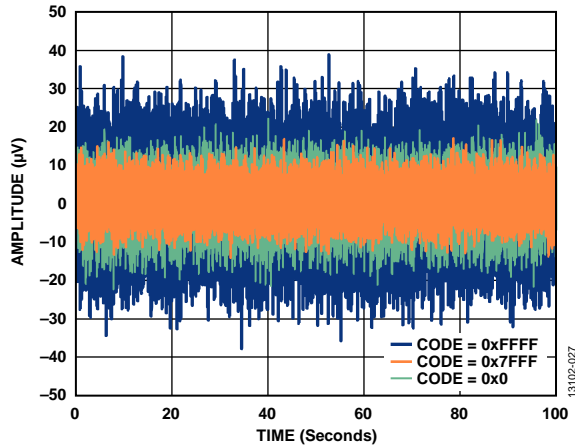


Figure 27. ADP5070, LC Filters, and AD5761R Peak-to-Peak Noise (Voltage Output Noise), 100 kHz Bandwidth, Internal Reference

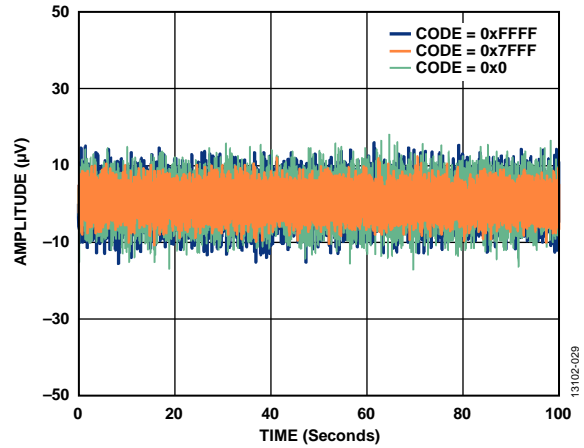


Figure 29. ADP5070, LDOs, and AD5761R Peak-to-Peak Noise (Voltage Output Noise), 100 kHz Bandwidth, Internal Reference

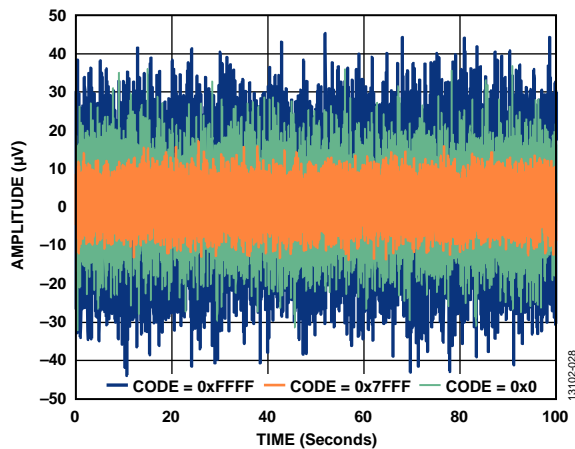


Figure 28. ADP5070, LC Filters, AD5761R Peak-to-Peak Noise (Voltage Output Noise), 100 kHz Bandwidth, External Reference

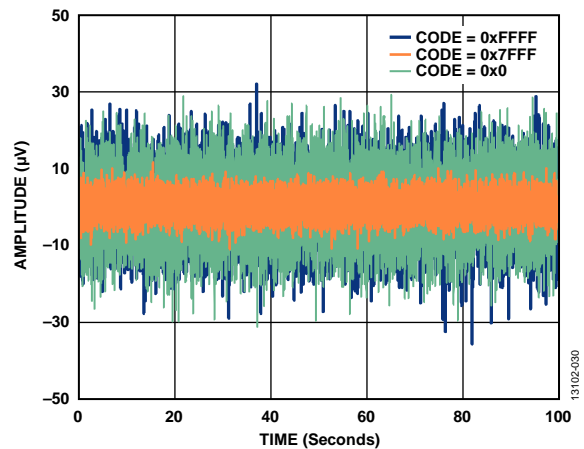


Figure 30. ADP5070, LDOs, and AD5761R Peak-to-Peak Noise (Voltage Output Noise), 100 kHz Bandwidth, External Reference

Table 10. ADP5070, LC Filters, LDOs, and AD5761R Maximum Peak-to-Peak Output Noise ( $\mu\text{V p-p}$ ), 0.1 Hz to 10 Hz Frequency Bandwidth

Code	Maximum Peak-to-Peak Output Noise	
	AD5761R Internal Reference	ADR4525
Zero-Scale	40.6 $\mu\text{V p-p}$ , 0.13 LSB p-p	12.8 $\mu\text{V p-p}$ , 0.04 LSB p-p
Half-Scale	5.4 $\mu\text{V p-p}$ , 0.018 LSB p-p	4.4 $\mu\text{V p-p}$ , 0.014 LSB p-p
Full-Scale	45.2 $\mu\text{V p-p}$ , 0.15 LSB p-p	13.2 $\mu\text{V p-p}$ , 0.04 LSB p-p

Table 11. ADP5070, LC Filters, LDOs, and AD5761R Maximum Peak-to-Peak Output Noise ( $\mu\text{V p-p}$ ), 100 kHz Frequency Bandwidth

Code	Maximum Peak-to-Peak Output Noise	
	AD5761R Internal Reference	ADR4525
Zero-Scale	36.8 $\mu\text{V p-p}$ , 0.12 LSB p-p	60.4 $\mu\text{V p-p}$ , 0.2 LSB p-p
Half-Scale	23.8 $\mu\text{V p-p}$ , 0.08 LSB p-p	22.6 $\mu\text{V p-p}$ , 0.07 LSB p-p
Full-Scale	33.6 $\mu\text{V p-p}$ , 0.11 LSB p-p	60 $\mu\text{V p-p}$ , 0.2 LSB p-p

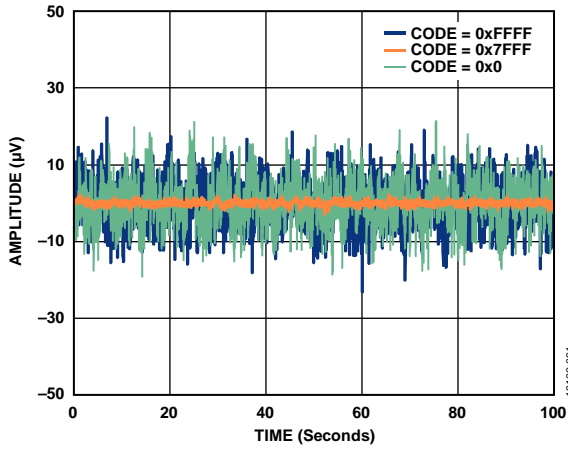


Figure 31. ADP5070, LC Filters, LDOs, and AD5761R Peak-to-Peak Noise (Voltage Output Noise), 0.1 Hz to 10 Hz Bandwidth, Internal Reference

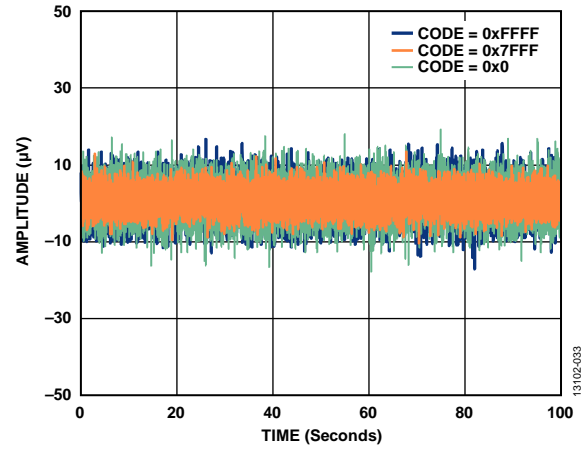


Figure 33. ADP5070, LC Filters, LDOs, and AD5761R Peak-to-Peak Noise (Voltage Output Noise), 100 kHz Bandwidth, Internal Reference

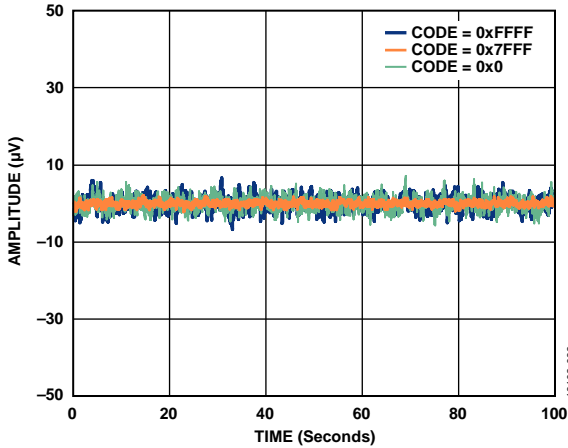


Figure 32. ADP5070, LC Filters, LDOs, and AD5761R Peak-to-Peak Noise (Voltage Output Noise), 0.1 Hz to 10 Hz Bandwidth, External Reference

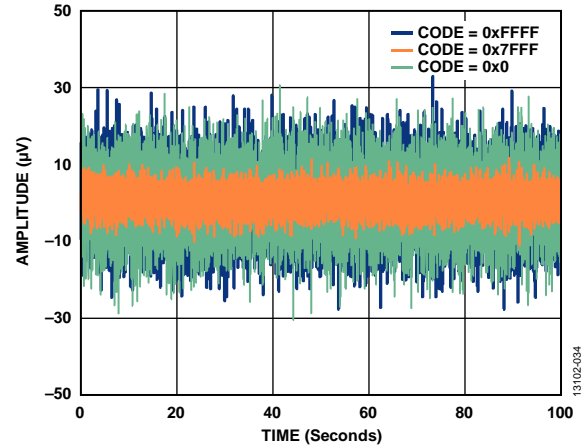


Figure 34. ADP5070, LC Filters, LDOs, and AD5761R Peak-to-Peak Noise (Voltage Output Noise), 100 kHz Bandwidth, External Reference

**AC PERFORMANCE**

This section presents the signal-to-noise ratio (SNR), total harmonic distortion (THD), signal-to-noise-and-distortion (SINAD), and spurious-free dynamic range (SFDR) parameters for the supply configurations using the [ADR4525](#) as the voltage reference. Table 12 summarizes the ac performance obtained for the three supply configurations shown in Figure 35 to Figure 37, for which a continuous 1 kHz sine wave was generated.

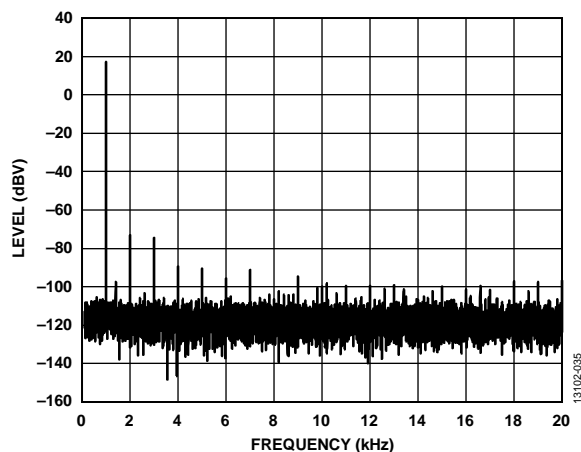


Figure 35. External Supply and [AD5761R](#) Digitally Generated Sine Wave, 1 kHz Tone at 17 dBV (7.07 V RMS)

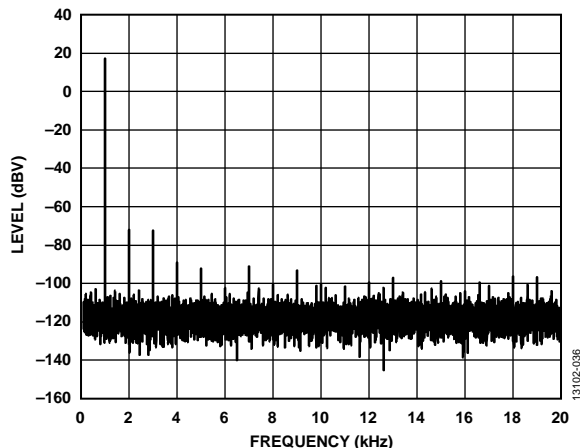


Figure 36. [ADP5070](#), LC Filters, and [AD5761R](#) Digitally Generated Sine Wave, 1 kHz Tone at 17 dBV (7.07 V RMS)

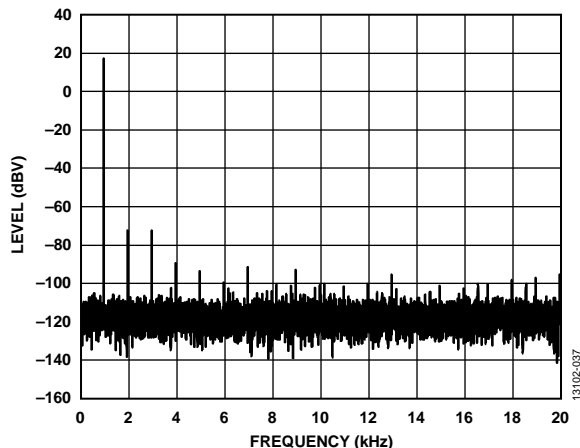


Figure 37. [ADP5070](#), LC Filters, LDOs, and [AD5761R](#) Digitally Generated Sine Wave, 1 kHz Tone at 17 dBV (7.07 V RMS)

**Table 12. AC Performance**

Parameter	External Supply and <a href="#">AD5761R</a> (dB)	<a href="#">ADP5070</a> , LC Filters, and <a href="#">AD5761R</a> (dB)	<a href="#">ADP5070</a> , LC Filters, LDOs, and <a href="#">AD5761R</a> (dB)
SNR	95.05	95.19	95.24
THD	-86.38	-86.30	-86.52
SINAD	85.82	85.77	85.98
SFDR	89.42	89.35	89.45

## CONCLUSION

The [AD5761R](#) is a 16-bit bipolar DAC with an integrated output amplifier, reference buffer, and reference; the high integration within the chip provides a complete solution. This application note introduces a flexible power solution for the [AD5761R](#) from a single supply rail using the [ADP5070](#) dc-to-dc switching regulator.

The configurations and results presented show the [AD5761R](#) performing within specification. To obtain a DAC output low noise response in a 0.1 Hz to 10 Hz frequency bandwidth, the recommended power solution includes the [ADP5070](#), LC filters,

and the [AD5761R](#). However, if a DAC output low noise response is required at a higher frequency bandwidth, the optimal power solution includes the [ADP5070](#), LC filters, LDO regulators, and the [AD5761R](#). The performance is also comparable when the LC filters are removed from the power configuration, sufficiently reducing the switching spurs from the [ADP5070](#) down to the target LSB threshold.

There is little variation in the ac performance across the different power configurations, which is comparable to the baseline measurement result using an external supply.