DIGITAL-TO-ANALOG CONVERTER ICS

Contents

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DAC with Dynamic Power Control Optimizes Thermal Management in Multichannel Industrial Control Applications

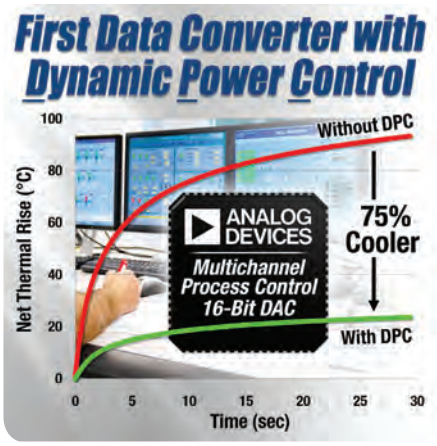
As the density of factory process control terminals increases, the system power dissipation reaches levels where thermal issues begin to undermine equipment performance, reliability, and safety.

Solution

The AD5755 is a complete, multichannel control IC that incorporates on-chip dynamic power control with four precision 16-bit programmable voltage, or 4 mA to 20 mA current, output DACs. The dynamic power control works by continually sensing the load impedance and delivering the required power to the load while minimizing power loss in the rest of the system. This reduces self-heating and temperature elevation in dense, multichannel systems by 75% and lowers overall power consumption by 80% compared to other control technologies. The AD5755 offers fully specified performance with maximum total unadjusted error of 0.05% and a relative accuracy of ±0.006% max—meaning system calibration is no longer required. Supporting standard industrial voltage and current output ranges, the AD5755 can be used with standard HART protocol modems. Watch a brief video at *www.analog.com/AD5755* for more information on this device and its features.

AD5755 Features

- Quad DAC with 16-bit resolution and monotonicity
- Dynamic power control for thermal management
- Integrated on-chip internal reference
- Diagnostics and real-time fault analysis
- 9 mm × 9 mm, 64-lead LFCSP
- Pricing: $13.65



Integrated Industrial Multichannel DACs

Part Number	Number of Channels	Resolution (Bits)	Output Type	HART Compliant
AD5755	4	16	V or I	
AD5755-1	4	16	V or I	•
AD5735	4	12	V or I	
AD5757	4	16	I	•
AD5737	4	12	I	•

Loop-Powered DAC Conserves Power in Remote Industrial Applications

Smart transmitters are powered from the 4 mA to 20 mA loop and, hence, operate within a limited power budget. As a result, the development of systems that accurately and efficiently monitor and transmit remote system measurements is an imposing challenge.

Solution

To address this, system designers require a 4 mA to 20 mA loop-powered communication solution that is power efficient, highly accurate, and, ultimately, compact. The AD5421 has been specifically engineered to address this challenge by integrating on-board programmable power management circuitry with precision converter technology to bolster available system power. A complete transmitter solution, the AD5421 combines a precision, 16-bit, loop-powered digital to 4 mA to 20 mA transmitter with on-board voltage regulation circuitry. The on-chip regulator is designed to power the AD5421 and the peripheral components within the smart transmitter and generates a user-programmable 1.8 V to 12 V output voltage. Consuming only 250 μA of quiescent current, the AD5421 conserves the system power budget, enabling the selection of more accurate, higher power sensor electronics. Housed in 28-lead TSSOP and 32-lead LFCSP (5 mm × 5 mm), the AD5421 offers a complete single chip solution that reduces the overall PCB component count, providing a 55% footprint savings over alternative solutions. The high linearity and low drift performance offered by the AD5421 enable the development of high performance, feature-rich designs. The AD5421 can be used with standard HART protocol circuitry and offers NAMUR-compliant output ranges. Watch the AD5421 DAC video for more information on its features at *www.analog.com/AD54210verview*.

AD5421 Features

- 16-bit resolution and monotonicity
- Output ranges: 4 mA to 20 mA, 3.8 mA to 21 mA, 3.2 mA to 24 mA
- On-chip fault alerts via FAULT pin or ALARM current
- On-chip 2.5 V reference (4 ppm/°C max)
- Pricing: $5.90

Applications

- Smart transmitters
- 4 mA to 20 mA loop-powered transmitters

Recommended Complementary Components

- Low power precision analog microcontroller: ADuC7060
- Low noise, low power, Σ-Δ ADC: AD7794

Breakthrough 1 PPM Digital-to-Analog Converter

Across a range of applications from MRI systems to precision instrumentation there has long been a need for more accurate, simpler, and cost-effective DACs with guaranteed specifications that don't require calibration or constant monitoring.

Solution

The AD5791 is the industry's first single chip DAC to feature true 1 ppm resolution and accuracy, providing 4× greater accuracy and 4× more resolution than competing converters. The 20-bit AD5791 offers a relative accuracy specification of ±1 ppm INL maximum. Operation is guaranteed monotonic with a ±1 ppm DNL maximum specification. The product delivers 0.025 ppm low frequency noise, 7.5 nV/√Hz noise spectral density, 1 μs settling time, and 0.05 ppm/°C output drift. In addition, the device features sub-1 ppm lifetime drift. The AD5791 DAC incorporates a power-on reset circuit that ensures the DAC powers up at 0 V output and in a known output impedance state. The low noise, low drift, and fast refresh rate of the AD5791 maximizes operational up-time by eliminating costly calibration cycles and enabling faster system response times, thereby reducing cost of test. For more on the specific features of the AD5791, watch the video at *www.analog.com/AD57910verview*. For details on the design of a 1 ppm system, read our technical article at *www.analog.com/AD5791Article*.

AD5791 Features

- 20-bit resolution
- 1 ppm linearity without adjustments
- 20-lead TSSOP package
- Pricing:
  - AD5791 (A grade)—$46.10
  - AD5791 (B grade)—$64.58

Recommended Complementary Components

- 36 V precision, 2.8 nV/√Hz, rail-to-rail output op amps: AD8675 and AD8676

Reference Circuits

Circuits from the Lab™ Reference Circuits

20-Bit, Linear, Low Noise, Precision, Bipolar ±10 V DC Voltage Source Using the AD5791 DAC. Complete documentation available at *www.analog.com/CN0191*.

IF DAC Solutions in Base Station Transmit Architectures

In W-CDMA, CDMA2000, TD-SCDMA, GSM, and WiMAX base station transmit applications, high performance DACs are commonly used to synthesize the I/Q intermediate frequency (IF) in the transmit signal chain architecture. As service providers are continually requiring more performance and functional integration delivered in a shrinking amount of space, it is incumbent upon system designers to choose optimal components for the task. Having a broad portfolio from which to choose the optimal component is mandatory.

Solution

As the market leader in high speed data conversion, Analog Devices offers a deep and unique portfolio of TxDAC® IF transmit DAC solutions that allows the designer to optimize product selection and meet all critical system criteria, whether it be bandwidth, dynamic performance, power, package size, data interface, level of integration, etc. ADI fully understands transmit architectures and communications requirements and has engineered an IF DAC product portfolio to match the needs of any application. Premiere products include:

AD9148—Quad, 16-Bit, 1 GSPS, TxDAC+ Transmit DAC

- On-chip 32-bit NCO for complex modulation schemes with 2×, 4×, and 8× interpolation
- Noise spectral density of –158 dBm/Hz
- 3rd-order IMD = 85 dBc
- ACLR = 78 dBc
- 12 mm × 12 mm flip-chip package technology
- Pricing: $56.80

AD9146—16-Bit, 1.2 GSPS, TxDAC+ Transmit DAC

- Noise specification of –164 dBm/Hz
- 2× and 4× interpolators with fine NCO modulation control
- IMD of 81 dBc @ 100 MHz
- Single-carrier W-CDMA ACLR = 82 dBc @ 122.88 MHz IF
- 7 mm × 7 mm LFCSP
- Pricing: $29.95

AD9125—Dual, 16-Bit, 1 GSPS TxDAC+ Transmit DAC

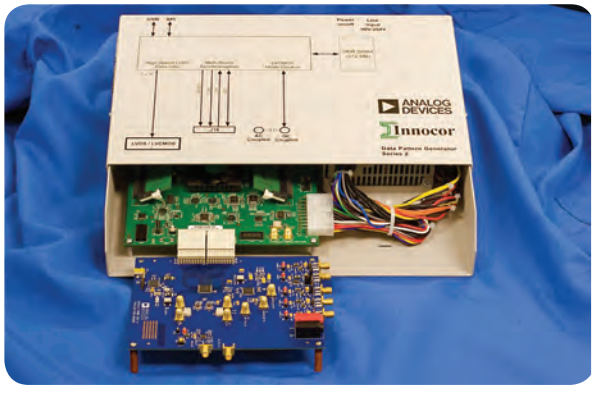
- Single-carrier W-CDMA ACLR = 80 dBc at 122.88 MHz IF
- Novel 2×/4×/8× interpolator/complex modulator allows carrier placement anywhere in the DAC bandwidth
- Gain and phase adjustment for sideband suppression
- Multichip synchronization interface
- 10 mm × 10 mm exposed paddle LFCSP
- Pricing: $30.00

AD9117 and AD9717—14-Bit, 125 MSPS, TxDAC+ Transmit DACs with 20 mA and 4 mA I_{OUT}

- NSD @ 10 MHz output, 125 MSPS, –157 dBc/Hz
- SPI interface for device configuration and status register readback
- PDISS of 220 mW while operating at maximum speed
- 6 mm × 6 mm LFCSP
- Pricing: $9.50

Easy High Speed DAC Evaluation Using DPG

ADI provides a unique set of hardware and software tools to evaluate a DAC's functionality and test its performance within a full complex-IF signal chain. Analog Devices evaluation boards integrate clock generation and a quadrature modulator with the DAC solutions to demonstrate real-world signal chain performance. The Data Pattern Generator hardware and software allow the user to generate and stimulate the DAC input data port with multiple CW tones, multicarrier W-CDMA or LTE, or other customer-generated waveforms. For more information, please visit *www.analog.com/dpg*.



Transmit system evaluation platform.

New Direct Digital Synthesis (DDS) IC Delivers Power and Size Savings for Industrial and Communications Applications

Large communication and instrumentation systems, such as wireless base stations and test and measurement equipment, have been taking advantage of fine frequency tuning, fast frequency hopping and settling times, and other performance benefits of DDS technology for over a decade. Now, designers of low power devices also seek to incorporate the benefits of DDS technology into their products without board space and power penalties.

Solution

The AD9838 is a complete, low power, small package DDS specifically engineered for wireless, handheld, and sensory equipment. The first DDS with sub-11 mW power consumption for a 16 MHz master clock, the AD9838 settles in nanoseconds with granularity well below 100 mHz. With an on-chip, low power DAC, it provides 28-bit fine frequency tuning and high SFDR that enables the user to more quickly and accurately generate a stable signal in the band of interest. Integration of various communication and modulation features enables the devices to support single-tone, 2FSK, 2PSK, QPSK, sweep capability, and amplitude modulation, simplifying the design of communications systems and reducing development risk and cost.

AD9838 Features

- Narrow-band SFDR > 66 dB
- Low 11 mW operating power
- Supports 16 MHz clock speed
- Sine, square, and triangular output
- 4 mm × 4 mm, 20-lead LFCSP
- Pricing: $2.10

Applications

- Industrial sensory excitation applications
- Impedance spectroscopy
- Battery-enabled diagnostic and communications equipment

Recommended Complementary Components

- Voltage feedback amplifiers: AD8038, AD8065
- Current output DACs: AD5543, AD5443

Multioutput Clock Distribution Function with Serial On-Chip PLLs Delivers <200 fs RMS Jitter to Enhance Data Converter SNR Performance

The clock signals provided to high speed, high performance DACs are often one of the primary limiting factors for the performance achieved by that DAC. In order to achieve their rated performance specifications, high speed data converters require a fast rising, low jitter sampling clock. In large complex systems where there are many digital chips requiring clock signals as a reference, it can be a significant challenge to maintain a good low noise/low jitter clock signal throughout the entirety of the clock tree.

The AD9523 is designed to support the clocking requirements for data conversion stages in long-term evolution (LTE) and multicarrier GSM base station designs, medical instrumentation, ATE, and other wireless transceiver systems. It relies on an external VCXO to provide the oscillator source for a jitter cleanup PLL to achieve the restrictive low phase noise requirements necessary for acceptable data converter SNR performance. When connected to a recovered system reference clock and a VCXO, the device generates 14 low noise outputs with a range of 1 MHz to 1 GHz and one dedicated buffered output from the input PLL (PLL1).

In addition, Analog Devices has developed a broad portfolio of discrete clock buffers that feature jitter on the order of 75 fs for LVPECL fanout buffers with skew on the order of 9 ps (picoseconds). These buffers can be situated near the data converter to revitalize the clock signal. When a very sharp edge for just one or two DACs is needed, the ADCLK905, ADCLK907, ADCLK914, ADCLK925, and ADCLK944 clock buffers provide very fast edges with little impact on the noise of the clock signal.

AD9523 Features

- Output frequency: <1 MHz to 1 GHz
- Absolute output jitter: <200 fs @ 122.88 MHz
  - Integration range: 12 kHz to 20 MHz
- 14 outputs: configurable LVPECL, LVDS, HSTL, and LVCMOS
- Distribution phase noise floor: –160 dBc/Hz
- Pricing: $8.34

Data Conversion Knowledge Resource

Designing analog and mixed-signal circuits is usually tougher than designing purely digital circuits, and high performance analog-to-digital or digital-to-analog conversion stages can be one of the toughest challenges of all. Data conversion involves many critical analog-oriented circuit considerations that directly impact the success of your design.

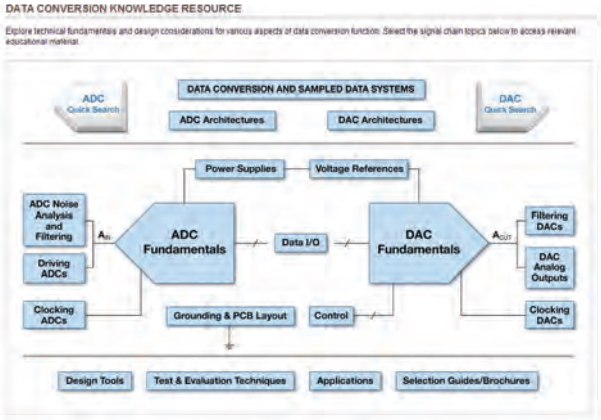
To help with this challenge, Analog Devices has launched its new Data Conversion Knowledge Resource, which is an easy-to-navigate library of in-depth technical material focusing on all aspects of a conversion stage design. It comprises the best of the design and applications engineering knowledge that ADI has accumulated over our 45-year span of pioneering work in data conversion. It is material that you need to know, and who better to learn from than the experts at the company that literally wrote the book on the subject?

For instance, among the 17 items in the ADC Noise Analysis and Filtering category are two articles authored by renowned ADI data converter technologist Walt Kester:

- "The Good, the Bad, and the Ugly Aspects of ADC Input Noise—Is No Noise Good Noise?"
- "Understand SINAD, ENOB, SNR, THD, THD + N, and SFDR so You Don't Get Lost in the Noise Floor"

The library's rich and varied content was compiled from the best of ADI's seminar notes, tutorials, *Analog Dialogue* articles, and technical webcasts.

We welcome you to visit *www.analog.com/TheKnowledgeResource* and learn.



The Data Conversion Knowledge Resource *site provides easy browsing in a library of technical content sorted to specific areas of the data conversion function.*

ENGINEERZONE BETA Answers. Right. Now.

Become part of a growing online design community where you can get answers to your toughest data conversion design questions in real time at *ez.analog.com.*

DAC Buffer: Low Power, Precision, Rail-to-Rail Input and Output Amplifier

Digital-to-analog converters are often designed with outputs that need a buffer in order to drive low impedance loads or to convert their current output into a voltage output. Often, the design engineers need this function over a wide variety of products, and it is time-consuming to select different op amps for the various supply voltages and output configurations required for each product.

Solution

The ADA4096-2 operational amplifier operates with voltage supplies compatible with nominal supply voltages from 3 V to 30 V (±1.5 V to ±15 V), and with its rail-to-rail input and output capability, it is a flexible op amp that is useful in a wide variety of applications. With its low input bias current, input offset voltage, and temperature drift specifications, it is well suited for 10-bit to 14-bit DACs where its voltage offset is less than an LSB. As an example, it will support the 14-bit AD5640 DAC with its LSB weight of 300 μV. The ADA4096-2 device's stability when driving low impedance and high capacitance loads also contributes to the usefulness of this product as a DAC driver.

ADA4096-2 Features

- Wide voltage supply: 3 V to 30 V nominal
- Rail-to-rail input and output
- Useable in single and dual supply voltage applications
- Low offset voltage and temperature drift: 35 μV and 1 μV/°C typical
- Low input bias current: 3 nA typical
- Low supply current: 60 μA/amp typical
- Wide unity gain bandwidth:
  - 800 kHz typical @ V_{SY} = 30 V
  - 50 kHz typical @ V_{SY} = 10 V
  - 475 kHz typical @ V_{SY} = 3 V
- Input overvoltage protection for 32 V above/below voltage supply
- Pricing: $1.87

Selection Guide

Integrated Industrial Single-Channel DACs

Part Number	No. of Channels	Resolution (Bits)	Output Type (V, I, V or I)	Current Range (mA)	Voltage Range (V)	Package	Price ($U.S.)
AD5421	1	16	I	4 to 20, 3.8 to 21, 3.2 to 24	N/A	28-lead TSSOP	5.90
AD5420	1	16	I	4 to 20, 0 to 20, 0 to 24	N/A	40-lead LFCSP, 24-TSSOP	4.95
AD5410	1	12	I	4 to 20, 0 to 20, 0 to 24	N/A	40-lead LFCSP, 24-lead TSSOP	3.75
AD5422	1	16	V or I	4 to 20, 0 to 20, 0 to 24	0 to 5, 0 to 10, ±5, ±10	40-lead LFCSP, 24 lead-TSSOP	5.60
AD5412	1	12	V or I	4 to 20, 0 to 20, 0 to 24	0 to 5, 0 to 10, ±5, ±10	40-lead LFCSP, 24-lead TSSOP	4.38

Integrated Industrial Multichannel DACs

Part Number	No. of Channels	Resolution (Bits)	Output Type (V, I, V or I)	Current Range (mA)	Voltage Range (V)	Package	Price ($U.S.)
AD5755	4	16	V or I	4 to 20, 0 to 20, 0 to 24	0 to 5, 0 to 10, ±5, ±10, ±6, ±12	64-lead LFCSP	13.65
AD5755-1*	4	16	V or I	4 to 20, 0 to 20, 0 to 24	0 to 5, 0 to 10, ±5, ±10, ±6, ±12	64-lead LFCSP	15.88
AD5735	4	12	V or I	4 to 20, 0 to 20, 0 to 24	0 to 5, 0 to 10, ±5, ±10, ±6, ±12	64-lead LFCSP	10.85
AD5757*	4	16	I	4 to 20, 0 to 20, 0 to 24	N/A	64-lead LFCSP	12.14
AD5737*	4	12	I	4 to 20, 0 to 20, 0 to 24	N/A	64-lead LFCSP	8.95

* HART compliant.

Precision DACs

Part Number	Resolution (Bits)	INL	Output Range	Noise Spectral Density (nV/√Hz)	Temperature Drift (ppm/°C)	Settling Time (µs)	Package	Price ($U.S.)
AD5791	20	1	V_{REFN} to V_{REFP} (V_{REFP} = 5 V to 14 V, (V_{REFN} = –14 V to 0 V)	7.5	0.04	1	20-lead TSSOP	37.86
AD5781	18	1	$\pm V_{REF}$, 0 to V_{REF}, ($V_{REFP/N}$ = 5 V to 14 V)	7.5	0.04	1	20-lead TSSOP	16.42
AD5541A	16	1	0 to V_{REF} (V_{REF} = 2 V to 5.5 V)	11.8	±0.1	1	10-lead LFCSP, 8-lead LFCSP, 10-lead MSOP	6.25
AD5542A	16	1	0 to V_{REF}, $\pm V_{REF}$ (V_{REF} = 2 V to 5.5 V)	11.8	±0.2	1	16-lead LFCSP, 10-lead LFCSP, 16-lead TSSOP	6.25
AD5512A	12	1	0 to V_{REF}, $\pm V_{REF}$ (V_{REF} = 2 V to 5.5 V)	11.8	±0.2	1	16-lead LFCSP, 10-lead LFCSP, 16-lead TSSOP	3.12

Transmit IF DACs

Part Number	Resolution (Bits)	Max Update Rate	DAC Channels	Interface	Max Output Signal Bandwidth (MHz)	Max Output Frequency (MHz)	Power Dissipation (W)	Price ($U.S.)
AD9122	16	1.23 GSPS	2	LVDS	500	614	1.1	34.50
AD9146	16	1.23 GSPS	2	LVDS	307.5	615	1.2	29.95
AD9125	16	1 GSPS	2	CMOS	250	500	1.1	30.00
AD9148	16	1 GSPS	4	LVDS	310	500	3	56.80
AD9783/AD9781/ AD9780	16/14/12	500 MSPS	2	LVDS	250	500	462.3 mW	22.77/20.24/ 16.19
AD9717/AD9716/ AD9715/AD9714	14/12/10/8	125 MSPS	2	CMOS	62.5	62.5	86 mW	9.50/8.75/ 6.90/5.95
AD9117/AD9116/ AD9115/AD9114	14/12/10/8	125 MSPS	2	CMOS	62.5	62.5	232 mW	9.50/8.75/ 6.90/5.95

RF DACs

Part Number	Resolution (Bits)	Max Update Rate (GSPS)	Multichip Synchronization	Interface	Max Output Signal Bandwidth (MHz)	Max Output Frequency (MHz)	Power Dissipation (W)	Price ($U.S.)
AD9739A	14	2.5	No	LVDS	1250	3000	960 mW	43.69
AD9739	14	2.5	Yes	LVDS	1250	3000	1.16	43.69
AD9789	14	2.4	No	CMOS	150	3000	1.7	58.54

Selection Guide (continued)

*dense*DAC High Channel Count DACs

Part Number	Resolution (Bits)	Interface	Reference (V)	Channels	Package	Price ($U.S.)
AD5668	16	SPI	1.25	8	16-lead WLCSP	11.39
AD5668	16	SPI	1.25/2.5	8	16-lead LFCSP/16-lead TSSOP	11.39
AD5648	14	SPI	1.25/2.5	8	16-lead TSSOP	10.63
AD5628	12	SPI	1.25/2.5	8	16-lead LFCSP/16-lead TSSOP	7.70
AD5628	12	SPI	1.25	8	16-lead WLCSP	7.70
AD5669R	16	I²C	1.25/2.5	8	16-lead LFCSP/16-lead TSSOP	12.30
AD5629R	12	I²C	1.25/2.5	8	16-lead LFCSP/16-leadTSSOP	7.95

Output Buffer Amplifiers

Part Number	Nominal V_{SY} Range (V)	V_{OS} Max @ 25°C	TCV_{OS} Typ	Unity Gain Bandwidth (Typ)	I_{SY} Max @ 25°C (μA)	I_B Max @ 25°C	RRIO	Price ($U.S.)
ADA4096-2	3 to 30	300 μV	1.0 μV/°C	800 kHz	75	10 nA	Yes	1.87
ADA4091-2	3 to 30	250 μV	3.0 μV/°C	1.27 MHz	250	60 nA	Yes	2.22
ADA4084-2	3 to 30	100 μV	0.2 μV/°C	8.3 MHz	750	450 nA	Yes	2.85
AD8622	3 to 30	125 μV	0.5 μV/°C	560 kHz	250	200 pA	RRO	2.30
AD8606	3 to 5	65 μV	1.0 μV/°C	10 MHz	1.2 ma	1 pA	Yes	1.19
ADA4665-2	5 to 16	4 mV	3.0 μV/°C	1.2 MHz	400	1 pA	Yes	0.70

Clock Generator

Part Number	Description	No. of Inputs	No. of Outputs	Max f_{OUT} (GHz)	Output Logic	Random Jitter (fs)	Price ($U.S.)
AD9523-1	Low jitter, dual loop clock generator	2	14	1	CMOS, HSTL, LVDS, LVPECL	187	8.34
AD9523	Low jitter, dual loop clock generator	2	14	1	CMOS, HSTL, LVDS, LVPECL	225	9.27
AD9516-0	Multioutput clock generator	2	14	2.25	CMOS, LVDS, LVPECL	400	11.39
AD9520-1	Multioutput clock generator	1	12	2.65	CMOS, LVPECL	225	12.65
AD9524	Low jitter, dual loop clock generator	2	14	1	CMOS, HSTL, LVDS, LVPECL	225	6.57

Clock Buffers and Distribution ICs

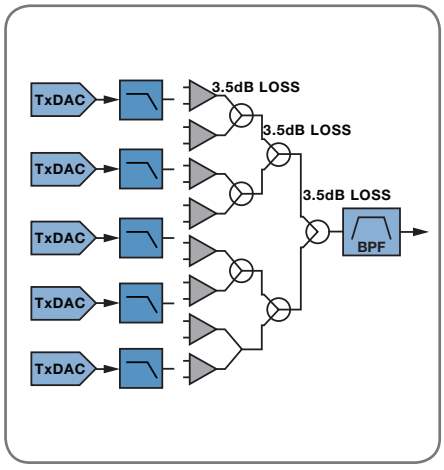
Part Number	Input/Output	Input/Output Logistics		Toggle Rate	RMS Jitter (ps)	Typ Output-to-Output Skew (ps)	Price ($U.S.)
		Input	Output				
AD9512/AD9513/ AD9514/AD9515	1 to 2/3/5	Differential	LVDS/CMOS	800 MHz LVDS/ 250 MHz CMOS	0.3	—	9.06/5.35/ 6.02/4.81
ADCLK905/ADCLK907	1 to 1 Dual 1 to 1	Differential	LVPECL	7.5 GHz	0.06	—	5.27/8.04
ADCLK925	1 to 2	Differential	LVPECL	7.5 GHz	0.06	9	6.29
ADCLK944	1 to 4	Differential	LVPECL	7 GHz	0.05	9	5.95
ADCLK946/ADCLK948/ ADCLK950/ADCLK954	1 or 2 to 6/8/10/12	LVPECL/CML/ CMOS/LVDS	LVPECL	4.8 GHz	0.075	9	6.25/6.50/ 6.58/6.95
ADCLK914	1 to 1	LVPECL/CML/CMOS/ LVTTL/LVDS	HVDS	7.5 GHz	0.11	—	8.18
ADCLK846/ADCLK854	1 or 2 to 6/8	LVPECL/LVDS/ HSTL/CML/CMOS	LVDS/CMOS	1.2 GHz LVDS/ 250 MHz CMOS	0.1	65	4.75/5.35
ADN4670	1 or 2 to 10	Differential	LVDS	1.1 GHz	0.1	30	5.50

When Synthesizing Large Bandwidths or Narrow-Band Waveforms Below 2.7 GHz, RF DACs Provide Unique Technology That Allows Direct Bits-to-RF Conversion in a Single Package

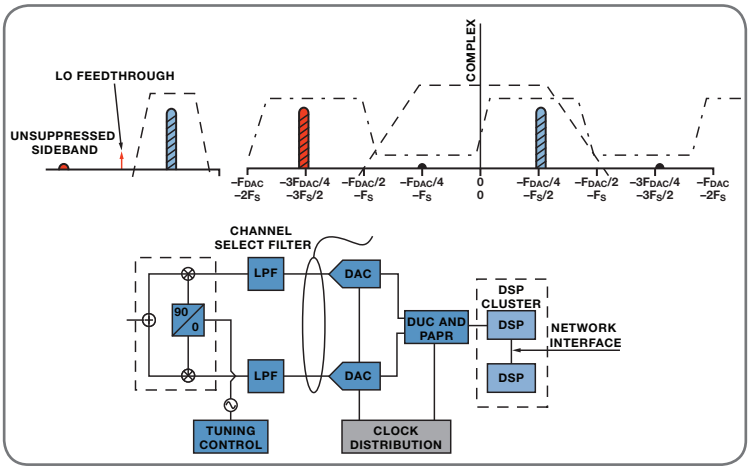
In wired and wireless communication applications, multicarrier transmitters are becoming the norm. To modulate and combine multiple carriers to form the transmit output, system engineers are challenged by complex analog signal processing and power-inefficient combiners, as shown in the traditional multiple carrier transmit signal chain below.

Solution

A traditional solution for this challenge in wireless communication systems is to utilize discrete dual DACs and a quadrature modulation function to generate signals above 300 MHz. Although flexible, this solution requires specific clock and power circuitry. As can be seen in the complex IF transmit signal chain below, stringent RF filtering is required to correct analog imperfections such as unsuppressed sideband and LO feedthrough. When combining these architecture limitations with infrastructure equipment's trending requirements for smaller and lower power solutions, the RF system engineer is challenged to provide a solution meeting market demand.



Traditional multiple carrier transmit signal chain.



Complex IF transmit signal chain.

AD9739—14-Bit, 2.5 GSPS RF DAC with Multichip Synchronization

- DOCSIS 3.0 performance
  - 8 QAM carriers @ 400 MHz IF: –71 dBc
  - 16 QAM carriers @ 400 MHz IF: –68 dBc
  - 32 QAM carriers @ 400 MHz IF: –65 dBc
  - 72 QAM carriers @ 600 MHz IF: –61 dBc
- RF synthesis support: FS mix, RZ modes
- Dual-port LVDS data interface with on-chip 100 Ω terminations
- 12 mm × 12 mm, 160-ball CSP_BGA
- Pricing: $43.69

AD9739A—14-Bit, 2.5 GSPS RF DAC

- Direct RF synthesis at 2.5 GSPS
- Update rate: dc to 1.25 GHz in baseband mode, 1.25 GHz to 3.0 GHz in mix mode
- Industry-leading single/multicarrier IF or RF synthesis
- Dual-port LVDS data interface up to 1.25 GSPS operation
- Source-synchronous DDR clocking
- Pin-compatible with the AD9739
- Programmable output current: 8.7 mA to 31.7 mA
- Low power: 1.1 W at 2.5 GSPS
- 12 mm × 12 mm, 160-ball CSP_BGA
- Pricing: $43.69

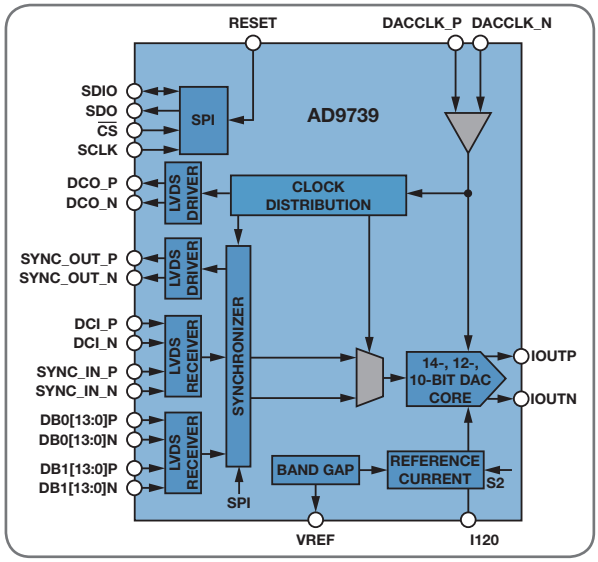
AD9789—14-Bit, 2.4 GSPS RF DAC with 4-Channel Signal Processing

- On-chip and bypassable 4 QAM encoders with SRRC filters
- 16× to 512× interpolation, rate converters, and modulators
- DOCSIS 3.0 performance: 4 QAM carriers
- ACLR over full band (47 MHz to 1 GHz)
  - –75 dBc @ f_{OUT} = 200 MHz
  - –72 dBc @ f_{OUT} = 800 MHz (noise)
  - –67 dBc @ f_{OUT} = 800 MHz (harmonics)
- Flexible data interface: 4, 8, 16, or 32 bits wide with parity
- 12 mm × 12 mm, 164-ball CSP_BGA
- Pricing: $58.54

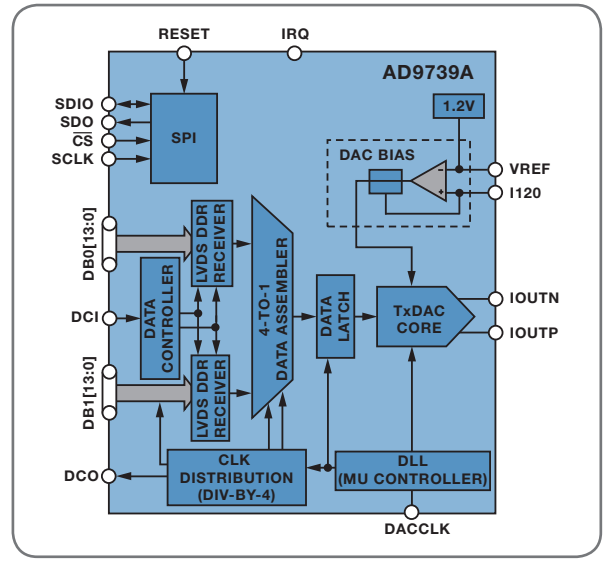
RF DAC Solution

As the market leader in high speed data conversion, Analog Devices provides unique technology to solve the bandwidth and transmit architecture challenges for RF frequencies below 2.7 GHz. RF DAC technology from Analog Devices can not only synthesize up to 1 GHz of modulated signal bandwidth, but with its proprietary mixed-mode sampling capability, it enables the use of the second Nyquist zone to provide bits-to-RF conversion of frequencies up to 2.7 GHz, in a single package. Analog Devices provides three such RF DACs with bit-to-RF capability.

The AD9739 and AD9739A are high performance, high frequency 14-bit DACs that provide sampling rates of up to 2.5 GSPS. These devices permit multicarrier generation at up to the Nyquist frequency in baseband mode, and utilizing their unique mix-mode functionality, they can generate carriers of up to 2.7 GHz in the second and third Nyquist zones. They include a dual-port LVDS interface to readily interface with existing FGPA/ASIC technology to facilitate the maximum baseband signal synthesis bandwidth of 1.25 GHz. Unlike the AD9739A, the AD9739 features a multichip synchronization feature that allows the synchronization of multiple transmit channels (see block diagrams below). With 1.1 W power consumption at the full sampling rate, the AD9739 and AD9739A RF DAC IC devices provide the lowest power and smallest package-size solution for synthesizing up to 1 GHz of bandwidth and output frequencies below 2.5 GHz in multicarrier transmit systems. They eliminate the need for discrete multichannel or multistage design by integrating all the bandwidth and output frequency capabilities in a single chip.



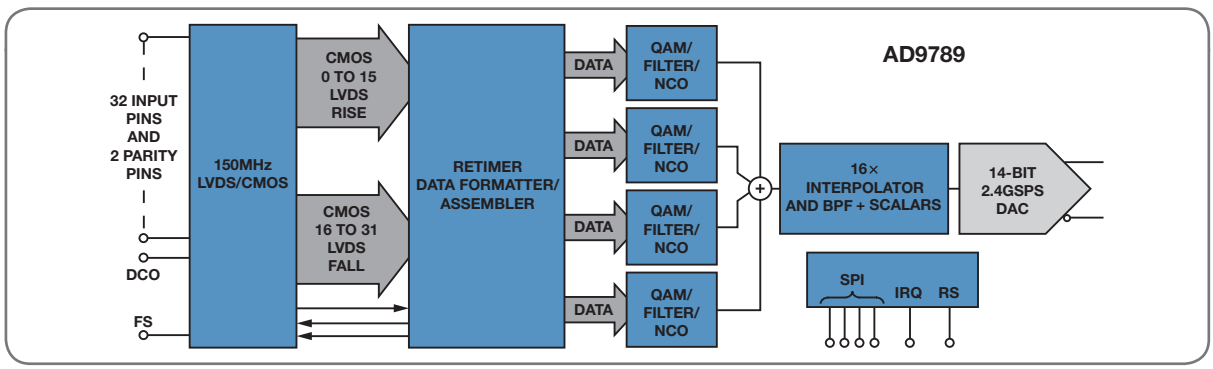
AD9739 block diagram.



AD9739A block diagram.

The AD9789 is a flexible QAM encoder/interpolator/upconverter combined with a high performance 2400 MSPS, 14-bit RF DAC. The flexible digital interface can accept up to four channels of complex data, and the QAM encoder supports constellation sizes of 16, 32, 64, 128, and 256 with SRRC filter coefficients for all standards. The on-chip rate converter supports a wide range of baud rates with a fixed DAC clock. The digital upconverter can place the channels anywhere from 0 to 0.5 × fDAC. This permits four contiguous channels to be synthesized and placed anywhere from dc to fDAC/2 (see AD9789 block diagram below).

With 1.6 W power consumption at full rate, the AD9789 provides the most integrated solution for multicarrier transmit systems required to modulate and synthesize independently up to four channels for output frequencies below 2.5 GHz. The AD9789 eliminates the need for multichannel or multistage design by integrating the modulation and output frequency capabilities in a single chip.



AD9789 block diagram.

Mixed-Signal Front-End ICs Combine Dual Transmit DAC and Wideband ADC to Reduce Power and PC Board Space in Wireless Communications Equipment

Cost- and space-sensitive wireless equipment, such as femtocell and picocell base stations and portable radios, require high levels of integration in their transmit-and-receive signal paths to reduce board space and system cooling requirements.

Solution

Mixed-signal front-end ICs (MxFE® devices), pioneered by ADI, provide that solution by integrating the required high performance transmit DACs and receive ADCs onto a single chip, while tailoring their dynamic range for compliance with multicarrier applications. The 12-bit AD9963 and pin-compatible 10-bit AD9961 MxFE devices use 40% less power and 25% less printed circuit board area and enable up to 10 dB better ACLR (adjacent-channel leakage ratio) performance than competing devices.

AD9963 and AD9961 Features

- Dual-channel, 10-bit (AD9961) and 12-bit (AD9963), 170 MSPS digital-to-analog converter Tx path configurable for 1×, 2×, 4×, and 8× interpolation
- ACLR = 74 dBc (12 bits)
- Dual-channel, 10-/12-bit, 100 MSPS analog-to-digital converter Rx path includes a bypassable 2× decimating low-pass filter
- SNR = 67 dB (12 bits), F_{IN} = 30.1 MHz
- 5 channels of analog auxiliary input/output (two 12-bit DACs, two 10-bit DACs, and a 12-bit ADC)
- 1.8 V single-supply operation; <425 mW at maximum sample rates
- Supports full- and half-duplex data interfaces
- Small 72-lead LFCSP lead-free package
- Pricing:
  - AD9963—$29.50
  - AD9961—$25.75

Applications

- Wireless infrastructure
- Picocell, femtocell base stations
- Medical instrumentation
- Ultrasound AFE
- Portable instrumentation
- Signal generators, signal analyzers

Recommended Complementary Components in Femtocell Base Stations

- ADF4602 3G multiband transceiver
- ADL5501 rms power detector
- RF amplifiers: ADL5320, ADL5542, and ADL5601

Octal 16-/12-Bit *dense*DAC Devices Available in Tiny 2.645 mm × 2.645 mm Package

ADI's *dense*DAC® digital-to-analog converter portfolio offers products that combine high DAC channel count with a small package and low power, at low cost. The AD5668/AD5628 *dense*DAC devices are octal 16-/12-bit SPI rail-to-rail DACs with an integrated reference, which are now available in a 2.645 mm × 2.645 mm, 16-lead WLCSP package, as well as 4 mm × 4 mm, 16-lead LFCSP and 16-lead TSSOP. With the AD5668/AD5628 there is no need to let space constraints force you to accept lower performance. These parts offer eight buffered voltage output DAC channels and integrated 1.25 V reference with 5 ppm/°C tempco in a tiny package. They are ideally suited to applications such as optical transceivers, base stations, and instruments. The AD5668/AD5628 DNL spec of ±1 LSB max meets the performance requirements for closed-loop systems. The related AD5669R/AD5629R products offer an I²C rather than SPI interface.

Easy Precision DAC Evaluation Using SDP

The AD5668 can be evaluated using the System Demonstration Platform (SDP), which is designed to be low cost, reusable, and versatile. The platform is compatible with a growing number of precision ADI components.

AD5668/AD5628 Features

- Tiny 2.645 mm × 2.645 mm WLCSP package
- 8 DAC channels
- On-chip 1.25 V reference with 5 ppm/°C tempco
- 2.7 V to 5.5 V power supply
- Guaranteed monotonic by design
- Power-down to 400 nA @ 5 V, 200 nA @ 3 V
- Pricing:
  - AD5668—$11.39
  - AD5628—$7.70

Applications

- Optical transceivers
- Base station power amplifier control
- Process control
- Portable battery-powered instruments

Versatile, Easy to Use, Precision DAC Building Block Components in a Compact Package

Across a range of applications from instrumentation to communications, system developers require easy to use versatile DACs, which provide true 16-bit precision to facilitate their use as a core building block component.

Solution

This challenge is addressed by the AD5541A (16-bit), AD5542A (16-bit), and AD5512A (12-bit) family of core building block DAC devices. These single-channel, high performance, unbuffered voltage output DACs operating from a single supply are ideally suited for a wide range of applications where precision is required. They deliver full 16-bit resolution and accuracy, low noise performance (11.8 nV/√Hz), low drift (0.05 ppm/°C), and low glitch impulse (1.1 nV/sec). Specified over a wide temperature range from −40°C to +125°C, this family is classified for 5 kV HBM ESD, making these devices highly robust solutions in any environment. Their fast settling time of 1 µs with low offset errors makes them ideal for high speed open-loop control. The AD5512A/AD5542A incorporate a bipolar mode of operation that generates a $\pm V_{REF}$ output swing via integrated internal feedback resistors, while also including Kelvin sense connections for the reference and analog ground pins to reduce layout sensitivity.

AD5541A/AD5542A/AD55121A Features

- 16-bit and 12-bit resolution
- 11.8 nV/√Hz noise spectral density
- 1 µs settling time
- 0.375 mW power consumption at 3 V
- 50 MHz SPI/QSPI™/MICROWIRE®/DSP-compatible interface
- Pricing:
  - AD5541A/AD5542A—$6.25
  - AD5512A—$3.12

Recommended Complementary Components

- AD8628/AD820 single-supply RRIO amplifier
- ADR421 low noise 2.5 V reference

Reference Circuits

Circuits from the Lab™ Reference Circuits

Precision, 16-Bit, Voltage Level Setting with Less than 5 mW Total Power Dissipation Using the AD5542A/AD5541A. Complete documentation available at *www.analog.com/CN0181*.

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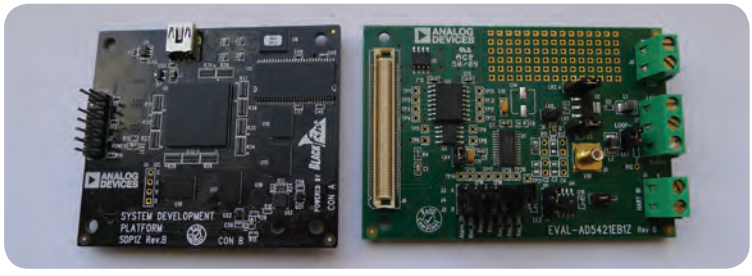
New System Demonstration Platform Facilitates Quick Prototyping and Evaluation

System design can be a complex problem with many different elements to comprehend, but the ability to prototype and quickly demonstrate subsections of the solution can simplify the process and, more importantly, reduce the risks faced by designers. Analog Devices' System Demonstration Platform (SDP) is comprised of a series of controller boards, interposer boards, and daughter boards that implement an easy to use evaluation system for ADI components and reference circuits. With the SDP, system designers can reuse central elements, allowing subsections of their designs to be evaluated and demonstrated prior to the final system implementation. Familiarity gained from prior use of the platform makes it easy for users to evaluate new categories of components in an environment they already know and understand.



SDP-B controller board connects to AD5421 DAC evaluation board.

Sample of SDP-Compatible DAC Evaluation Boards

- AD5421: 16-bit, serial input, loop-powered, 4 mA to 20 mA DAC
- AD5791/AD5781: 1 ppm 20-bit, ±1 LSB INL, voltage output DAC
- AD5755-1: quad channel, 16-bit, serial input, 4 mA to 20 mA and voltage output DAC, dynamic power control, HART connectivity
- AD9837: low power, 8.5 mW, 2.3 V to 5.5 V, programmable waveform generator
- AD9838: 11 mW power, 2.3 V to 5.5 V, complete DDS

To learn more about the SDP and to view a full list of compatible products and circuits, please visit: *www.analog.com/sdp*.

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I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

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