ANALOG DEVICES

Precision Instrumentation Amplifier

AD620

1.1 Scope.

This specification covers the detail requirements for a high accuracy, resistor programmable, precision monolithic instrumentation amplifier. The AD620 requires only a single external resistor for gain selection.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
−1	AD620S(Q)/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
Q	Q-8	8-Pin Ceramic DIP Package

1.3 Absolute Maximum Ratings. (T_A = +25°C unless otherwise noted)

Supply Voltage . . . . . ±18 V
Internal Power Dissipation[1] . . . . . 650 mW
Input Common-Mode Voltage, Range . . . . . $\pm V_S$
Differential Input Voltage . . . . . ±25 V
Rated Operating Temperature Range . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature Range (Soldering 10 seconds) . . . . . +300°C

NOTE
[1]Maximum internal power dissipation is specified so that T_J does not exceed +175°C at an ambient temperature of +25°C. For temperatures above +25°C, derate the Q-8 package @ 6.7 mW/°C.

1.5 Thermal Characteristics.

Thermal Resistance:
8-Pin Ceramic DIP Package: θ_{JA} = 110°C/W
θ_{JC} = 22°C/W

REV. A

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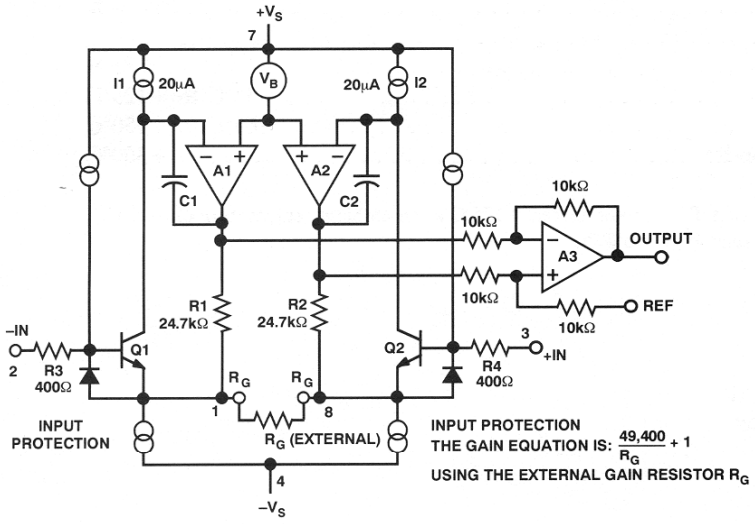
AD620—SPECIFICATIONS

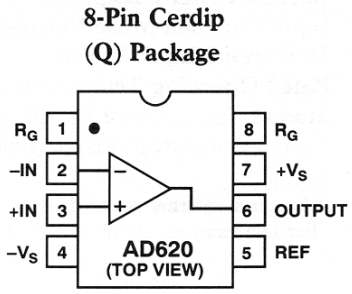
Table 1.

Test	Symbol	Device	Design Limit @ −55°C & +125°C	Sub Group 1	Sub Group 2, 3	Test Conditions[1]	Unit
Gain Error, G = 1	GE_1	−1		0.1	0.6	G = 1, V_O = ±10 V	±% max
Gain Error, G = 100	GE_{100}	−1		0.3	0.8	G = 100, V_O = ±10 V	±% max
Gain Error, G = 1000	GE_{1000}	−1	1.2			G = 1000, V_O = ±10 V	±% max
Input Offset Voltage	V_{OSI}	−1		125	225	V_{IN} +0 V	±μV max
Output Offset Voltage	V_{OSO}	−1		1000	2000	V_{IN} = 0 V	±μV max
Input Bias Current	I_B	−1		2	4	G = 1	±nA max
Input Offset Current	I_{OS}	−1		1	2	G = 1	±nA max
Common-Mode Rejection	$+CMRR_1$	−1		73	73	G = 1, V_{IN} = 0 V to +10 V	dB min
Common-Mode Rejection	$-CMRR_1$	−1		73	73	G = 1, V_{IN} = 0 V to −10 V	dB min
Common-Mode Rejection	$+CMRR_{100}$	−1		110	110	G = 100, V_{IN} = 0 V to +10 V	dB min
Common-Mode Rejection	$-CMRR_{100}$	−1		110	110	G = 100, V_{IN} = 0 V to −10 V	dB min
Power Supply Current	I_{CC}	−1		1.3	1.6	G = 1, V_S = ±15 V	mA max
Power Supply Rejection	$PSRR_1$	−1		80	70	G = 1, V_S = ±2.3 V to ±18 V	dB min
Power Supply Rejection	$PSRR_{100}$	−1		110	100	G = 100, V_S = ±2.3 V to ±18 V	dB min

NOTE
[1]V_S = ±15 V, R_L = 2 kΩ, unless otherwise noted.

3.2.1 Simplified Schematic and Package Pinout.



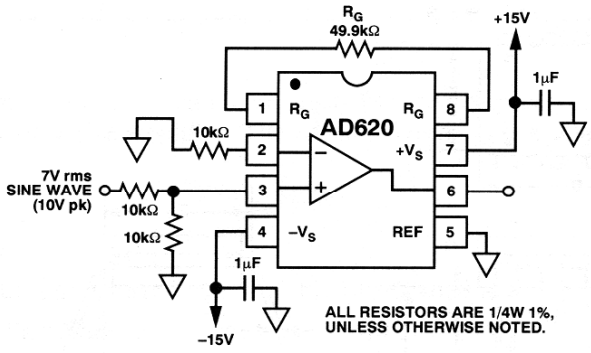


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (49).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).

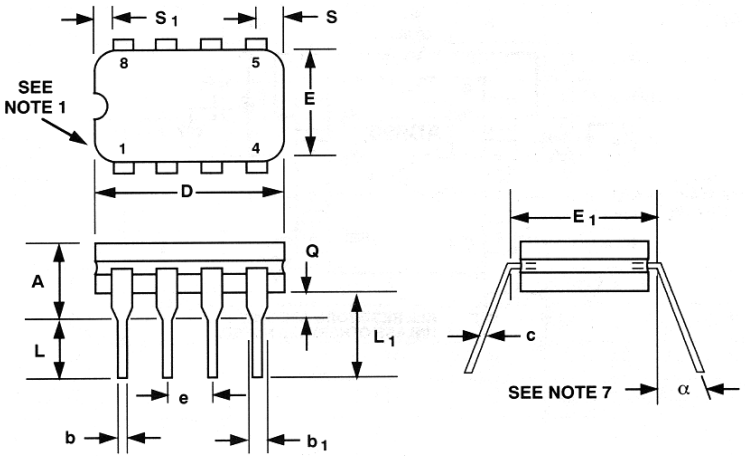


ESD Susceptibility

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 volts, which readily accumulate on the human body and on test equipment, can discharge without detection. Although the AD620 features proprietary ESD protection circuitry, permanent damage may still occur on these devices if they are subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid any performance degradation or loss of functionality.

OUTLINE DIMENSIONS

8-Lead Cerdip Package



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.200		5.08	
b	0.014	0.023	0.36	0.58	7
b_1	0.038	0.065	0.96	1.65	2, 7
c	0.008	0.015	0.20	0.38	7
D		0.405		10.29	4
E	0.220	0.310	5.59	7.87	4
E_1	0.290	0.320	7.37	8.13	6
e	0.100 BSC		2.54 BSC		8
L	0.125	0.200	3.18	5.08	
L_1	0.150		3.81		
Q	0.015	0.060	0.38	1.52	3
S		0.055		1.35	5
S_1	0.005		0.13		5
α	0°	15°	0°	15°	

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023″ (0.58 mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. Applies to all four corners.
6. Lead center when α is 0°. E_1 shall be measured at the centerline of the leads.
7. All leads–increase maximum limit by 0.003″ (0.08 mm) measured at the center of the flat, when hot solder dip lead finish is applied.
8. Six spaces.

C1691–7–8/92

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