ANALOG DEVICES

AN-502
APPLICATION NOTE

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Designing a Superheterodyne Receiver Using an IF Sampling Diversity Chipset
by Brad Brannon

Abstract: The paper introduces a chipset to simplify receiver design and puts forth a design example based on GSM but can be extended to many open or closed air interface. Advances in analog converter technology now allow IF sampling which can greatly simplify receiver design. Advances in digital integrated circuits also advance the state of the art in terms of digital tuning and filtering. Together these two chips can replace many of the cumbersome stages of a traditional analog receiver with predictable and reliable performance.

The superheterodyne receiver is still a workhorse in receiver technology. It has served its duty faithfully for many years now. However new technologies in receiver component designs are offering to extend the possibilities into the digital age.

A typical receiver design may consist of two or three down conversions to provide the sensitivity and selectivity required of the individual receiver. With each down conversion, a local oscillator, mixer and filter are required. Each additional stage adds complexity, cost and difficulty of manufacture.
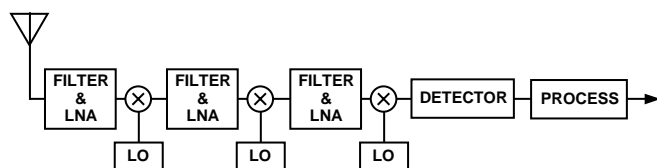

Figure 1. Typical Receiver Block Diagram

As shown above in the block diagram, receiver technology can be "straight forward", however, implementation and manufacture can be another story.

There are several key issues that must be addressed. Of course, the issues of noise and intercept point are always of concern when it comes to receiver design. However, in moderate and high volume applications, questions about assembly and test begin to arise. It is one thing to build one in the lab, but it is a completely different story to build many in production. With three local oscillators, mixers and IF strips, alignment can be a real issue, even with automated tools. To keep manufacturing cost low, several of these analog stages must be eliminated, but how can this be done without

sacrificing performance? Perhaps the real question is can performance be enhanced. One solution is to digitize the analog signals and do the processing in a DSP. Once in the digital domain, many creative and proprietary processes can take place to enhance and add value, while eliminating many of the manufacturing problems (alignment and component yield) that often increase the cost of manufacturing and reduce margins.

Already, it is common practice to use an analog-to-digital converter to form the detector and a DSP (digital signal processor) to process the data. However, this does not reduce the cost or complexity of the design (to digitize the baseband), it simply adds flexibility. What is needed is an analog to digital converter that can digitize closer to the antenna. Sampling at the antenna is not realistic since some amount of band select and filtering must occur prior to the ADC to minimize adjacent channel issues. However, sampling at the first IF is practical.
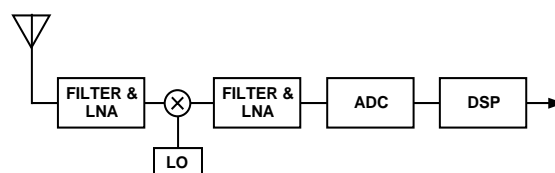

Figure 2. Digital Receiver Block Diagram

IF SAMPLING

Recent advances in converter technology have allowed data converters to faithfully sample analog signals as high as several hundred MHz. Sample rates need only be as high as twice the signal bandwidth to keep the Nyquist principle. Since most air interface standards are less than a few MHz wide, sample rates in the tens of MHz are required, eliminating the need for extremely fast sample rates in radio design. Thus allowing for low cost digitizers.

One such analog to digital converter (ADC) that performs this function is the AD6600. The AD6600 can digitize up to 20 MSPS and sample analog signals up to 250 MHz with 60 dB spurious free dynamic range. In addition to high performance data conversion, this ADC also includes gain control and dual inputs to facilitate diversity applications.
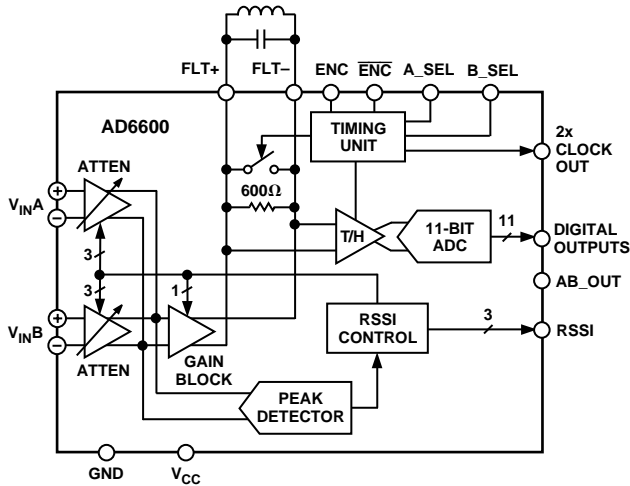
Figure 3. AD6600 Block Diagram

The block diagram above shows the details of the AD6600 IF data converter. The AD6600 Dual Channel, Gain Ranging ADC with RSSI (Receiver Signal Strength Indicator) consists of three stages. The first consists of a pair of 1 GHz phase compensated step attenuators followed by an output selection multiplexor. The second stage is a wide input bandwidth 11-bit ADC based on the AD9042, 12-bit 41 MSPS analog-to-digital converter. The third stage is a high speed synchronous peak detector and RSSI control interface. Together these on-chip systems form a high dynamic range IF sampling ADC. The AD6600 is fabricated on an advanced bipolar integrated circuit process.

The input attenuator consists of two identical inputs. These dual inputs may be diversity channels, two independent IF signals or only one input may be used. The attenuation factor is controlled through a range of 30 dB in 6 dB steps by on-chip switches. The matching between the gain settings is better than 0.5 dB and maintains a bandwidth of almost 1 GHz so the phase delay is small. Likewise the phase mismatches between different attenuator settings is very small, less than 0.2 degrees up to 200 MHz analog input. Additionally, the input impedance does not change with attenuator settings so there is no AM to PM distortion.

Since one ADC serves both attenuator inputs, two control pins are provided to select which attenuator is connected to the ADC. The options allow one or both inputs to be connected to the ADC. When both inputs are selected, the ADC alternates between the two on a clock by clock basis. An output pin, AB_OUT, indicates which input is currently available on the digital output simplifying interface logic.

The on-chip RSSI (Receive Strength Signal Indicator) controls the Input attenuator. The RSSI peak detector function consists of a high-speed comparator bank. The peak detector has five reference points, with each reference point being 6 dB lower than the previous one.

A regenerative positive feedback comparator is tied to each point and referenced to full-scale of the A/D converter. Once one of the comparators is tripped it stays in the state until it is reset by the falling edge of the encode. The 5 comparator outputs are decoded into a 3-bit word that is used to select the proper attenuation. Six dB of digital hysteresis is used to eliminate level uncertainty at the threshold points due to noise and amplitude variations. The peak detector monitors both positive and negative excursions of the input signal to accurately track complex modulated signals.

The RSSI follows the IF envelop one clock cycle before the conversion is made. During this time period, the RSSI watches for the signal peaks and prior to digitization, the RSSI word is set to the appropriate attenuation factor to prevent the ADC from overranging on the following conversion cycle. The RSSI always allows an extra 6 dB of ADC headroom to prevent clipping if the signal power has increased unexpectedly. This is true until the last attenuator is selected. Then the ADC will clip in a normal manner. The RSSI word is made available to read via the RSSI pins. The 11-bit ADC output forms the mantissa of a binary floating point word, while the RSSI the exponent. This data can be interpreted in several ways. The data can be converted in software by using the following pseudo-code:

```
r0 = dm(rssi);
r2 = 5;
r0 = r2-r0;
r1 = dm(adc);(11 bits, MSB justified into DSP word)
rshift r1, r0; (arithmetic shift to extend the sign bit)
```

An ASIC/PLD can be used to convert the code to fixed point or a digital preprocessor such as the AD6620 (to be discussed later) can be used to convert the data. The resulting data can then be treated as a standard 16-bit fixed point word.

Since the analog front end has a bandwidth of nearly one-gigahertz and the ADC a bandwidth of 450 MHz, a filter is required to bandwidth limit the wideband noise out of the attenuator and MUX stage. This simple external LC filter is tuned to the chosen IF frequency and is designed to settle quickly between clock cycles. To expedite settling between samples, an internal clamp circuit is utilized to discharge the filter. This minimizes feed through between inputs (cross talk) because of the natural time constant of the resonant network. Overall, the AD6600 achieves 60 dB SFDR and 57 dB SNR with analog inputs up to 300 MHz, providing true IF sampling with baseband performance. See Figure 4.

Once digitized, the signal would have to be processed. With a typical sample rate of 20 MHz, data would stream too fast for even the hottest DSP to do much with in terms of filtering, much less process the data for user

information. Therefore, some preprocessing of the data must occur. With a sample rate of 20 MHz, the data bandwidth would be 10 MHz, much more than is needed for most air interfaces. Therefore, one thing that preprocessing should achieve is to reduce the data bandwidth as well as the data rate. Thus in addition to the ADC (analog-to-digital converter) a DSP preprocessor is required.
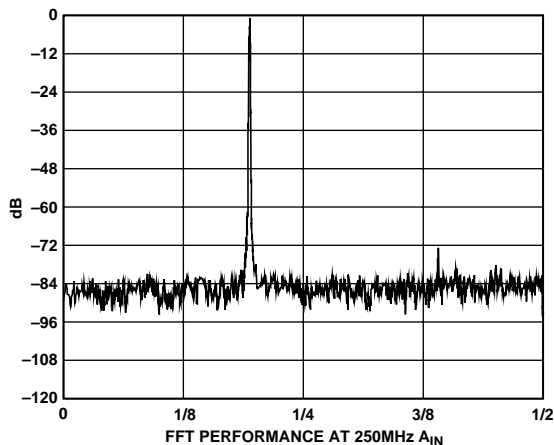

Figure 4. AD6600 FFT with 250 MHz Analog Input

DIGITAL PREPROCESSING
As shown in the diagram below, the AD6620 performs many functions. First it functions as a quadrature demodulator, separating the I and Q signals for later processing. The CIC (cascaded integrator comb) filters provide data rate decimation and low pass filtering. Overall decimation rates can be programmed from 1 (inclusive) to over 8192. The RAM Coefficient Filter, a sum of product design, provides programmable filter performance, covering a wide range of designs.
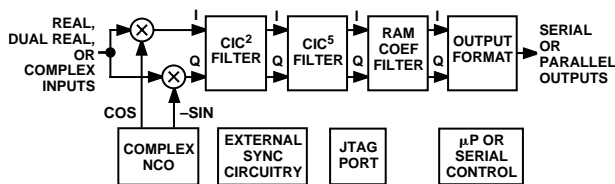

Figure 5. AD6620 Block Diagram

The numerically controlled oscillator (NCO) provides spurious performance to better than –105 dBc. This ultra clean digital local oscillator is mixed with the digitized input through 18-bit multipliers. As shown in the spectral plot below of the NCO, spurious performance is hidden well in the 16-bit noise floor shown below.

Interstage precision is maintained at 18 bits while individual stages use much higher precision to prevent artifacts due to truncation. Data out of the AD6620 can be delivered to the DSP through either a standard serial interface or through a parallel interface as a memory mapped address device. Data can be delivered in 16-, 24- or 32-bit precision.
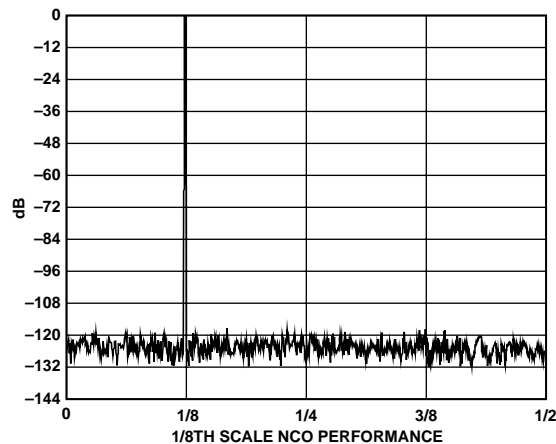

Figure 6. AD6620 NCO Spurious Performance at 1/8th the Clock Rate

DIVERSITY CHIPSET
The AD6600 and AD6620 form the heart of a chipset for IF sampling and processing. Between the two chips, AGC, digitizing, data rate reduction and channel filtering are performed. The benefits from this pair are immense. First, the integration level allows reduced system size and power reduction. This is achieved through the elimination of analog IF stages along with their respective components. Second, alignment time is greatly reduced. Since filters and oscillators are now digitally implemented there is no need to adjust them at the point of manufacture.
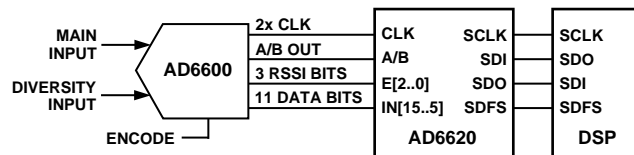

Figure 7. AD6600/AD6620 Diversity Receiver Chipset

Aside from the figures of merit mentioned above, the chipset also features a seamless interchip interface. The interchip connections are point to point and are designed for single layer wiring. Additionally, the serial output port of the AD6620 wires directly to a number of industry standard DSPs including the ADSP-21xx and ADSP-210x families.

The Diversity Chipset is applicable for many different air interfaces including narrow band FM, IS-136, CDMA, GSM and many others. The use of such a chipset requires many of the traditional techniques in receiver design as well as some new considerations. However, the end result is a more economical solution capable of much more than a traditional analog receiver.

GSM and the Diversity Chipset
The remainder of this report focuses on a design analysis of one such design. The chosen example is GSM because it is one of the most technically challenging in terms of selectivity. The analysis shown can just as

easily be applied to any of the other standards and have already been implemented. The front end is traditionally referred to as the "radio" and consists of the antenna connection through the ADC.

This report reviews the RF performance requirements in terms of the Diversity Chipset. Throughout this writing, certain assumptions about the RF section, ADC noise and process gains (to be explained later) are made. The basis of this work is the GSM specification for 900 MHz as proposed by ETSI recommendation 05.05. Since variations in receiver design exist, many possible designs solutions exist, this being but one. Many options exist in terms of sample rate, decimation and digital signal processing that change the receivers ability to deal with noise. In fact, the post ADC processing (DSP) determines much of the total receiver performance, and as a result, represents much of the proprietary information surrounding many manufacturers total receiver design.

Block Diagram
The following diagram is the one analyzed and will form the core discussion from this point forward. Various advantages will be discussed to many of the options.

The design consists of one RF strip and 1 IF strip. The RF section has a net gain of only about 3 dB, considering the filter losses and mixer conversion loss. As with traditional receiver designs, most of the gain is in the IF strip where filters have improved selectivity sufficiently to prevent overdrive from off channel signals (adjacent channel rejection). This forms a single analog down conversion with a second down conversion being performed digitally by the AD6620.

In the front end, the LNA is in front of the mixer. This arrangement minimizes noise figure because the lossy element is behind a gain block. Another possibilities is that the mixer could be ahead of the LNA which maximizes intermodulation performance, although, as seen later in the analysis, meeting spurious performance is not too difficult with the amplifier ahead of the mixer. However, with the mixer ahead of the amplifier, receiver noise figure is insufficient to meet sensitivity requirements due to the insertion loss of the mixer.

After the mixer and band pass filter is a fixed gain amp. This amplifier is working with relatively small signals and has no difficulty with intermodulation performance. The bulk of the IF gain is located between the two SAW filters. This allows adjacent signals to be attenuated prior to amplification, which improves the intermodulation performance. The last component in the analog chain is the second SAW filter. This effectively eliminates harmonics of the amplifier chain prior to digitization.

The first amplifier between the SAWs could be a variable gain amp as shown. This is not used for AGC purposes but instead to remove variation in component values either from lot to lot, or over temperature. Tolerances in insertion loss can be removed as a system calibration by setting the gain of this amplifier. Insertion losses of filters, mixers and amplifiers often worsen as temperature increases. The gain of this amplifier could be configured to increase with temperature to compensate for reduced conversion efficiency as a function of temperature.

Total RF and IF conversion gain is 35 dB to 40 dB. With a maximum input signal of –13 dBm, this would overdrive the ADC. The last IF amplifier should be a limit or clipping amplifier to prevent this. This does not adversely effect performance since the input signal is phase modulated. Adaptive equalization requires amplitude information, however at the point where the signal is so large as to overdrive the data converter, equalization is no longer necessary. The demodulation/equalization process will still recover the signal.

Total receiver dynamic range is derived from the RF/IF processing above, plus the 30 dB of gain ranging provided by the AD6600 as well as the 11-bit ADC incorporated in the AD6600.

RF Filtering
The purpose of the helical (preselect or band select) filter is to block out of band signals from entering the RF stages of the receiver. In a typical base station, this filter could consist of the bandwidth characteristics of the antenna, the RF trap or coupler (to keep Tx out of the Rx), and the broad band pass filter. As seen below, this filter should exhibit the lowest insertion loss possible, because receiver NF is directly (1 dB per dB) related to insertion loss at the front of the chain. High performance receivers would likely integrate a low loss microstrip filter directly on the PCB to minimize loss in this stage, especially 1800 MHz and 1900 MHz applications. This filter may also be a helical or dielectric filter, which is used to perform band filtering. This filter ensures that following stages are not disrupted by any remaining out of band signals, including the base station transmit signals. The filters can be designed specifically to block the transmit side as in TOKO part numbers 6DFSC and 6DFSD.
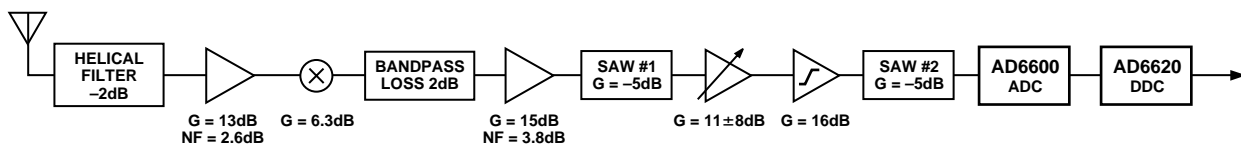

Figure 8. Signal Path Details

RF Amplifiers and Mixers

RF gain stages are available in many forms, including discrete, monolithic and hybrid/MCM technologies. Vendors such as Watkins-Johnson, M/A-Comm, Mini-Circuits and RF Micro Devices offering RF front ends suitable for use in many low noise, high intercept applications. Two of the better amplifiers are the AH1 and RF2312 (manufactured by Watkins-Johnson and RF Micro Devices respectively). These devices provide 13 dB to 15 dB of gain with noise figures of 2.6 dB and 3.8 dB respectively with even better performance planned in the future.

While large RF gains improve noise figure they also reduce intermodulation performance by increasing wideband signal levels to the mixer. As shown, the architecture requires 13 dB of gain.

Low loss mixers should also be used; however, they should have high intercept points. For example, a mixer with a +27 dBm LO drive level typically provides an input intercept point of +37 dBm. Thus, two signals at –43 dBm would give 3rd order intermodulation products at about –200 dBm. However, if the intercept point were lowered to +17 dBm, these products would increase to –163 dBm. As signal levels are increased, intermodulation performance will reduce rapidly. However, the GSM specification requires only –43 dBm two-tone intermodulation performance when receiving a reference sensitivity signal. Although most manufacturers work hard to exceed required performance, many mixers in this performance range are available. With this in mind, the highest intercept point mixers readily available should be used. Thus, for this reference design, a +27 dBm LO drive level mixer is specified. These are available from a number of sources, including Mini-Circuits. Insertion loss for this mixer is 6.3 dB.

In addition to the large LO drive levels for optimum performance, these LO signals must exhibit very low phase noise performance. The frequency domain process of the mixer is convolution (the time domain process of the mixer is multiplication). As a result of mixing, phase noise from the LO causes energy from adjacent (and active) channels is integrated into the desired channel as an increased noise floor. To determine the amount of noise in an unused channel when an alternate channel is occupied by a full-power signal, the following analysis is offered.

Although not usually the case, assume that the phase noise in the 200 kHz GSM channel is constant at this level (most often, phase noise reduces with carrier offset). In this case, the following equation is valid:

$$Noise = \int_{f=-0.1}^{+0.1} x(f) \times p(f)\, df$$

where Noise is the noise in the desire channel caused by phase noise, x(f) is the phase noise expressed in non-log format and p(f) is the spectral density function of the GMSK function. For this example, assume that the GSM signal power is –13 dBm. Also, assume that the LO has a phase noise that is constant across frequency (most often, the phase noise reduces with carrier offset). Under these assumptions when this equation is integrated over the channel bandwidth, a simple equation falls out. Since x(f) was assumed to be constant (PN—phase noise) and the integrated power of a full-scale GSM channel is –13 dBm, the equation simplifies to:

$$Noise = PN \times Signal_{adjacent}$$

or in log form,

$$Noise = PN_{log} + Signal_{log}$$

$$Noise = PN + (-13\ dBm)$$

$$PN_{required} = Noise - (-13\ dBm)$$

Since the goal is to require that phase noise be lower than thermal noise. Assuming that thermal noise at the mixer is the same as at the antenna, –121 dBm (thermal noise in 200 kHz at the antenna) can be used. Thus, the phase noise from the LO must be lower than –108 dBm with an offset of 200 kHz.

IF Amps and IF Configuration

In all radio designs, the IF is the most critical stage. Most of the receiver selectivity and almost all blocker rejection is gained in the IF stage though the use of ceramic, crystal or SAW filters. The balance of the selectivity is gained through oversampling and FIR filtering. In GSM as well as other standards, the SAW filters play a vital role in the implementation of this receiver. First, the SAW filters do provide some channel selection, but not in the usual sense where all adjacent signal are removed. The second and primary purpose of the SAW filters is to keep the AGC (RSSI in the AD6600) from responding adversely to adjacent and alternate channel signals. Third, they should adequately block unwanted mixer signals from entering the analog-to-digital converter.

This is actually quite important since large LO and RF signals are present in the mixer output and the AD6600 has a 1 GHz, RSSI input bandwidth. The blocking characteristics of the SAW filters are important in order to keep the RSSI circuitry from tracking an unwanted signal. These unwanted signals can take several forms. The obvious is adjacent or alternate channel signals. They could also include RF signals coupling directly from the antenna or even take the form of an LO signal coupling through the mixer. Several things can be done to minimize interstage coupling of these out of band signals. First, careful shielding and grounding can minimize interstage coupling and, second, proper impedance matching can maximize the efficiency of the filter.

In cases where contamination is not through conduction, but radiation and coupling, a differential IF stage can greatly aid in the suppression of feed through signals. For example, in cases such as radiation, differential inputs would likely receive the same contamination. Due to very low common-mode gain of the filters, amplifiers and ADC's, effective contamination will be greatly reduced. Since SAW filters are generally differential in, differential out devices, this common-mode rejection should be taken advantage of in the design of high performance receivers. Additionally, differential IF amplifiers that aid in matching differential filters to amplifiers are becoming available. Already, many high performance ADCs take advantage of differential mode inputs, such as the AD6600 and AD6640.

SAW Filter Requirements
In addition to digital filtering provided by decimating filters such as the AD6620, SAW filters are required to filter unwanted signals from the ADC input. If insufficiently filtered, these signals will be aliased back into the usable band of the AD6600 and cause C/I problems. If severe enough, the unwanted image could dominate the demodulation process and become the primary signal instead of the image. The GSM specification refers to these as blockers. To determine what filter requirements are needed, the following discussion is offered. Some references are made to the AD6600 and AD6620, but where necessary, the AD6600 and AD6620 data sheets should be referenced.

The AD6600 for GSM applications can be run at 13 MSPS. It can be run in two modes. The first is sampling only 1 IF signal with an effective sample rate of 13 MSPS. The second option is sampling both a main antenna and a diversity antenna, each at 6.5 MSPS. The second option will be considered here because it poses the strictest specifications on the SAW filters. Relaxation's can be achieved by increasing the sample rate, which softens the transition band requirements of the filters. Other common sample rates for GSM include 17 1/3 (64 × bit rate) and 19.5 (72 × bit rate) MSPS.

The main RF LO will have 200 kHz steps for channel selection. The NCO of the AD6620 can perform additional fine-tuning when fine-tuning is necessary due to Doppler Shift or handset frequency tolerance.

For this example, a sample rate of 6.5 MHz is used. Thus, the Nyquist bandwidth will be 3.25 MHz with a 13 MSPS clock and operating in diversity mode. The aliased IF will therefore be placed at or near 1.6 MHz. For this example, an IF frequency of 170.0 MHz was chosen. While other choices exist, 170 MHz works for both low and high side injection at both 900 and 1800 MHz. This allows the sampled IF to fall no less than 1.6 MHz from either dc or FS/2 for a variety of sample rates.

From the GSM specification 05.05, in-band blocking requirements are as shown below:

600 kHz ≤ Offset < 800 kHz	–26 dBm Signal Level
800 kHz ≤ Offset < 1.6 MHz	–16 dBm Signal Level
1.6 MHz ≤ Offset < 3 MHz	–16 dBm Signal Level
>3 MHz	–13 dBm Signal Level

In addition to the in-band blocking requirements, consideration must be given to co-channel and adjacent channel interference. Co-channel interference can not be filtered and must be accounted for in the equalization. The specification allows for co-channel C/I of up to 9 dB. Additionally, interferers in the next channel over (±200 kHz, which is the adjacent channel) are difficult to filter and must be eliminated with the digital filter (i.e., the AD6620), accommodated for in the equalization, or assumed not present. At 400 kHz offset (alternate channel), GSM also specifies that the interferer can be 41 dB stronger than the signal of interest. Some filtering can be expected from the SAW filters and more from the digital filter as shown below.

In the AD6600, the blockers and interferers cause 2 main problems. The first is that they can disrupt the RSSI circuitry causing the gain control circuitry to respond to one of the adjacent channels and not the one of interest, thus causing the receiver to be desensitized. The second problem is that if the IF output is inadequately filtered then signals that are outside the Nyquist band will be aliased back in band and possibly override the signal of interest. With these points in consideration, a SAW filter specification can be defined that prevents disruption of the RSSI control and prevents aliasing of out of band signals back in band by the sampling process.

Before an in-depth analysis of the SAW filter requirements, the receiver sensitivity analysis must first be performed in order to understand what the signal levels are and by how much they must be attenuated.

GSM Receiver Sensitivity
Receiver sensitivity is largely based on the noise figure. By careful selection of IF frequencies and ADC signal placement, the effects of harmonics can be greatly reduced. Additionally, the use of dither can also improve some types of spurious signals.

Receiver Noise
When analyzing the sensitivity of a receiver, the first place to start is by determining how much thermal noise exist in the bandwidth of the signal. The equation below shows the calculation for thermal noise on the receiver input.

$$N_{antenna} = k \times T \times BW$$

In this equation, k is Boltzmann's constant, T is absolute temperature and BW is bandwidth. Evaluating this expression at room temperature and across the 200 kHz GSM signal bandwidth gives 0.8284 femtowatts or –121 dBm.

Total receiver noise can then be calculated using the following equation:

$$N_{IF} = N_{antenna} + G + NF$$

The form of this equation shows that the antenna thermal noise is gained up by the conversion gain "G" of the receiver, plus degraded further by the receiver noise figure. For our purposes "G" is the net sum of signal gains and losses. The noise figure (NF) is not accounted for in "G" and must be separately calculated.

Cascaded Noise Figure of Down Converter
The figure below shows the RF section of the receiver. It is convenient to separate the receiver into a wideband section and a narrow band section. This is due to the fact that once the IF filters begin to filter off channel signals, receiver performance becomes limited by the signal of interest. Conversely, the front end is more sensitive to the effects of off channel signals such as blockers and interferers.
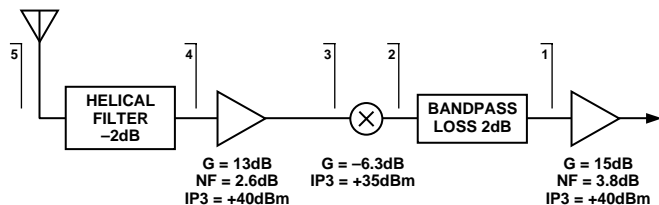

Figure 9. RF Circuit Details

From the circuit above, the cascaded noise figure can be determined. Converting the log numbers above to their linear representations and solving the equation below gives a cascaded noise factor of 1.579.

$$F = 1.585 + \frac{1.819-1}{0.631} + \frac{4.266-1}{0.631\times20} + \frac{1.585-1}{0.631\times20\times0.234} + \frac{2.239-1}{0.631\times20\times0.234\times0.631}$$

$$F = 4.005$$

$$NF = 6.03 \text{ dB}$$

In summary, the front-end section has a cascaded noise figure of 6 dB, a conversion gain of 17.7 dB, and an intercept point of about +38 dBm.

This results in an SNR at the output of the front end of 13.9 dB with the desired test signal at the input of –101 dBm. In terms of intermodulation performance based on 05.05 section 5.2, predicted performance is –153 dBm at the output of the RF stage. This is a C/I almost 70 dB, more than adequate to meet the required performance. Since the mixers are often the most costly item in the design, a cheaper (and lower intercept point mixer) can be used than the one shown here.

Cascaded Noise Figure of IF Processing
From our initial design, the following IF is offered. For the mean time, the variable gain amplifier and limiting amplifiers have been replaced with fixed gain devices. The final design should include the specialty devices shown in the original design.

Figure 10. IF Circuit Details

Examining the noise figure through the IF stage gives the analysis below. The IF stage is broken down as shown above. Power gain through the IF stage is 20 dB. A noise analysis similar to that of the RF stage gives an IF noise figure of 8.88 dB and an intercept point of +34.9 dBm.

Total Cascaded Performance
Total performance for both the RF and IF paths shows that total cascaded gain is 37.7 dB and cascaded noise figure is 6.24 dB. As shown in the fist stage, the C/I in the RF stage is 70 dB. After the SAW filters, they are still insignificant and meet the 9 dB C/I spec for all conditions.
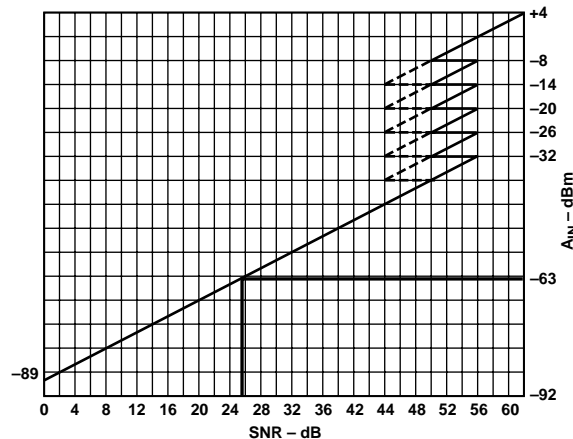

Figure 11. AD6600 SNR vs. Analog Input Power

With an input signal of –101 dBm at the antenna port, the SNR is thus 13.8 dB at the ADC input. The final discussion is thus how much the ADC degrades the SNR of the received signal. To determine this, the input signal level to the ADC must be known. Thus with a –101 dBm signal on the antenna and a conversion gain of 37.7 dB, the input signal to the ADC is –63.7 dBm.

With an input of –63 dBm, the AD6600 provides about 25 dB of wideband SNR. However, since the sample rate is 6.5 MSPS and our signal bandwidth is 200 kHz, the effective SNR is increased by the process gain, in this case 15.1 dB (10 log (6.5/0.2)). Thus the effective SNR of the ADC is about 40 dB.

Assume a full-scale ADC SNR of 60 dB, a full-scale range of about 32 mV (in the smallest range), a signal bandwidth of 200 kHz and a sample rate of 6.5 MSPS. This results in a noise voltage of 307 nV in 200 kHz of bandwidth. In the same 200 kHz of bandwidth, the analog portion of the receiver delivers –77 dBm (–121 + 37.7 + 6.24) of noise power. Into the impedance of the AD6600, this is 64 µV. Thus, the ADC noise is small compared with the

total thermal noise into the ADC. Thus overall the analog portion of the system and not the ADC determines SNR for this receiver. Based on this data, a minimum SNR of 10 dB exists with an input at the reference sensitivity. This is enough to satisfy the requirements of equalization. Better sensitivity can be achieved by selection of quieter analog components, especially the band select filter and the low noise amplifier.

SAW Filter Requirements Continued
As mentioned earlier, the SAW filter provides some amount of receiver selectivity. However the primary goal of the SAW filter is to prevent the adjacent signals from desensitizing the RSSI of the AD6600.

With a signal 3 dB above the reference level of –104 dBm, the ADC input level is –63.3 dBm. At this point, the SNR is 13.9 dB. The key is to maintain this SNR as various blockers and interferers come in-band. This is the purpose of the SAW filters. Since the AD6600 is a gain ranging ADC, out of band signals of sufficient amplitude can desensitize the AD6600 to the desired signals. For example, if a signal passes to the ADC with a level above –32 dBm, the first RSSI trip point will be reached and cause the front end to attenuate the input by 6 dB. This would reduce the SNR by 6 dB. Thus, any undesired signals must be kept at such a level that the input of the AD6600 is kept below –32 dBm on the high side or below –38 dBm on the low side. This is because the AD6600 employs gain hystereses to prevent gain 'chattering' during normal signal fluctuations. Normally, the upper trip point of –32 dBm can be used since normal power up ramping of the transmitted signal will cause the RSSI hystereses control to reset between users. The lower trip point is used in the case of fading profiles when the signal magnitude is falling.

Table I.

Interferer and Blocker	Level	SAW	AD6620
200 kHz	+9 dBc	0	18
400 kHz	+41 dBc	25 dB	25 dB
600 kHz	–26 dBm	37 dB	45 dB
800 kHz	–18 dBm	47 dB	45 dB
>3 MHz	–13 dBm	104 dB	

Table I shows the interferers and blockers of interest. Absent from this list is the 600 kHz interferer (Section 6.3) because it is equivalent to a blocker at –35 dBm, 9 dB below the interferer, which should not disrupt either the AD6600 performance or the equalization. The 600 kHz blocking specification is included in the Table I.

For the interferer specs, the desired signal is 20 dB above the reference point. This generates an SNR of 30.9 dB on an input signal level of –46.3.

With a 200 kHz interferer, the interferer is 9 dB above the signal level at the input, and the analog filters internal to the AD6600 provide little or no rejection. Therefore, at the ADC input, the interferer is about –35 dB. This is not enough to trip the RSSI unless peaking occurs. If this does occur only 1 RSSI step will be inserted causing the SNR to fall 6 dB to 24.9 dB. This is more than enough for equalization with an acceptably low FER.

In the case of the 400 kHz interferer, the signal level on the radio input is 41 dB above the desired signal. Since each of the two SAW filters provide 13 dB of rejection, a total of 26 dB can be expected for a net signal level 15 dB above the desired signal. Thus with the desired signal of –46.3 dBm, the interferer is –31.3 dBm which would cause 1 RSSI step to be inserted and possibly two. In the later case 12 dB of SNR loss would result for a net SNR of 19 dB, still more than adequate for a low frame error rate (FER).

In the case of the blocker tests, the desired signal is 3 dB above the reference sensitivity of –101 dBm. As before, this gives an SNR of 13.9 dB. Now in the 600 kHz case, a maximum block level of –26 dBm must be tolerated. In this case, a minimum rejection of 23 dB is needed from each SAW filter for a total of 46 dB. Thus the input blocker is (–26 + 37.7 – 46) or –34.3 dBm, which is below the RSSI threshold.

Between 800 kHz and 3 MHz, the receiver must tolerate blockers at –16 dBm. From the filter information, the SAW filters provide a total rejection of 56 dB. As before, the blocker is (–16 + 37.7 – 56) or –34.3 dBm, again below the RSSI threshold.

Finally, blockers outside 3 MHz may be up to –13 dBm. The SAW filters provide 106 dB of rejection to these signals. Thus, ADC input levels to >3 MHz blockers are (–13 + 37.7 – 106) or –82 dBm, which are well below any RSSI thresholds. Furthermore, the desired signal is at (–101+37.7) or –63.3 dBm. Since the sample rate is 6.5 MHz and our signal placement puts the signal at 1/4 the clock rate (about 1.6 MHz), the potential exists for the blocker to alias directly on top of our desired signal. In this case however, we have a C/I ratio of (–63.3 – –82.0) or 18.7 dB, 9 dB better than the equalizer is required to tolerate from a co-channel interferer!

Looking at the SAW filter plots below it can be seen that actual rejections are better than those shown by these calculations. This provides greater insurance that RSSI gain stages will not switch improperly and reduce the SNR below 13 dB.

To achieve 106 dB of out of band rejection, two filters must be cascaded. One filter could be used as a roofing filter; however, the burden of the channeling filter would then be placed on a single filter. Therefore, two identical filters would allow the performance to be split equally
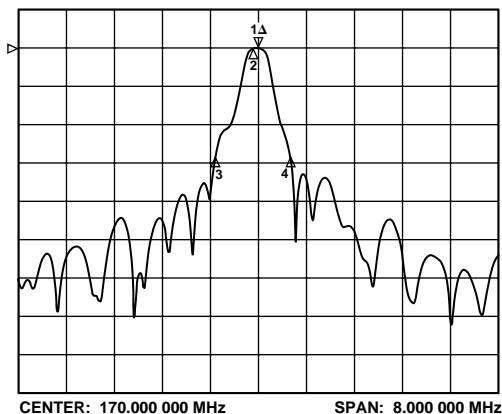
Figure 12. SAW Filter Performance Plot

CENTER: 170.000 000 MHz   SPAN: 8.000 000 MHz

between the two. The following table is used to define SAW filter acoustic performance. In addition to the required rejection, some margin has again been added.

Table II.

	Single SAW Filter Specifications For More Information, Reference SAWTEK Part Number 855297
Offset Frequency	Rejection
100 kHz	0
400 kHz	13
600 kHz	23
800 kHz	28
>3 MHz	53
Insertion Loss	<6 dB
Passband Ripple	<0.5 dB
Delay Variation	<350 ns

Out-of-Band Performance
Outs-of-band specifications require tolerance to 0 dBm blockers. For out of band blockers, the SAW filters provide very little additional rejection. However, the dielectric filters in the RF front end provide additional rejection. Typical filters from TOKO show that 20 MHz out of band, rejection is easily obtainable down to 25 dB. The matching networks of the SAW filters will gain additional rejection. However, worst case images can occur at (0 + 37.7 – 106 – 25) or –93.3 dBm at the ADC input, well below the worst in-band interferers.

Adjacent Time Slot Requirements
Reference sensitivity is measured while the adjacent time slots are at a power level that is 50 dB above the reference level. This does not effect the AD6600 because the RSSI is updated on a per clock basis. Thus when one data burst ends, and the next encode clock for the AD6600 occurs, the RSSI circuit is reset. Even counting

the internal hystereses, only one clock cycle is required before the effects of the old analog input are flushed. Thus, the AD6600 would respond accurately with adjacent time slots at –13 dBm allowing for one sample clock recovery, which is only 4% of a data bit.

Digital Filtering and Decimation
Since the sample rate of the ADC is much higher than the DSP can process, data decimation is required. Additionally, off channel signals and noise must be filtered to improve the SNR of the ADC. The result of oversampling followed by digital filtering is called process gain. Since the sample rate is 6.5 MSPS and the filtered bandwidth must be about 200 kHz for GSM, the process gain is 10 log (6.5/0.2) or 15.1 dB. As stated before, the ADC provides an SNR of about 40 dB under reference signal level conditions. This is more than enough to prevent the AD6600/AD6620 pair from being the performance-limiting portion of the system.

For the GSM receiver, a 6.5 MSPS clock provides 24 times oversampling of the bit rate. Thus the decimation factor should be 24. The AD6620 can perform one complex multiply for each clock cycle supplied. However, if a clock is provided that is a multiple of the data rate, more multiplies and hence more taps can be performed on the data set. To facilitate this feature of the AD6620, the AD6600 has a 2×-clock output. This clock can be used to double the number taps that the AD6600 can process. Thus, in our primary example of 6.5 MSPS, the 2× clock will allow a FIR filter up to 48 taps to be used.

Such a filter has been designed and the results are shown below. The filter design software provided for the AD6620 determined the impulse response and decimation rate distribution. Decimation was distributed as two in the CIC2, three in the CIC5 and four in the RCF.
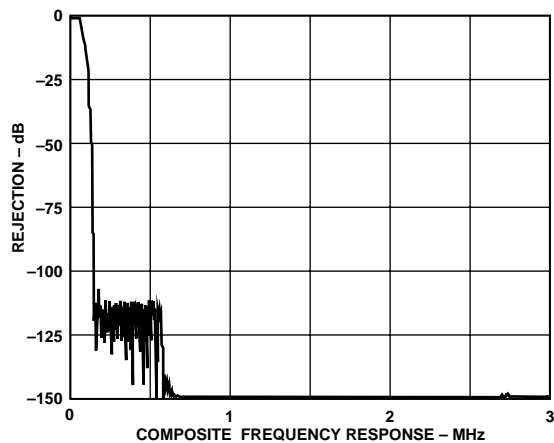

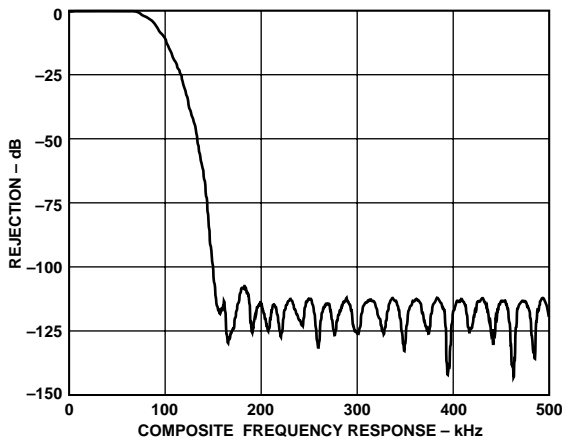Figure 13. Digital Filter Performance, Nyquist View

Figure 14. Digital Filter Performance, Channel View

Measured Receiver Performance

The receiver described here was assembled and the digital filter programmed as designed above. Data was then taken on the various parameters of the IF sub-circuit, the most critical and unique to this implementation. The results are shown here.

The first critical point of the IF is that of the SAW filters and their ability to reject off channel signals to a degree that will prevent the gain ranging from being disrupted. It was very quickly shown that SAW filters do not provide much rejection for signals at 2 GHz (typical high side local oscillator for a PCS basestation) when operated in the singled-ended mode. This is due to the capacitive coupling between the input and output transducers. However, this coupling is approximately common mode between the two output terminals. Therefore, taken differentially, the 2 GHz can be completely rejected. In addition to the local oscillator, this improves rejection of the reverse traffic that is usually generated in close proximity to the sensitive receiver circuit as well as any other strong RF fields that may enter the receiver intended or otherwise.

Run differentially, the dual SAW filters do indeed provide the pass band and stop band performance required as shown below in Figure 15.
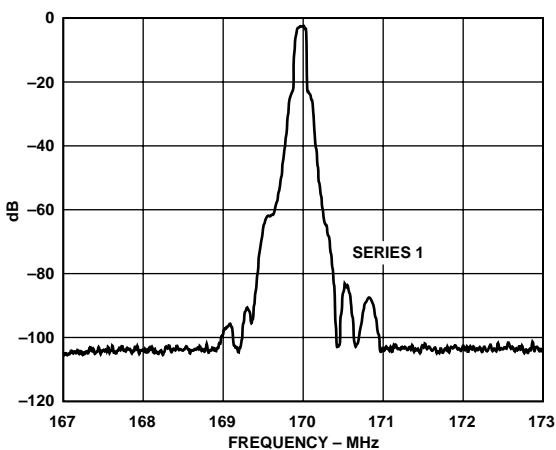

Figure 15. IF Frequency Response (In Band)

In this pass band performance shown, adequate attenuation is provided to prevent the RSSI from disruption from blockers and jammers are required in the GSM specification. Also, sufficient rejection is achieved to prevent aliasing of signals as they fold within the ADC.

Outside the passband, rejection continues to be flat. As shown in Figure 16, rejection from the high side of the IF out to 2 GHz continues to be flat at about –105 dBFS.

Finally, adding the performance of the digital filter to the analog filter provides the following performance. As seen in Figure 17, additional pass band shaping results as well as even more stop band rejection. The graph here has the three images superimposed. The first is the
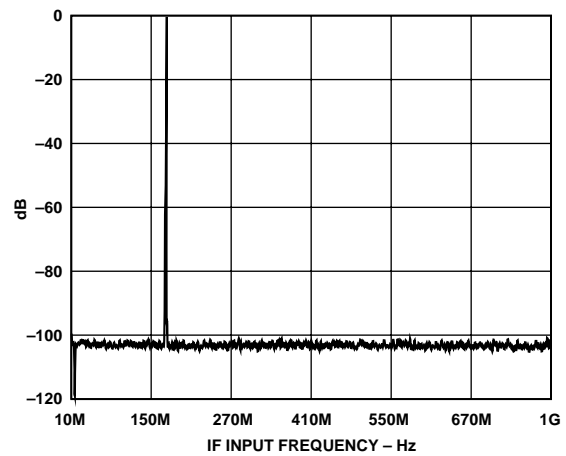

Figure 16. IF Frequency Response, 10 MHz to 1 GHz

basic dual SAW filter performance. The second is the combined SAW performance and digital filtering and the third is the required GSM masking required for the AD6600 and AD6620 to properly operate. As seen there is plenty of margin for all frequencies. Additionally, digital filtering provides additional margin in off channel rejection, which now provides over 130 dB rejection.
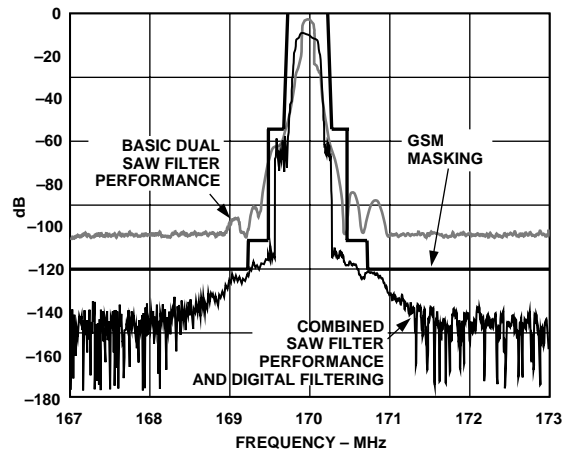

Figure 17. SAW Performance, Combined Performance and GSM Requirements

GSM 05.05 Blocker and Interferer Testing

Testing the receiver against the GSM specifications makes a more critical review of the receiver design. The critical specifications are the blocker and interferer tests, which provide multitone in-band requirements. These tests are outlined below in the tables. Since our receiver consists only of the IF filters and clamp amplifier, the test signals were injected at a level as would be found on the output of the mixer.

Table III.

Interferer Frequency Offset	C/I Level
0	*9 dBc*
±200 kHz	*−9 dBc*
±400 kHz	*−41 dBc*
±600 kHz	*−49 dBc*

Shown in Table III are the carrier to interferer levels as specified by GSM. The zero offset frequency (co-channel) interferer is a function of the equalizer performance and thus not discussed in this report. However, all other frequencies are of interest and will be tested. The plots below show the receiver performance to the ADC output for the 200 kHz, 400 kHz and 600 kHz interferer specs.
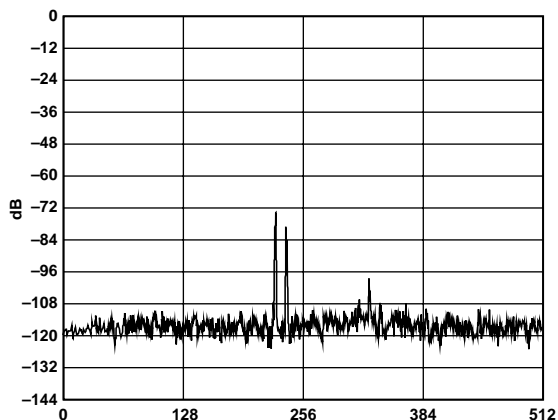

Figure 18. 200 kHz Interferer

In the 200 kHz blocker test above, the 200 kHz signal has been rejected to 6 dBc by the SAW filters. Before equalization, this signal is to be passed to the digital filter (AD6620) where the spectrum will be filtered. At 200 kHz offset, our digital filter should have at least 70 dB of rejection. Thus after filtering, the spurious will be about −76 dBc and the SNR in the channel of interest will be 32.3 dB, more than enough for a low bit error rate.
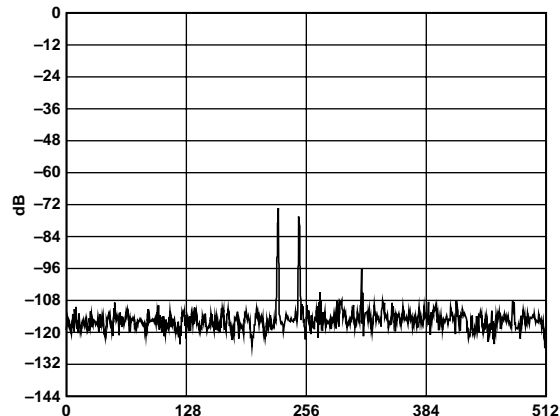

Figure 19. 400 kHz Interferer

Rejection at 400 kHz is very similar to that of 200 kHz. As before, the digital filtering provides additional rejection. By 400 kHz offset, the filter performance has reached the maximum rejection of just greater than 100 dB. Thus after filtering the spurious is again gone and the in-band SNR is still about 32 dB.
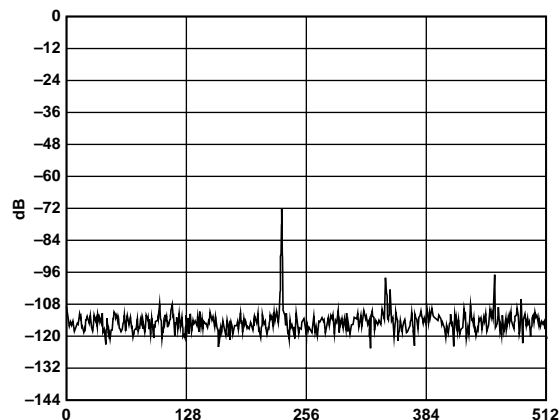

Figure 20. 600 kHz Interferer

The final interferer test is at 600 kHz. By 600 kHz, the SAW filters have begun rejecting the signal and all that remains are various spurious signals. It should be noted that none of the spurs in the above plot are 600 kHz. As with the 400 kHz offset test, the digital filter provides another 100 dB of rejection and the spurious products are all removed leaving an in-band SNR of 30 dB.

Table IV.

Blocker	C/I Level
600 kHz ≤ Offset < 800 kHz	*−26 dBm Signal Level*
800 kHz ≤ Offset < 1.6 MHz	*−16 dBm Signal Level*
1.6 MHz ≤ Offset < 3 MHz	*−16 dBm Signal Level*
>3 MHz	*−13 dBm Signal Level*

The blocking requirements are shown in Table IV. Again, the inputs to the IF filters were driven as if they had been processed by a proper front end, but the signal levels were representative of the blocking specification. Since blocking performance should be worse on the low frequency edge, the blocking tests were performed at the lower frequency corner.
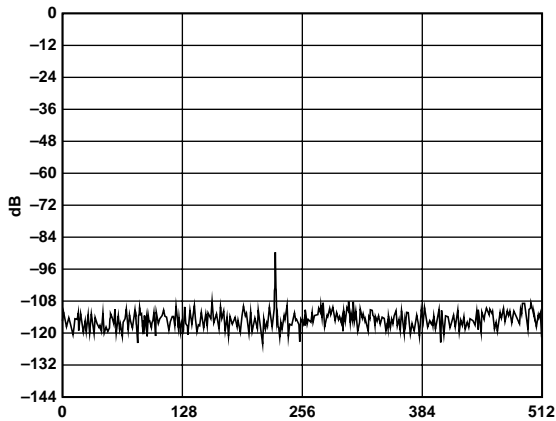

Figure 21. 600 kHz Blocker

As can be seen, only the desired carrier is present, the 600 kHz blocker is suppressed into the noise floor. As before, digital filtering will then remove excess noise and provide an SNR of 15 dB. Since this test is performed 3 dB above minimum sensitivity, this test defines what the minimum sensitivity for the receiver. Under these conditions, the reference sensitivity is –104 dBm, giving an SNR of 12 dB. Most equalizers will function adequately with 10 dB of SNR. Therefore providing a total sensitivity for the receiver of about –106 dBm.
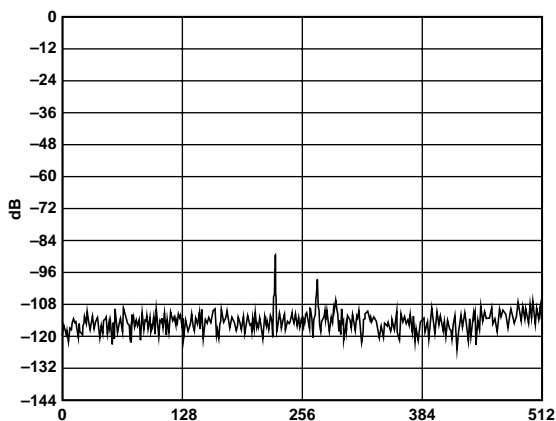

Figure 22. 800 kHz Blocker

At 800 kHz, an image appears, but is again suppressed with digital filtering. As before, SNR is about 15 dB, which gives an overall sensitivity of –106 dBm.
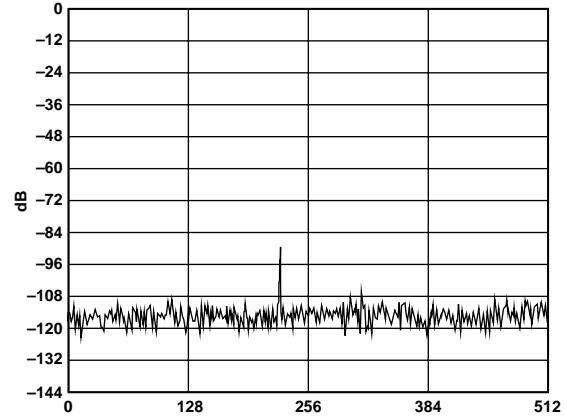

Figure 23. 1600 kHz Blocker

The final two plots are for the 1600 kHz and 3000 kHz offset blocker. As seen, the SNR is consistent at 15 dB and spurious rejection complete. Thus inclusion, the interferer and blocker test should pose no problem to a receiver implemented with the AD6600 and AD6620 Diversity Chipset.
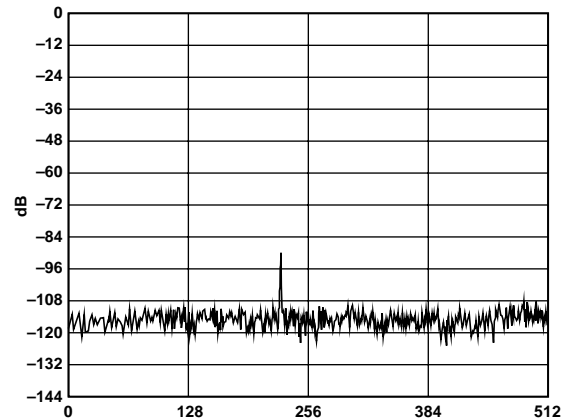

Figure 24. 3 MHz Blocker

GSM Receiver Summary

In summary, the AD6600 can make a very effective IF sampling receiver, eliminating many of the passive and active components associated with multiple down conversion receivers. Based on the analog receiver design required, it is quite feasible to produce a receiver with the required sensitivity as well. In fact, components exist that readily fill the requirements. These include RF amps, RF mixers, SAW filters, and now ADCs and digital drop receivers. Continued development of GaAs amplifiers and mixers will continue to improve receiver performance. The continuing move to differential components such as amplifiers and mixers will also tend to increase the performance of these systems. This will reduce the common-mode problems within the receiver design such as LO coupling and RF bleed through.