ANALOG DEVICES

LC²MOS Baseband I/O Converter

Preliminary Technical Data — AD7005

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GENERAL DESCRIPTION

The AD7005 is a complete low power, two-channel, input/output port with signal conditioning. The device is utilised as a baseband digitisation sub-system performing signal conversion between the DSP and the IF/RF sections in the American Digital Cellular telephone system.

The transmit path contains two high accuracy, fast DACs with output reconstruction filters. The receive path is composed of two high performance delta sigma ADCs with digital filtering. A common bandgap reference feeds the ADCs and signal DACs.

Three control DACs (AUX 1 to AUX 3) are included for such functions as AFC, AGC and Transmit Power Control.

As it is a necessity for all mobile systems to use the lowest power possible, the device has power-down or sleep options. Each of the three digital channels has an independent power-down control.

All the device control logic is contained on-chip.

The AD7005 is housed in 44-pin PQFP.

FEATURES

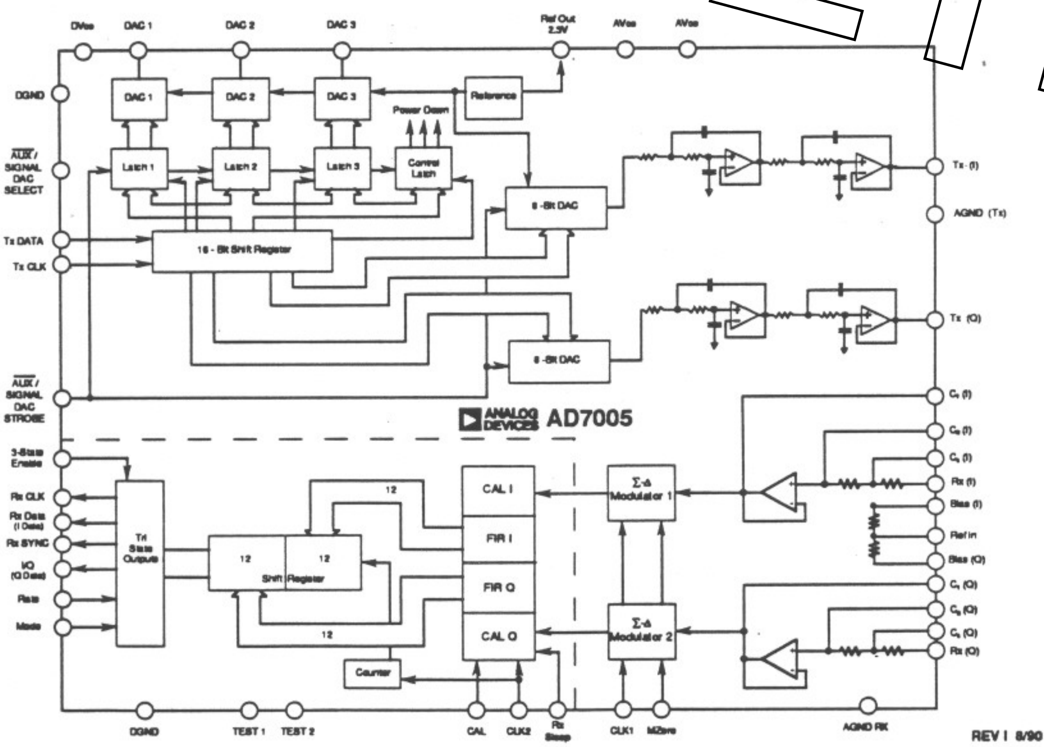
Single +5V Supply
2 Channel Delta Sigma ADC
- -2.33MHz Sampling Rate
- -Simultaneous Sampling
- - Digital Filter (20KHz Bandwidth)

2 Channel 8-Bit D/A Converters
- -800KHz Update Rate
- -Simultaneous Update
- - 4th Order Bessel Low-pass Filters

3 Auxilary D/A Converters
Fast Interface Port
Power Down Modes
On-Chip Voltage Reference
44-Pin PQFP

APPLICATIONS

Digital Cellular Telephony
Private Mobile Telephony
Signal Generation/Acquisition
FSK, PSK Demodulation



Functional Block Diagram

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SPECIFICATIONS[1]

(AV_{DD} = +5V ± 5%; DV_{DD} = +5V ± 5%; AGND Tx = AGND Rx = DGND = 0V, $f_{CLK1} = f_{CLK2}$ = 2.33MHz, V_{REF} = 2.3V; $T_A = T_{MIN}$ to T_{MAX}, unless otherwise stated)

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Parameter	AD7005J	Units	Test Conditions/Comments
ADC SPECIFICATIONS			
Resolution	12	Bits	
Signal Input Span	±1.15	Volts	Biased on V_{REF} (2.3V).
Sampling Rate	2.33	MHz	
Output Rate	48.6/97.2	kHz	
Accuracy			
Integral	1	LSB	
Differential	0[2]		
Bias Offset Error @ 25°C	±10	LSB	Prior to calibration
T_{MIN} to T_{MAX}	±12	LSB	
Input Resistance (dc)	100	kΩ min	
Input Capacitance	20	pF max	
Dynamic Specifications			
Dynamic Range	64	dB min	
Signal to (Noise+Distortion)	62	dB min	
Gain Match Between Channels	±0.1	dB max	Input frequency = 12.15kHz
Frequency Response			
0 - 17kHz	±0.1	dB max	
19kHz	-0.8	dB max	
21kHz	-2.5	dB max	
35kHz	-66	dB max	
>97.6kHz	-72	dB max	
Group Delay Between Channels (0 - 21kHz)	5	ns typ	
Group Delay Linearity (0 - 21kHz)	5	ns typ	
Power Down Option	Yes		Independent of Transmit
TRANSMIT DAC SPECIFICATIONS			
Resolution	8	Bits	
No. of Channels	2		
DC Accuracy			
Integral	±1	LSB max	
Differential	±1	LSB max	Guaranteed Monotonic
Output Signal Span	1.15	Volts	Centred on 2.3V nominal (10kΩ/100pF load)
Output Signal Full-Scale Accuracy	±1	dB typ	
Offset Error	±25	mV max	10 000 000 loaded to DAC
Gain Matching between Channels	±0.1	dB max	
Delay Matching between I and Q Channels[3]	500	ns max	
Power Down Option	Yes		Independent of Receive
Update Rate	194.4	Ks/s	4X Over Sampling
Transmit Filter Frequency Response			
Attenuation at 19.4kHz	<3	dB	
97.2kHz	>18	dB	
194.4kHz	>46	dB	
Spurious Output Spectra	<50	dBc	When producing a sine wave of 12.15kHz on output with receive side inactive and over the frequency band 0 to 2.33MHz

AUXILLIARY DAC SPECIFICATIONS	AUX1	AUX 2	AUX 3	Units	Test Conditions/Comments
Resolution	9	10	8	Bits	
DC Accuracy					
Integral	±4	±4	±2	LSB max	
Differential	±1	±1	±1	LSB max	Guaranteed Monotonic
Offset Error	±2	±2	±1	LSB max	
Gain Error	±4	±4	±2	LSB max	
Output Signal Span	0 to V_{REF}	0 to V_{REF}	0 to V_{REF}	Volts	Unloaded output
Output Impedance	10	10	10	kΩ max	AUX DAC's have unbuffered resistive outputs.
Coding	Binary	Binary	Binary		
Power Down	Yes	Yes	Yes		Independent of Signal DACs

LOGIC INPUTS			
V_{INH}, Input High Voltage	3.15	V min	
V_{INL}, Input Low Voltage	0.9	V max	
I_{INH}, Input Current	10	µA max	
C_{IN}, Input Capacitance	10	pF max	
LOGIC OUTPUTS			
V_{OH}, Output High Voltage	4.0	V min	$\lvert I_{OUT} \rvert \leq 40\mu A$
V_{OL}, Output Low Voltage	0.4	V max	$\lvert I_{OUT} \rvert \leq 1.6mA$
POWER SUPPLIES			
Reference Output	2.2/2.4	Vmin/Vmax	
AV_{DD}	4.75/5.25	Vmin/Vmax	
DV_{DD}	4.75/5.25	Vmin/Vmax	
I_{DD}(Total)	21	mA max	
ADC and Auxilliary Paths Active	10	mA max	
Transmit DAC and Aux Paths Active	12	mA max	
Auxilliary Path only Active	0.5	mA max	

NOTES
1. Operating Temperature Ranges as follows : A Versions : -40°C to +85°C.
2. Unmeasurable : Sigma Delta conversion is inherently free of Differential Nonlinearities.
3. Defined as the delay between Vref transition on the I and Q output as each DAC is stepped from 1/3 to 2/3 full scale.

Specifications subject to change without notice.

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ABSOLUTE MAXIMUM RATINGS[1]
(T_A = +25°C unless otherwise noted)

DV_{DD} to AGND .... -0.3V to +6V
AV_{DD} to AGND .... -0.3V to +6V
AGND to DGND .... -0.3V to +0.3V
Digital Input Voltage to DGND .... -0.3V to DV_{DD} + 0.3V
Analog Input Voltage to AGND .... - 0.3V to AV_{DD} + 0.3V
Input Current to any Pin except Supplies[2] .... ±10 mA
Operating Temperature Range
Commercial Plastic (A,B Versions) .... -40°C to +85°C
Storage Temperature Range .... -65°C to +150°C
Lead Temperature (Soldering, 10 secs) .... +300°C
Power Dissipation (Any Package) to +75°C 450mW
Derates above +75°C by .... 10mW/°C

NOTES
1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION :
ESD (Electro-Static Discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subjected to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam shoud be discharged to the destination socket before devices are removed.

WARNING!
ESD SENSITIVE DEVICE

PIN CONFIGURATION

INPUT CLOCK TIMING SPECIFICATIONS[1]

(AV_{DD} = +5V ± 5%; DV_{DD} = +5V ± 5%; AGND Tx = AGND Rx = DGND = 0V, V_{REF} = 2.3V; T_A = T_{MIN} to T_{MAX}, unless otherwise stated)

Parameter	Limit at T_A = 25°C	Limit at T_A = -40°C to +85°C	Units	Description
t_1	300	300	ns min	CLK1, CLK2, AUXCLK Cycle Time
t_2	100	100	ns min	CLK1, CLK2, AUXCLK High Time
t_3	100	100	ns min	CLK1, CLK2, AUXCLK Low Time

NOTES

[1] Sample tested at 25°C to ensure compliance. All input signals are specified with tr = tf = 5ns (10% to 90% of 5V) and timed from a voltage level of 1.6V.

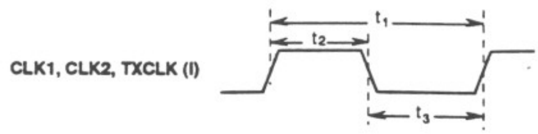

Figure 1. Clock Timing

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AUX/SIGNAL DAC TIMING

(V_{DD} Tx = V_{DD} Rx = +5V ± 10%; Test = AGND Tx = AGND Rx = DGND Tx = DGND Rx = 0V; unless otherwise stated)

Parameter	Limit at T_A = 25°C	Limit at T_A = -25°C to +85°C	Units	Description
t_4	100	100	ns min	TX CLOCK Low Duration
t_5	100	100	ns min	TX CLOCK High Duration
t_6	40	40	ns min	TX DATA to TX CLOCK Setup Time
t_7	50	50	ns min	TX DATA to TX CLOCK Hold Time
t_8	50	50	ns min	STROBE to TX CLOCK Setup Time
t_9	40	40	ns min	STROBE to TX CLOCK Hold Time
t_{10}	16 (t_4 + t_5)	16 (t_4 + t_5)	ns min	STROBE Duration

NOTES

[1] All input signal rise and fall times measured from 10% to 90% of +5V. $t_r = t_f$ = 20ns.

[2] Timing measurement reference level is $(V_{IH} + V_{IL})/2$.

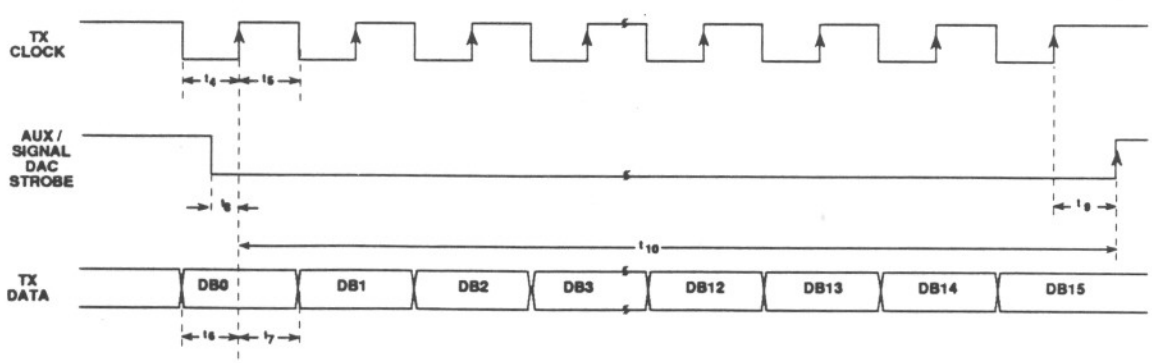

Figure 2. Aux/Signal DAC Timing Diagram

RECEIVE SECTION TIMING (AV_{DD} = +5V ± 5%; DV_{DD} = +5V ± 5%; AGND Tx = AGND Rx = DGND = 0V, f_{CLK1} = f_{CLK2} = 2.33MHz, V_{REF} = 2.3V; T_A = T_{MIN} to T_{MAX}, unless otherwise stated)

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Parameter	Limit at T_A = 25°C	Limit at T_A = -40°C to +85°C	Units	Description
t_{22}	0	0	ns min	RxSLEEP Hold Time After CLK1, CLK2 High
t_{23}	25	25	ns min	RxSLEEP Setup Time Before CLK1, CLK2 High
t_{24}	0	0	ns	RxSLEEP Hold Time After Q LSB
t_{25}	$8t_1$	$8t_1$	ns	RxSLEEP Setup Time Before Q LSB
t_{26}	$50t_1$	$50t_1$	ns	RxCLK Active After CLK1 Rising Edge
t_{27}	t_1	t_1	ns	RxCLK Cycle Time, Mode 0
t_{28}	30	30	ns min	RxCLK Low Pulse Width, Mode 0
t_{29}	30	30	ns min	RxCLK High Pulse Width, Mode 0
t_{30}	15	15	ns max	Propagation Delay from CLK1, CLK2 High to RxCLK High
t_{31}	15	15	ns max	RxSYNC High After CLK1, CLK2 Rising Edge
t_{32}	t_1	t_1	ns	RxSYNC High Pulse Width, Mode 0
t_{33}	$12t_1$	$12t_1$	ns	RxSYNC Cycle Time (Mode 0, decimate by 12)
t_{34}	15	15	ns min	RxDATA Valid After RxCLK Rising Edge
t_{35}	15	15	ns max	Propagation Delay from CLK1,CLK2 Rising Edge to I/Q
t_{36}	$24t_1$	$24t_1$	ns	RxSYNC Cycle Time (Mode 0, decimate by 24)
t_{37}	$2t_1$	$2t_1$	ns	RxCLK Cycle Time, Mode 1
t_{38}	30	30	ns min	RxCLK Low Pulse Width, Mode 1
t_{39}	90	90	ns min	RxCLK High Pulse Width, Mode 1
t_{40}	$2t_1$	$2t_1$	ns	RxSYNC High Pulse Width, Mode 1
t_{41}	$24t_1$	$24t_1$	ns	RxSYNC Cycle Time (Mode 1, decimate by 12)
t_{42}	$48t_1$	$48t_1$	ns	RxSYNC Cycle Time (Mode 1, decimate by 24)
t_{43}	10	10	ns max	Digital Output Rise Time
t_{44}	10	10	ns max	Digital Output Fall Time

NOTES

[1] Sample tested at 25°C to ensure compliance. All input signals are specified with tr = tf = 5ns (10% to 90% of 5V) and timed from a voltage level of 1.6V.

[2] Digital output rise and fall times specify the time required for the output to go between 10% and 90% of 5V.

[3] See Figure 8 for Test Circuit.

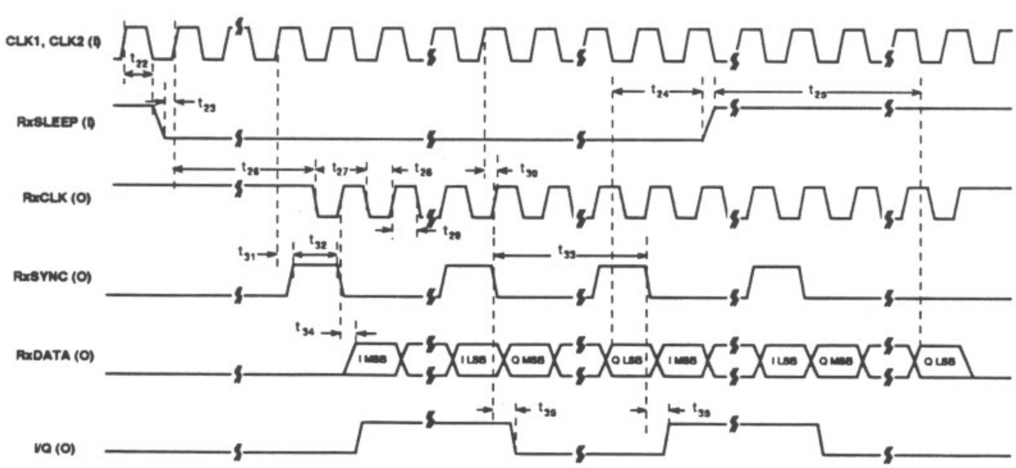

Figure 4. Mode 0 Receive Timing (Decimate by 12)

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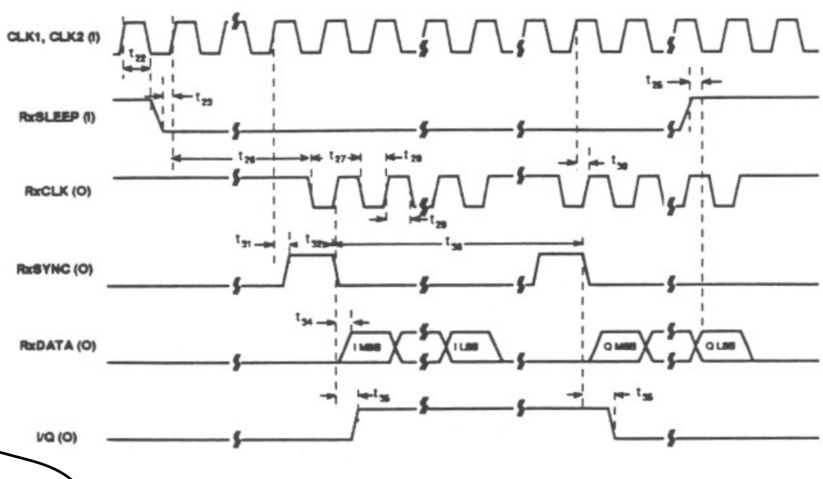

Figure 5. Mode 0 Receive Timing (Decimate by 24)

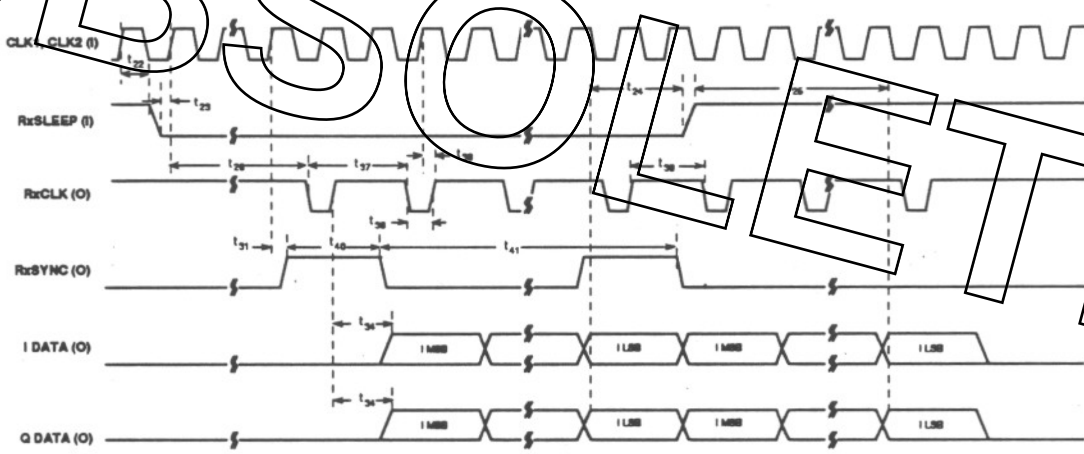

Figure 6. Mode 1 Receive Timing (Decimate by 12)

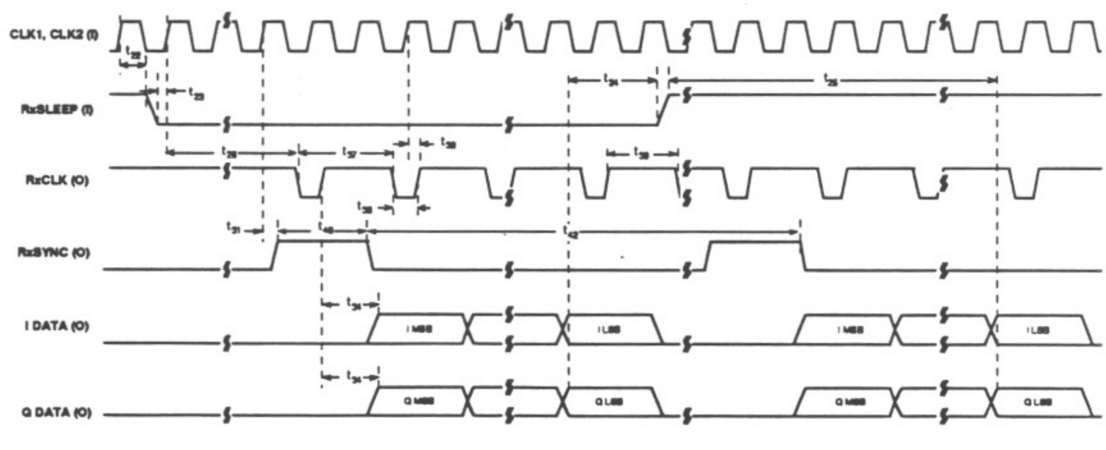

Figure 7. Mode 1 Receive Timing (Decimate by 24)