ANALOG DEVICES

Picoampere Input Current Bipolar Op Amp

AD705

1.1 Scope.

This specification covers the detail requirements for a precision, low input current, low offset voltage, monolithic bipolar amplifier.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
−1	AD705T/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
Q	Q-8	8-Pin Cerdip Package

1.3 Absolute Maximum Ratings. (T_A = +25°C unless otherwise noted)

Supply Voltage . . . . . ±18 V
Internal Power Dissipation[1] . . . . . 650 mW
Input Voltage . . . . . $\pm V_S$
Differential Input Voltage[2] . . . . . ±0.7 V
Output Short Circuit Duration . . . . . Indefinite
Storage Temperature Range . . . . . −65°C to+150°C
Operating Temperature Range . . . . . −55°C to +125°C
Lead Temperature Range (Soldering 60 sec) . . . . . +300°C

NOTES

[1]Maximum package power dissipation vs. ambient temperature.

Package Type	MAXIMUM AMBIENT Temperature for Rating	DERATE ABOVE MAXIMUM Ambient Temperature
Q-8	75°C	6.7 mW/°C

[2]The Input pins of this amplifier are protected by back-to-back diodes. If the differential voltage exceeds ±0.7 V, external series protection resistors should be added to limit the input current to less than 25 mA.

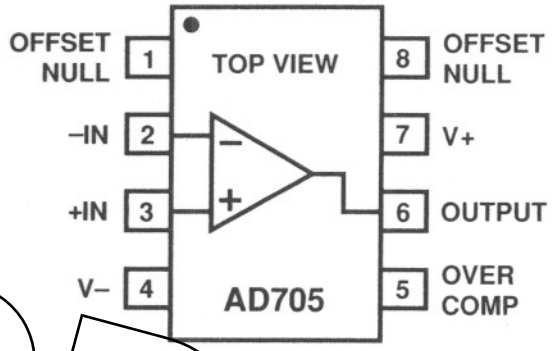
AD705 – SPECIFICATIONS

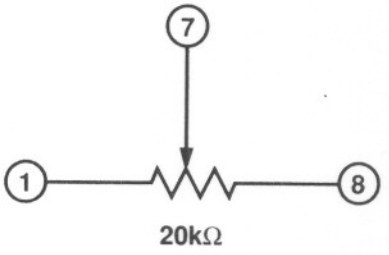
Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition[1]	Units
Input Offset Voltage[2]	V_{OS}	−1	25	90	60	25		±μV
Input Offset Voltage Drift	TCV_{OS}	−1	0.6		0.6			±μV/°C
Power Supply Rejection Ratio	PSRR	−1	114	114	 108		±2 V≤V_S≤±18 V ±2.5 V≤V_S≤±18 V	±dB
Input Bias Current[3]	I_B	−1	100 150	150 200	250 450	100 150	Either Input, V_{CM} = 0 V Either Input, V_{CM} = ±13.5 V	±pA
Input Offset Current	I_{OS}	−1	100 150	150 200	250 450	100 150	V_{CM} = 0 V V_{CM} = ±13.5 V	±pA
Unity Gain Crossover Frequency	F_U	−1	0.4					MHz
Slew Rate	I_{SR}	−1	0.1					V/μs
Common Mode Rejection Ratio	CMRR	−1	114	114	108		V_{CM} = ±13.5 V	dB
Open Loop Gain	A_{OL}	−1	400 300	400 300	300 200		V_O=±12 V, R_L = 10 kΩ V_O=±10 V, R_L = 2 kΩ	V/mV
Output Voltage Swing	V_{OUT}	−1	±13	±13	±13		R_L = 10 kΩ	V
Power Supply Quiescent Current	I_Q	−1	600	600	800			μA
Input Noise Voltage	e_N	−1	1				0.1 to 10 Hz, p-p max	μV

NOTES
[1]V_S = ±15 V unless otherwise noted.
[2]Input offset voltage specifications are guaranteed with V_{OS} unnulled at T_A = +25°C.
[3]Bias current specifications guaranteed maximum at either input.

3.2.1 Functional Block Diagram and Terminal Assignments.

8-Pin Cerdip (Q-8) Package





V_{OS} TRIM

3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (49).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).