AD7124-4 and AD7124-8
Frequently Asked Questions (FAQs)

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Q1. The AD7124-4 and AD7124-8 have 3 power modes which one should I used?

The end application will dictate the power mode to use.

Common applications for the part are smart transmitters, process control input modules and low power or battery operated instrumentation.

For Field transmitter applications, the maximum current that can be used by the complete transmitter is 4 mA when the transmitter is loop powered. Therefore, the less current consumed by the ADC, the better, as it allows more current for the processor, and other components in the design. Therefore, the AD7124-4/AD7124-8 for this application would be used in low power mode.

For process control, current consumption is not a concern so any power mode could be used. The benefits of using the full power mode for this application is that for a given output data rate, the rms noise is lowest in the full power mode. Also, the part supports higher output data rates in the full power mode. This enables the customer to increase the number of channels sampled per second for a given level of performance.

Q2. What are the differences between the standard AD712-4/8 and the B-grade?

There are a number of key differences between the standard parts and the B-grade parts, and the choice of part for your application will depend on your requirements. The key differences are

- Package
- Internal Reference TempCo Specification
- Multichannel Measurement (channel sequencing) settling time (at Gain=1)
- Excitation currents status/mode in standby mode
- Gain Registers value when MCLK & SCLK are Asynchronous

B-Grade v's Standard Package:

The B-grade is available in the LFCSP package only whereas the standard is available in both TSSOP and LFCSP. The LFCSP package is 5 x 5 mm package for both B-grade and standard however the height is the key difference, the B-grade height is 0.95 mm and the standard is 0.75mm.

B-Grade v's Standard Internal Reference TempCo:

The B-grade AD7124-4/8 internal reference has a tempco of 10 ppm/'C max, whereas the standard silicon (LFCSP) has a temp co of 15 ppm/'C max

B-Grade v's Standard Multichannel settling time (at G=1):

The B-grade silicon includes a pre-charge buffer which aids the settling and hence ensures that all conversions are fully settled within the allowed time.

The standard silicon, when used in multi-channel mode, does not settle within the allowed time when switching channels for gains of 1 when high output data rates are used in conjunction with large resistive loads.

B-Grade v's Standard Excitation currents status in standby mode:

The excitation currents on the B-Grade can remain active in standby mode. This is useful when current consumption minimization is not important. On the standard silicon (LFCSP and TSSOP), the excitation currents are disabled when the ADC is placed in standby mode.

Some customers use single conversion mode as a timing mechanism to provide conversions within timeslots. In this use case, keeping the excitation currents enabled during standby mode minimizes the power up time.

B-Grade v's Standard Gain Registers value when MCLK & SCLK are Asynchronous

On the standard silicon, the gain register can reset to its default value periodically if SCLK and MCLK are asynchronous. So, if internal Full Scale (FS) calibrations or system FS calibrations are performed in a system where SCLK and MCLK are asynchronous, the gain register should be read periodically to ensure that it has not reset.

On the B-grade, the gain register does not reset even when SCLK and MCLK are asynchronous.

Q3. For the AD7124-4/AD7124-8 Is the B-Grade better than the standard?

The B-Grade is better than the standard and should be used for new designs, to understand the key differences see Q2 above.

Q4. How can I tell the difference between the standard and B-grade models for the AD7124-4/AD7124-8?

When ordering there are two options available for each product,

AD7124-4:

- AD7124-4B**B**CPZ
- AD7124-4BCPZ

AD7124-8

- AD7124-8BBCPZ-RL
- AD7124-8BCPZ-RL.

The extra B in the first option for each product represent the B-grade. The B-grade offers substantial improvements over the standard silicon and therefore would be recommended for new design, for full details on the differences Q2 above.

Q5. What are the tradeoffs in performance between the three power modes available on the AD7124-4 / AD7124-8?

There are 3 power modes available on the AD7124-4/AD7124-8, low, mid and full power mode.

In full power mode the analog input signal is sampled at 614.4 kHz. The maximum output data rate is 19.2 kHz. In this mode, the part has lowest rms noise for a given output data rate. It also has low offset drift and best PSR.

In the mid power and low power modes, the master clock is internally reduced by 4 in the mid power mode and 8 in the low power mode. This means that the sampling frequency of the input signal is also reduced by 4 or 8 accordingly, this also leads to the reduction of current consumption to some of the on board analog circuitry. This saving in current consumption offers considerable savings in the overall power budget, however this reduction in current leads to an increase in the rms noise, and also leads to higher offset drift, PSRR.

Q6. What digital filters are available on the AD7124-4/AD7124-8?

There are many digital filters available on the AD7124-4/AD7124-8 these include standard sinc filters, Sinc4, Sinc3 as well as Sinc4+Avgeraging and Sinc3 plus average, as well as post filters that offer simultaneous 50Hz and 60Hz rejection with reasonable settling time.

Q7 What are the differences and key benefit associated with the post filters over the standard sinc filters available on the AD7124-4 / AD7124-8?

To highlight the key differences we will give an example. Looking at some of the applications where the AD7124-4/AD7124-8 are used and specifically focusing on industrial applications, 50Hz and 60Hz rejection is one of the key requirements. For these applications customers would like to sequence through multiple channels with each channel producing a valid conversion in 20ms. The main challenge here is the difficulty to achieve this timing while attaining good 50/60Hz rejection.

The post filters on the AD7124-4/AD7124-8 offer a compromise between settling time and rejection.

If we look at a standard sinc3 filter this has a settling time of 60ms when operating at 50sps while still offering simultaneous 50Hz and 60Hz rejection. The rejection obtained by this filter is 66dB

There are a number of different options available for the post filters, if we take the 25sps post filter. This filter has a settling time of 40ms and has a rejection of 62dB. The rejection is slightly degraded using the post filter when compared with the sinc3 filter, but the value is acceptable for a lot of the applications, the key difference is around the settling time where the post filters settle much faster than the sinc3 filter.

To see the behaviour of the different filter options understand the trade offs and associated timing please go to our virtual eval online simulation tool, you can find this at the following weblinks

http://beta-tools.analog.com/virtualeval/#tool_pid=AD7124-4&tab=fbd

http://beta-tools.analog.com/virtualeval/#tool_pid=AD7124-8&tab=fbd

Click here to watch a video that uses the Virtual Eval online tool to highlight the filters available.

Q8 Is an IBIS model available for the AD7124-4/AD7124-8?

Yes, the IBIS models are available for the AD7124-4 as well as the AD7124-8. The link to the models can be found on the product pages at the following links

https://www.analog.com/en/products/ad7124-4.html#product-tools
https://www.analog.com/en/products/ad7124-8.html#product-tools

Q9 The AD7124-4/AD7124-8 diagnostics, how or where can these be used?

The AD7124-4/AD7124-8 have been designed with a high degree of on board diagnostics. The diagnostics enable a guaranteed and trusted result. Diagnostics are available from the input right to the digital interface and can be enabled/disabled through specified registers in the register map. These diagnostics can be not just used for functional safety type applications but can also be used to give a level of confidence that the measurement solution is working as expected.

Q10. What level of diagnostics are available on the AD7124-4/AD7124-8?

The on-chip diagnostics allow the user to verify the circuit connections ensuring that the input signal is still connected as well as carrying out checks on the internal blocks of the chip as the PGA, reference and ADC itself can be monitored. A key benefit is that all the on-chip registers can be monitored, and thus gives the user confidence that no register changes have occurred. The AD7124-4/AD7124-8 also incorporates a high number of diagnostics around the serial interface which include read/write checks, a full list of diagnostics can be found in the datasheet. We also have a video that discusses each of the available diagnostics in detail and this can be found here

Q11. On the AD7124-4/AD7124-8 Is the serial interface reset when CS is taken high?

Yes. Each time that CS is taken high, the serial interface is reset. When CS is taken low, the serial interface is in a state where it expects a write to the communications register, indicating the next operation. This feature is useful as it allows the user to reset the serial interface.

When reading or writing to the AD7124-8, a user can transmit the data as a continuous stream or the data can be split into bytes. For example, if writing 24 bits to the ADC, all 24 bits can be transmitted continuously or the data can be divided into 8-bit

words. However, if the data is divided into bytes, CS must be held low until all bytes are transmitted.

Q12. When single conversion mode is used, can CS be taken high after the single conversion is initiated?

The serial interface is independent of the sampling process. So, once the single conversion is initiated, the AD7124-8 will power up and perform the single conversion irrespective of the $\overline{CS}$ polarity. So, the user can take $\overline{CS}$ low, initiate the single conversion and then take $\overline{CS}$ high again. When the conversion is complete, $\overline{CS}$ can be taken low to read the conversion and another single conversion can be started if required.

When $\overline{CS}$ is taken high, the DOUT/$\overline{RDY}$ pin is tri-stated. Therefore, the DOUT/$\overline{RDY}$ pin will not indicate the end of the conversion. The user can determine the end of the conversion by reading the status register. Alternatively, the conversion time could be timed out by the microcontroller clock.

Q13. What is the ESD rating of the AD7124-8?

HBM Model Pass Level: 4.0 kV, FICDM Model Pass Level: 1250 V, Machine Model Pass Level: 400 V

Q14. Should an anti-alias filter be used with the AD7124-4/AD7124-8?

Yes, an anti-alias filter is required. However, because the AD7124-4/AD7124-8 is a sigma delta ADC, this means that the ADC oversamples the analog input, thus greatly simplifying the design of the anti-alias filter when compared to an ADC that samples at the Nyquist rate (Maximum signal Bandwidth * 2).

The AD7124-4 / AD7124-8 also incorporates a digital filter, where the associated frequency response is reflected around the sampling frequency of the ADC. This means that the filter will provide 0dB of attenuation at frequencies which are integer multiples of the ADC sampling frequency. Thus the purpose of the an anti-alias filter is required to provide adequate rejection at multiples of the ADC sampling frequency. The anti alias filter is usually a single pole (possibly a 2 pole) RC filter is all that is required. An example of an anti filter for the AD7124-4/AD7124-8 would be a 1KΩ resistor in series with each analog input, a 0.1µF capacitor from AINP to AINM, and a 0.01 µF capacitor from each analog input pin to AVSS. These R and C values are recommended when the analog input channel is buffered.
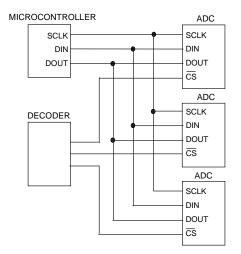
When the converter is operated in unbuffered mode (gain = 1), the inputs look directly into the sampling capacitor of the modulator. The modulator is continually charging and discharging the sampling capacitor. If the time constant of the anti-aliasing filter is too large, the modulator may be unable to fully charge the sampling capacitor and gain errors will result. To prevent the R-C combination from introducing errors, the R and C values used must be limited.

Q15. How do I interface to multiple AD7124-4/AD7124-8 ADCs over the same serial interface?

A single microcontroller can be used to communicate with several AD7124-4/AD7124-8 devices. The $\overline{CS}$ input of the ADC can be used to enable or disable the serial interface to the associated ADC. By controlling the $\overline{CS}$ inputs to the ADCs using a decoder, the microcontroller can communicate with each ADC individually or simultaneously.

The figure below shows the interface between a microprocessor and several ADCs. The $\overline{CS}$ input of each ADC is connected to the decoder. Using the decoder, the microprocessor can select the ADC with which it wants to transfer data/instructions. When $\overline{CS}$ is high, the serial interface of the ADC is disabled and it ignores any activity on the data bus. To communicate with the ADC, its $\overline{CS}$ line can be taken low. The ADC will then have access to the data bus between itself and the microprocessor. The datasheet should be consulted for timing specifications.

Q16. What is the data output coding used on the AD7124-4/AD7124-8?

On the AD124-4 & AD7124-8 two different coding options exist unipolar and bipolar coding. Unipolar coding is used to represent positive voltages only, and bipolar coding can be used to represent both negative and positive differential voltages applied to the analog inputs of the ADC.

For the ADC operating in unipolar mode, the input range to the ADC is from 0V to Full scale, where the full scale value is equal to VREF/Gain (reference input voltage/ selected PGA gain). The output coding is straight binary which means that

- a zero differential input voltage applied to the analog inputs results in an output code of 00...00 (0x000000)
- a midscale voltage ((Vref/gain)/2) applied to the analog inputs results in an output code of 100...000 (0x800000)
- a full-scale input voltage (Vref/gain) results in an output code of 111...111. (0xFFFFFF)

When the ADC is operated In bipolar mode, the input range is from negative Full Scale to positive Full Scale where Full Scale is VREF/Gain (reference input voltage/selected PGA gain). The output coding for bipolar operation is offset binary with

- a negative full-scale voltage applied to the analog inputs results in an output code of 00...00 (0x000000)
- a zero differential input voltage applied to the analog inputs results in an output of 100...000 (0x800000)
- a positive full-scale input voltage applied to the analog inputs results in an output code of 111...111 (0xFFFFFF)

Q17. How to convert the AD7124-4/AD7124-8 data output Code to equivalent analog input voltage?

As discussed in Q16 above, the ADCs operate in unipolar or bipolar coding modes.

When **unipolar mode** is selected the ADC output code for any analog input voltage applied to the analog inputs can be calculated using the following formula as:

$$Code = (2^N \times AIN \times Gain)/VREF$$

- where AIN is the applied differential input voltage
- VREF is the reference applied to the ADC.
- N = 24 (number of data output bits)

- Gain is the PGA settings

Working through an example where:

AIN = 1V, VREF=2.5V, PGA = 1.

The equivalent code in unipolar mode is

Code = (2^N × AIN xGain)/VREF = (2^24 x 1V x 1)/2.5V = 6710886

When **bipolar mode** is selected the ADC output code for any analog input voltage applied to the analog inputs can be calculated using the following formula as:

Code = 2^ (N – 1) × [(AIN x Gain/VREF) + 1]

- where AIN is the applied differential input voltage
- VREF is the reference applied to the ADC.
- N = 24 (number of data output bits)
- Gain is the PGA settings

Working through an example where:
AIN = 1V, VREF=2.5V, PGA=1. The equivalent code in bipolar mode is

Code = 2^ (N – 1) × [(AIN/VREF) + 1] = 2^ (24 – 1) × [(1V x 1/2.5V) + 1] = 11744051

Q18. How are the offset and gain coefficients applied to the data conversion of AD7124-4/AD7124-8?

The following equations show the calculations associated with the offset and gain for both unipolar and bipolar modes of operation. Note that the AD7124 ADC does all this processing internally, therefore the main conversion of codes to associated voltages can be found described in Q17.

Unipolar Mode:

Data = [(0.75 × VIN x Gain/VREF) × (2^23) – (Offset_Reg – 0x800000)] × Gain_Reg/0x400000 × 2;

Bipolar Mode:

Data = [(0.75 × VIN x Gain/VREF) × (2^23) – (Offset_Reg – 0x800000)]× Gain_Reg/0x400000 + 0x800000;

- Where Data = output code conversion
- VIN= applied analog input voltage, AIN
- VREF= reference voltage
- Offset_Reg = value contained in the offset register

- Gain_Reg = value contained in the gain register
- Gain = PGA gain setting

Some additional notes:
The 0.75 number reflects the attenuation of the analog input to 75% before the offset and gain coefficients are applied. This is done to avoid modulator saturation after applying the offset and gain corrections. This number will vary slightly from part to part because of manufacturing tolerances.
The value 0x800000 is the default offset coefficient. In the Offset_Reg each bit is equal to 1LSB.
The additional 0x800000 in the bipolar equation is to implement the offset binary that is used in bipolar mode.
The 0x400000 along with the gain coefficient invert the 0.75 scaling.

Working through an example where we assume there is no offset and no gain correction applied to the ADC output codes, where the offset coefficient of 0x800000 and gain coefficient of 0x555555. The offset correction is 0x800000– 0x800000= 0. The gain coefficient of 0x555555 divided by the fixed value 0x400000 together give a value closer to 1/0.75. So, the attenuation (0.75) is reverted here.

Q19. What is the equation for calculating Internal Temperature Sensor for AD7124-4/AD7124-8 in unipolar mode?

For AD7124-4/AD7124-8 the sensitivity of the internal temperature sensor is 13,584 codes/°C, approximately when Vref = 2.5V. Both unipolar and bipolar coding can be used when reading the internal temperature sensor.

The formula to convert the ADC output code to a temperature when operating in unipolar mode is:

Temp (°C) = (Conversion / (2*13,584)) – 272.5

Example:

ADC is configured in unipolar. The output code of the AD7124 internal temp sensor at ambient temperature is 8082480 this code to a temperature is done as follows

Temp (°C) = (Conversion / (2*13,584)) – 272.5

Substitute Conversion = 8082480,

Temp (°C) = (8082480/ (2*13,584)) – 272.5 = 25°C

For more details please reference the product pages AD7124-4 / AD7124-8 or Engineer Zone