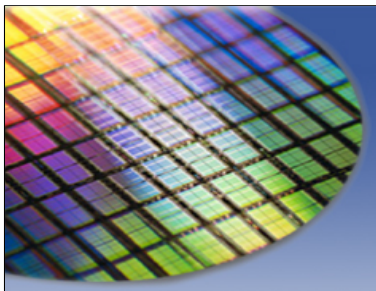
This slide set focuses on the AD719x family of parts.



— AGENDA —

- **Introduction**
- AD719x Features
- Wrap-Up

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AD719x – Overview

4.8 kHz Ultra-Low Noise 24-Bit Σ-Δ ADC with PGA

- **Supports a very wide range of real-world direct sensor input voltage signals (milliVolts to Volts)**
- **Superior noise-free resolution across the widest data-rate and input signal range of *any* Σ-Δ ADC**
- **Offers designers the flexibility to use the same Σ-Δ ADC converter in multiple lines of end equipment**

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The AD719x family uses a low noise, higher speed, high precision core. The aim was to design a family of parts which have ultra low noise. The family can be used in a wide range of applications where the input signals can vary from the milli-volt to volt level. The parts also operate with a wide range of output data rates while still maintaining excellent noise performance over the complete rate of output data ranges.

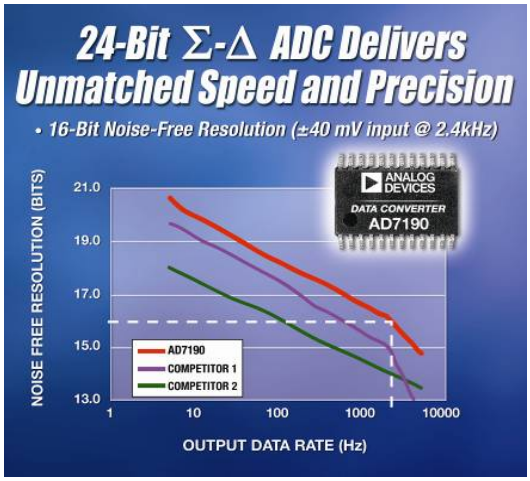
Due to the selection of output data rates, its ability to operate with a wide range of analog input signals and its excellent noise performance over the complete range of input voltages and output data rates, a customer can use the part in multiple applications.

Applications such as high-end weighscales, PLC and chromatography would require this type of performance.

AD7190 – Product Description

4.8 kHz Ultra-Low Noise 24-Bit Σ-Δ ADC with PGA

- **8.5 nV rms Noise**
  - **20.5 bits noise free resolution**
    - Gain = 128, Output Data Rate = 4.7 Hz
  - **22.5 bits noise free resolution**
    - Gain = 1, Output Data Rate = 4.7 Hz
  - **16 bits noise free resolution**
    - Gain = 128, Output Data Rate = 2.4 kHz
- **Output Data Rates up to 4.8 kHz**
- **PGA: Gains from 1 to 128**
- **INL: 1ppm typical @ Gain = 1**
- **Offset Drift 5 nV/°C**
- **Gain Drift 1 ppm/°C**
- **Specified Drift Over Time**
- **3.0 V to 5.25 V Power Supply**



Resolution	Current	Channels	Output Data Rate	Interface	Package	Temperature
24-Bit	6 mA	2 / 4	4.7 Hz – 4.8 kHz	SPI	24-TSSOP	-40°C to +105°C

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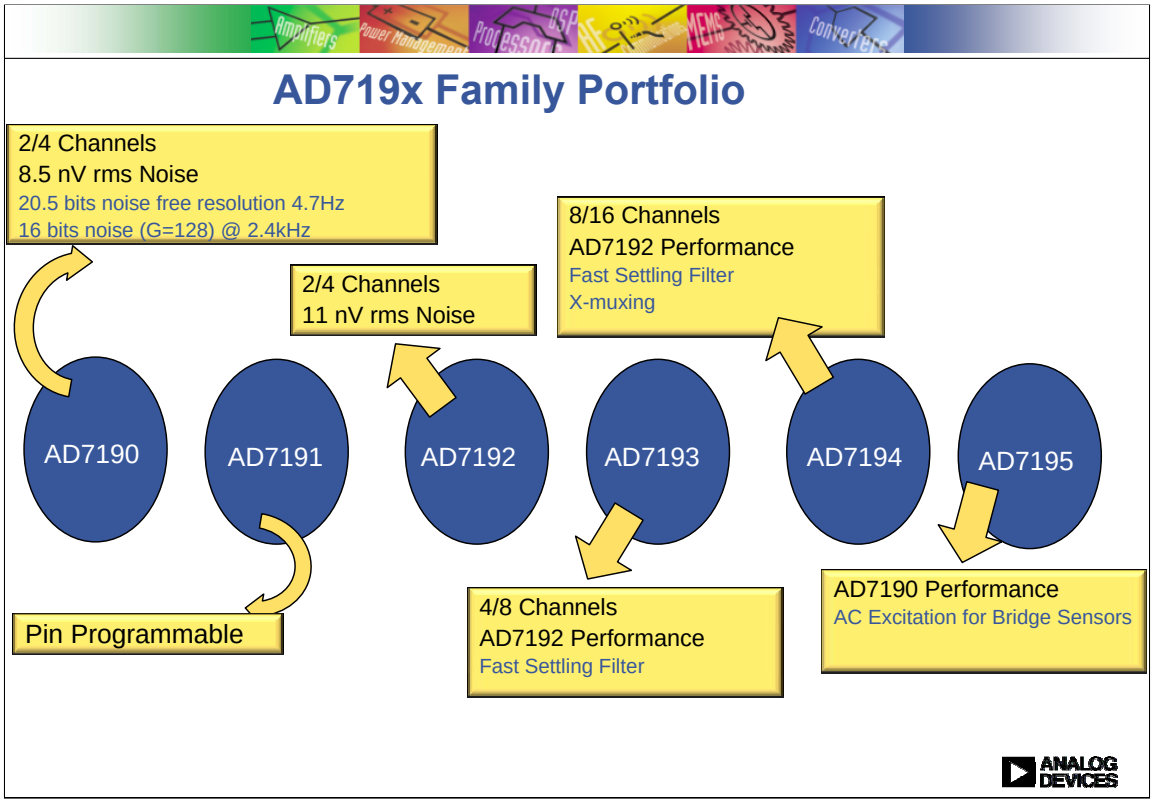
This slide shows the features/benefits of the AD7190.

One of the key specifications for sigma delta converters is the rms noise. The AD7190 is one of the lowest noise converters available on the market. At an output data rate of 4.7 Hz, the rms noise is 8.5 nV when the gain is equal to 128. This equates to 20.5 noise free bits. At a higher output data rate of 2.4 kHz the ADC still maintains good noise performance. At a gain of 128, the ADC has a resolution of 16 noise free bits.

The AD7190 INL is specified at a gain of 1 and for higher gains. At a gain of 1, the INL is 1 ppm typical.

Drift with temperature and time is very important for applications such as weigh scales. The AD7190 has excellent offset and gain drift with temperature. The drift with time has also been characterised and is specified in the datasheet.



Following the release of the AD7190, several other members of the AD719x family were released.

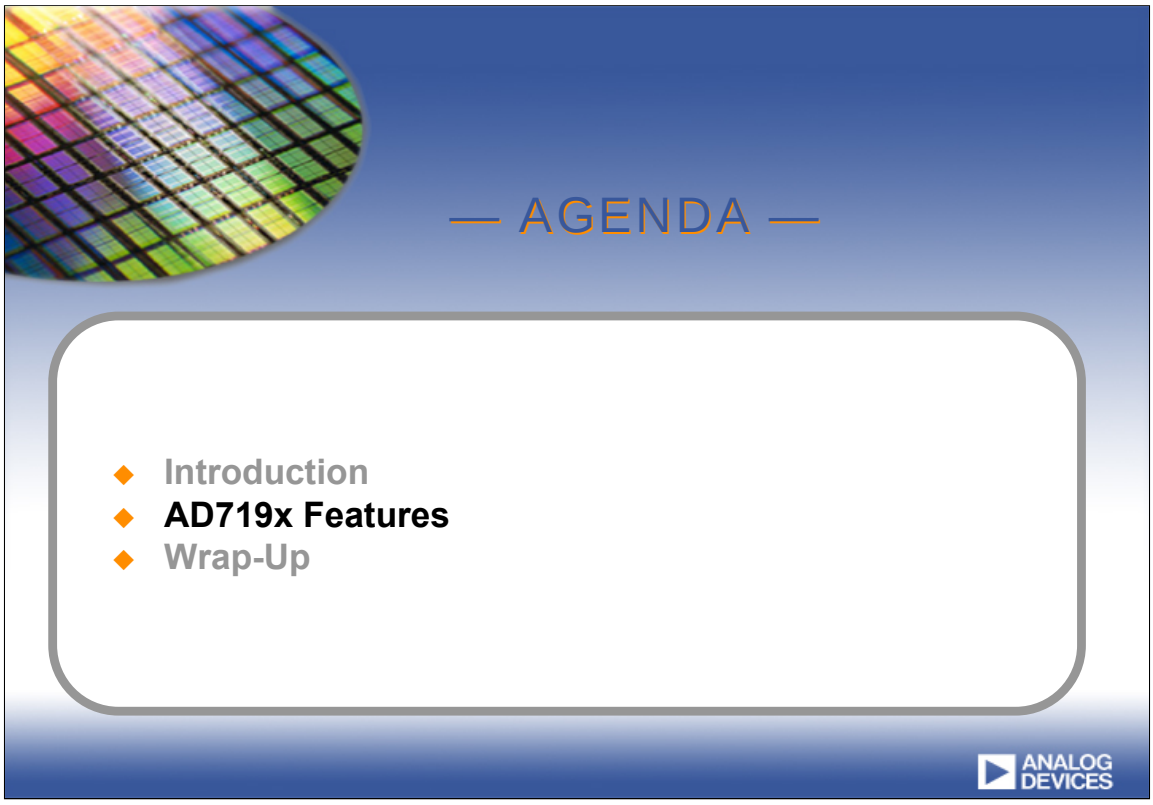
AD7191: Pin programmable part, easy to use. Reduced feature set – 4 gains, 4 output data rates.

AD7192: same pinout as the AD7190. The part has higher noise (11 nV vs 8.5 nV at 4.7 Hz, gain = 128). However, its current consumption is approximately 30% less than the AD7190.

AD7193: same performance as the AD7192 but the part has 4 diff/8 SE inputs. This part also has an extra filtering option (fast filter).

AD7194: same performance as the AD7192. This part has 8 diff/16 SE inputs. It includes the fast settling filter. This part uses x-muxing while the other parts have dedicated input pins.

AD7195: same performance as the AD7190 but the part includes ac excitation also.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AD719x – Main Features

4.8 kHz Ultra-Low Noise 24-Bit Σ-Δ ADC with PGA

- **Programmable Gain Amplifier**
- **2 Fully Differential Channels / 4 Psuedo-Differential Channels**
- **Selectable Sinc^3 or Sinc^4 Digital Filter**
- **Selectable Zero-Latency Mode**
- **Selectable Chop or non-Chopped Input Signal**
- **Simultaneous 50 / 60 Hz Rejection @ 50 Hz o/p data rate**
  - **Also available at lower o/p data rates**
- **Selectable Internal or External Clock**
- **Channel Sequencer**
- **Bridge Power Down Switch**
- **Temperature Sensor**
- **Diagnostics**
  - **Open Sensor Detect & Reference Detect**
- **SYNC pin to synchronise conversion on multiple devices**
- **4 General Purpose Output Pins**

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The AD719x offers excellent performance along with a lot of on-chip features. This slide shows the main features which are available.

Some AD719x Features to Highlight

- **RMS Noise vs Output Data Rate**
- **INL**
- **Sinc^3 versus Sinc^4 Digital Filter**
- **Chop Enabled**
- **Simultaneous 50 / 60 Hz Rejection**
- **Fast Settling (AD7193, AD7194)**
- **X-Muxing (AD7194)**
- **AC Excitation (AD7195)**

The following slides focus on a few performance specifications such as the RMS noise and INL. Why are these specifications important. How do they translate to the performance of the end system.

In addition, the slides will focus on a few of the features

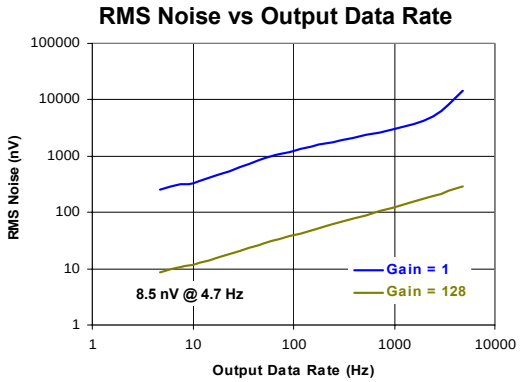
Sinc^3 vs Sinc^4

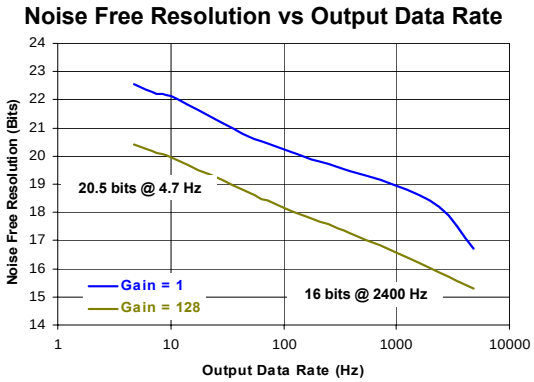
Chop on/off

50 Hz/60 Hz rejection.

The slides discuss these options and highlight the benefits of each option. The fast settling option of the AD7193/4 will also be reviewed along with the x-muxing available on the AD7194 and the ac excitation on the AD7195.

AD7190 – Noise and Resolution
4.8 kHz Ultra-Low Noise 24-Bit Σ-Δ ADC with PGA



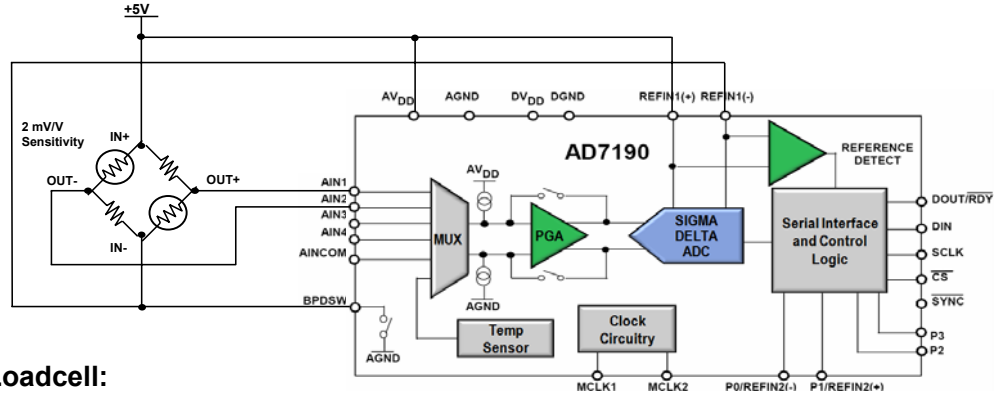


The plots show the rms noise for a gain of 1 and a gain of 128 for the complete range of output data rates (4.7 Hz to 4.8 kHz). From the plot, the rms noise increases linearly as the output data rate increases – the noise performance is good over the complete range of output data rates. The plot on the right shows the corresponding noise free resolution.

As stated previously, rms noise is a key specification for a sigma delta converter. The noise is always specified so that the customer can easily compare parts. The noise free resolution listed in the datasheet uses a full scale span of $\pm V_{REF}$/gain when calculating the resolution. In practice, a customer may not use the full range.

AD719x: RMS Noise vs System Accuracy

Application Example: Weigh Scale Loadcell



- **Loadcell:**
  - **2 mV/V typically => With +5V excitation, full-scale signal from loadcell = 10 mV**
- **AD7190**
  - **With V_{REF} = 5V, Gain = 128, full-scale signal = ±40 mV**
  - **12.5% of range used by loadcell signal**
  - **The loadcell has an offset (~50%) and full- scale error (~±20%). The wider range available from the AD7190 prevents the offset and full-scale error from overloading the AD7190.**

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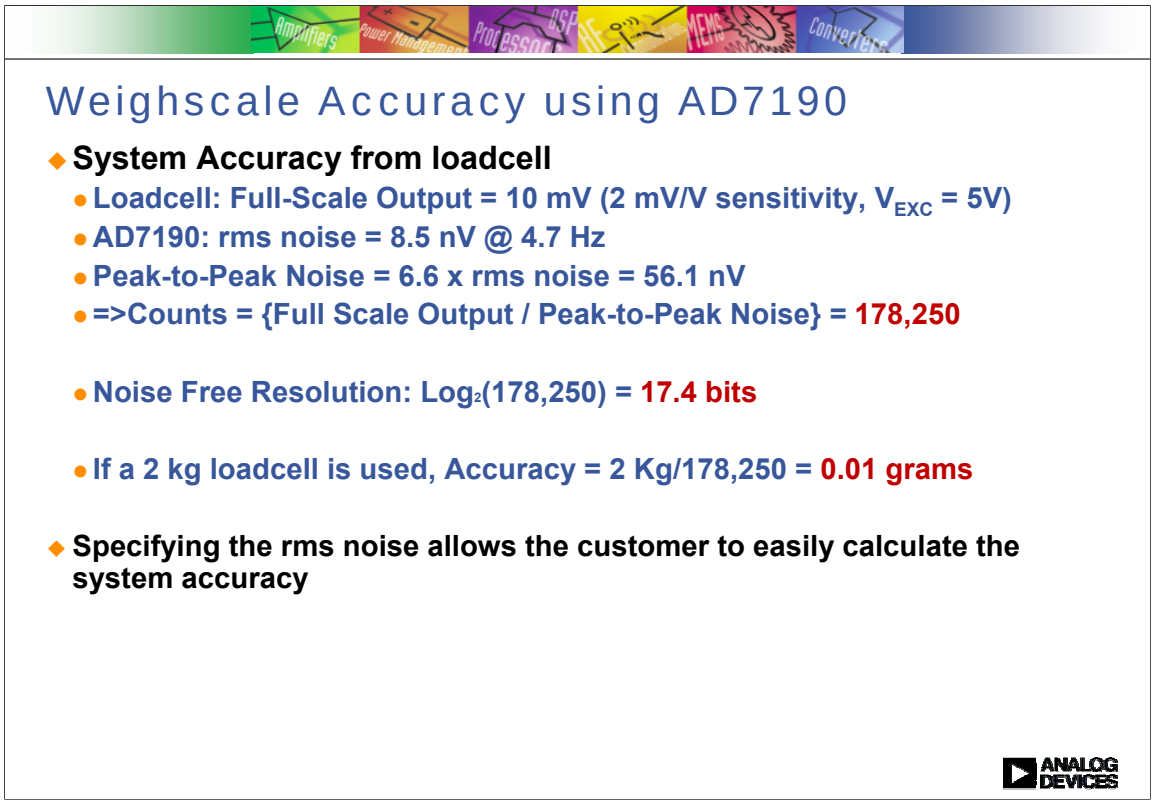
Using a weighscale system as an example, we can calculate the system accuracy if the rms noise and the full scale signal from the sensor is known.

A weigh system is one application example where the ADC's full range is not used. When a +5V excitation voltage and the ADC configured for a gain of 128, the analog input range to the ADC is ±V_{REF}/gain = ±40 mV in bipolar mode.

A loadcell has a sensitivity of 2 mV/V typically. So, with a 5V excitation voltage, the full scale signal generated by the loadcell is 10 mV. Therefore, only 12.5% of the allowed range is used. However, the loadcell has an offset or TARE. The AD7730 included a TARE DAC which could be used to remove the loadcell's offset. However, since the AD7190 has a wider analog input range, a TARE DAC is not required. The offset error has a magnitude of 50% of the full-scale signal typically (5 mV). Similarly, the loadcell has a gain error which can be up to ±20%. Therefore, the wide analog input range of the AD7190 is useful in weigh scale design as the loadcell's offset and gain error can be accommodated by the ADC i.e. the offset and gain error do not overload the ADC.



So, how is the rms noise used to calculate the weigh scale system accuracy?

Knowing the rms noise from the datasheet, the p-p noise can be calculated. The p-p noise is typically 6.6 x rms noise. At an output data rate of 4.7 Hz and the gain set to 128, the AD7190 has an rms noise of 8.5 nV and a p-p noise of 56.1 nV. Weigh scale customers indicate the accuracy of a system in counts.

Counts = Full-Scale Signal from loadcell / p-p noise.

So, a weighscale with a sensitivity of 2mV/V will have 178,250 counts.

In terms of bits, this equates to 17.4 bits.

Finally, if the loadcell accepts a maximum weight of 2 kg so that 10 mV is output when 2 kg is placed on the loadcell, the resolution of the weigh scale is equal to 0.01 grams.

In summary, the full-scale range being used in a weigh scale system differs from the ADC's allowed analog input range. So, by specifying the rms noise, the customer can easily calculate the number of counts that can be obtained from the system.

Weighscale Accuracy using AD7192

- **System Accuracy from loadcell**
  - **Loadcell: Full-Scale Output = 10 mV**
  - **AD7192: rms noise = 11 nV @ 4.7 Hz**
  - **Peak-to-Peak Noise = 6.6 x rms noise = 72.6 nV**
  - **=>Counts = {Full Scale Output / Peak-to-Peak Noise} = 137,740**
  - **Noise Free Resolution: Log_2(137,740) = 17.1 bits**
  - **If a 2 kg loadcell is used, Accuracy = 2 Kg/137,740 = 0.015 grams**
    - (AD7190: 8.5 nV rms noise, Accuracy = 0.01 grams)

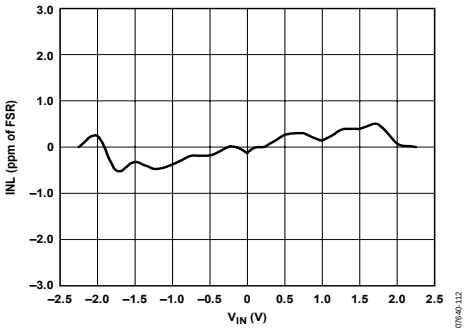
How does the higher noise of the AD7192 affect the system accuracy when it is used in a loadcell application?

The higher rms noise leads to a degraded end accuracy. The accuracy is now 0.015 grams (it was 0.01 grams with the AD7190).

So, rms noise allows the customer to calculate the expected system performance.

Integral Nonlinearity (INL)

- **Linearity is the absolute accuracy of an ADC**
  - **Following a zero-scale and full-scale calibration, INL is the deviation of the actual output code from the theoretical output code.**
- **AD7190's INL @ gain = 1: 1 ppm typ, 5 ppm max**



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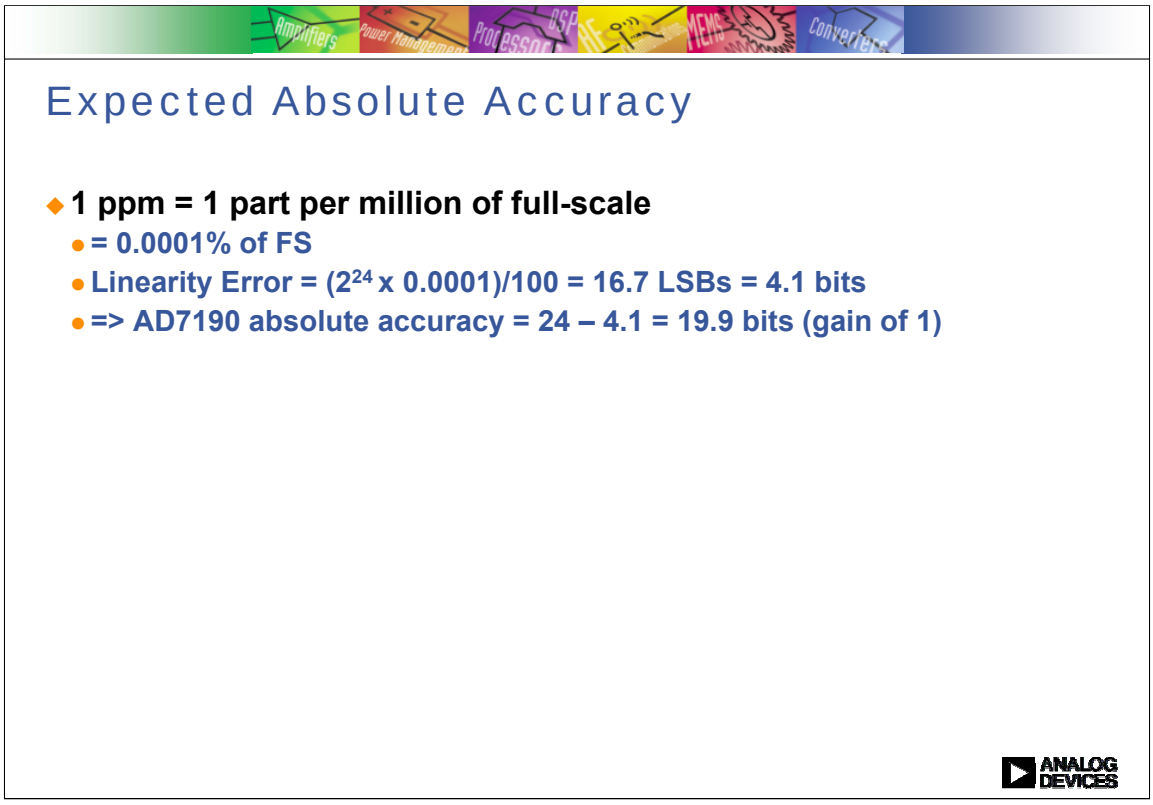
The other specification worth highlighting is the linearity. What is integral nonlinearity (INL).

INL is the maximum deviation of any code from a straight line passing through the endpoints of the transfer function. The endpoints of the transfer function are zero scale (not to be confused with bipolar zero), a point 0.5 LSB below the first code transition (000 . . . 000 to 000 . . . 001) and full scale, a point 0.5 LSB above the last code transition (111 . . . 110 to 111 . . .111). The error is expressed in ppm.

The INL indicates the absolute accuracy of the ADC. The rms noise indicates the relative accuracy. Good INL is essential along with good rms noise.

The AD7190 has an INL of 1ppm typical at a gain of 1.



This slide explains INL further. If the INL is equal to 1 ppm typically, what does this mean in terms of bits.

INL is specified in ppm of FSR (full scale range) in the datasheet.

1 ppm of FSR is equal to 0.0001% of FSR.

FSR is equal to 2^{24} bits or 16777216 as the AD7190 is a 24-bit part.

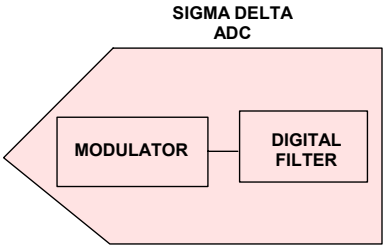
So, 0.0001% of 16777216 is equal to 17.6 LSBs. This equates to 4.1 bits.

Therefore, the difference between the actual output code from the AD7190 and the theoretical or expected output code can be up to 4.1 bits.

This means that the absolute accuracy of a system using the AD7190 is 24 – 4.1 = 19.9 bits.

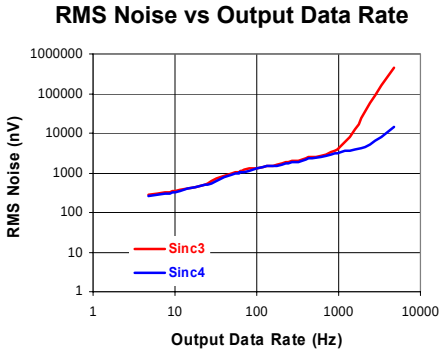
Sinc^3 versus Sinc^4 Filter

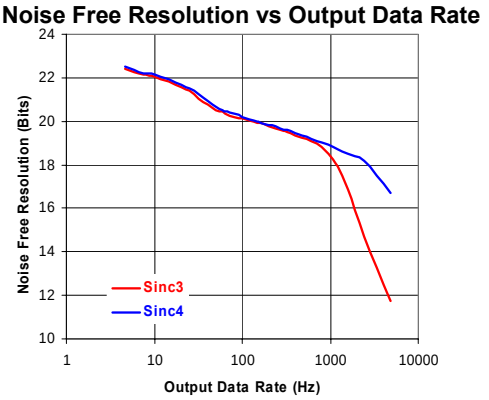
- **Choice of Sinc^3 or Sinc^4 Digital Filter**
- **User selectable**
- **Filter Choice affects**
  - **Settling Time**
  - **Resolution**
  - **50 Hz/60 Hz Rejection**



The AD719x has 2 digital filter options – a sinc^3 filter and a sinc^4 filter. The user can select which filter type to use using the SINC3 bit on the part. The filter chosen affects the settling time, the resolution and the 50/60 Hz rejection.

Sinc^4 vs Sinc^3 RMS Noise/Noise Free Resolution (Gain = 1)





- **Noise Free Resolution comparable for output data rates up to 1 kHz. Above this output data rate, the Sinc^4 Filter gives superior performance compared with the Sinc^3 Filter**

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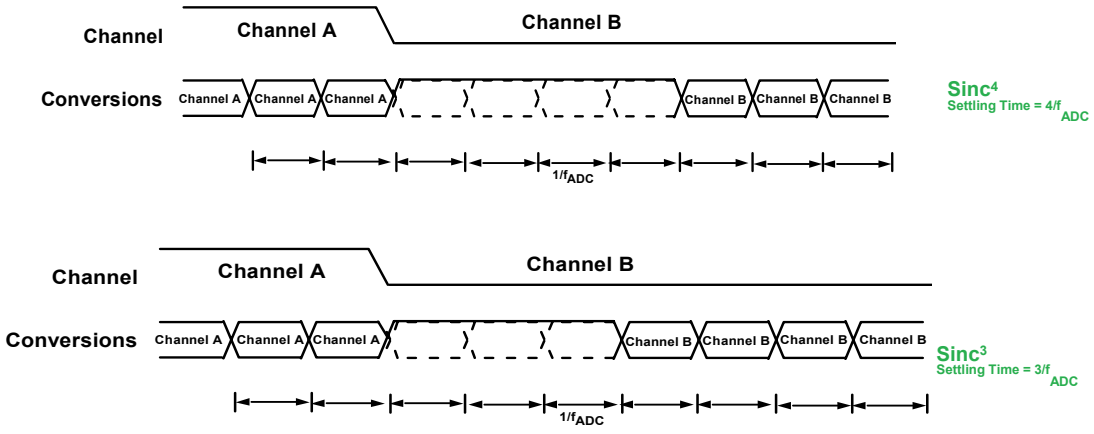
The above plots show the rms noise and the noise free resolution of the AD719x when using the sinc^3 filter and the sinc^4 filter. At low output data rates, the rms noise / p-p resolution is similar for the 2 filter types. However, at output data rates around 1 kHz and above, the rms noise increases rapidly for the sinc^3 filter while the sinc^4 filter still maintains good noise performance. Therefore, if a customer is using the AD719x at low output data rates, either the sinc^3 or sinc^4 filter can be selected. However, at high output data rates, the sinc^4 filter should be selected as this filter gives the best noise performance.

Settling Time (Sinc^4 vs Sinc^3)

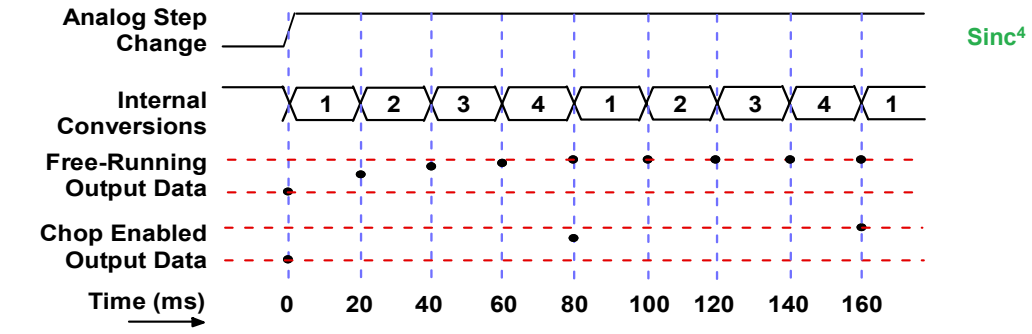


- **For the same output data rate, the Sinc^3 filter has a lower settling time than the Sinc^4 filter.**

The choice of filter also affects the settling time. The above plots show the settling time required when the channel is changed. If the conversion time is t_{ADC} (=1/output data rate), then the settling time is equal to 3 x t_{ADC} when the sinc^3 filter is used and 4 x t_{ADC} when the sinc^4 filter is used. So, for the same output data rate, a sinc^4 filter takes one conversion cycle longer to settle compared with a sinc^3 filter.

Chop Enabled versus Chop Disabled

- **Chopping minimizes analog input offset and offset drift**
- **Chopping significantly improves offset performance at gains from 1 to 16**
  - Very good performance at gains 32 to 128 regardless
- **Chopping affects the output data rate and the filter response**



Chop Disabled: Output Data Rate (f_{ADC}) = 50 Hz, Settling Time= 4/50 Hz = 80 ms

Chop Enabled: Output Data Rate (f_{ADC}) = 12.5 Hz, Settling Time = 2/12.5 Hz = 160 ms

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The AD719x includes chopping on-chip. By default, chopping is disabled. Chopping is used to minimise the offset and offset drift. The offset is continuously removed so the result is low offset and low offset drift.

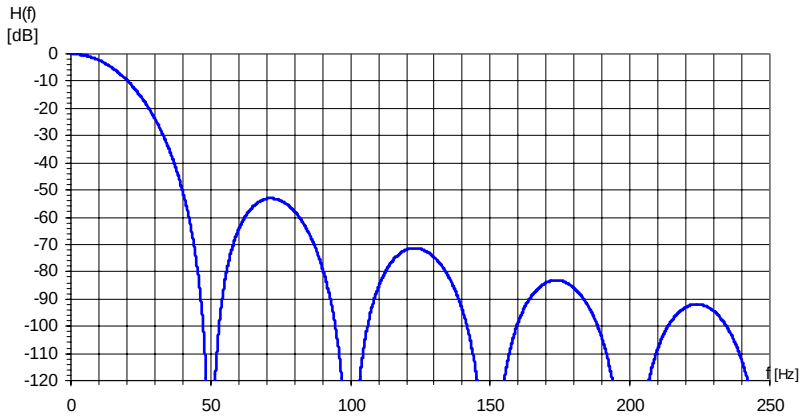
At gains of 1 to 16, the offset and offset drift is improved a lot. For higher gains, the AD719x has very low offset and offset drift. So, for these gains, there is no need to use chopping.

Chopping affects the output data rate and the filter response.

With chopping, the analog input pins are continuously switched. So, with the analog input pins connected to the analog input, the settling time is allowed to generate a valid conversion. The analog input pins are then reversed within the AD719x. The complete settling time must now elapse to generate a valid conversion. Subsequent conversions are then averaged. This removes the offset. Since this is done continuously, the offset and offset drift is minimised.

However, the continuous switching of the analog input pins reduces the output data rate. If the sinc^4 filter is used and there is a step change on the analog input, the conversions are valid after 4 conversion cycles when chopping is disabled. With chopping enabled, it will be 8 cycles later before a valid conversion is available.

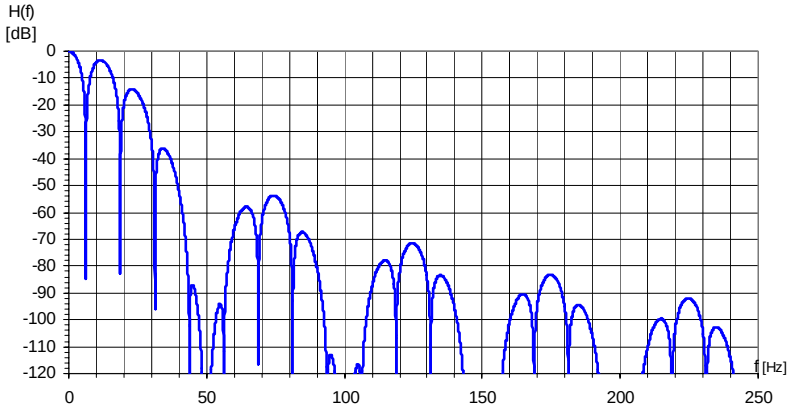
Sinc^4 Filter, Chop Disabled



- **50 Hz Output Data Rate**
  - **Notches at 50 Hz and multiples of 50 Hz**

The filter response is also altered when chopping is enabled. The above plot shows the frequency response when chopping is disabled and the output data rate is equal to 50 Hz. The first notch occurs at 50 Hz with subsequent notches occurring at multiples of 50 Hz (100 Hz, 150 Hz, 200 Hz,….).

Sinc^4 Filter, Chop Enabled



- **Output Data Rate (f_{ADC}) = 50 Hz/4 = 12.5 Hz (Sinc^4)**
  - **Notches at $f_{ADC}/2$, $3f_{ADC}/2$, $5f_{ADC}/2$…….**
  - **Notches can be used for simultaneous 50 Hz/60 Hz rejection**

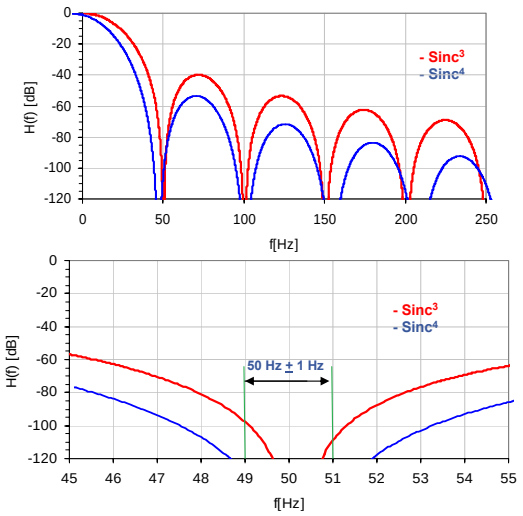
When chopping is enabled, the output data rate is reduced to 50 Hz/4 = 12.5 Hz for the sinc^4 filter. Additional notches are present in the filter response also. So, notches are still present at 50 Hz and multiples of 50 Hz. However, notches are also placed at 12.5 Hz/2, 3 x 12.5Hz/2, 5 x 12.5Hz/2……

These notches can be used to provide simultaneous 50 Hz/60 Hz rejection.

Simultaneous 50/60 Hz Rejection

Sinc Filter Order vs Rejection

- **Interference due to mains power supply introduces tones at 50 Hz and/or 60 Hz**
- **These tones need to be filtered**
- **Sinc filter has notches which can be used to filter tones**
- **Notches position the same for each filter order**
- **Notch width increases as Filter order increases.**
- **Stopband attenuation improves as Filter order increases**



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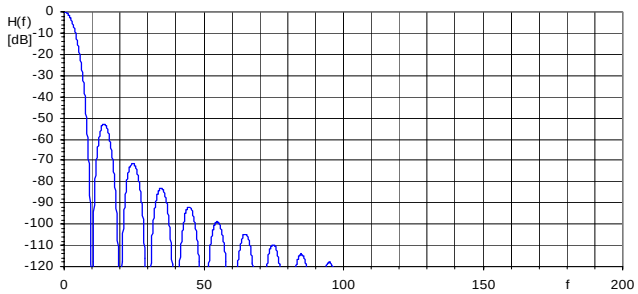
The mains power supply introduces interference at 50 Hz and/or 60 Hz. These tones need to be filtered. A sinc filter has notches which can be used to filter the 50/60 Hz interference. This is one benefit of sinc filters. For a given output data rate, the notch locations are the same for the sinc3 and sinc4 filters. However, the higher order filter has wider notches. Although we talk about 50/60 Hz rejection, the interference is not at 50 or 60 Hz exactly – there will be some variation. Therefore, datasheets normally specify the rejection that is achievable in a 1 Hz band about 50 Hz or about 60 Hz. Therefore, a sinc4 filter will give better 50/60 Hz rejection compared with a sinc3 filter.

Sinc^4 Filter, Chop Disabled
Simultaneous 50 / 60 Hz Rejection, f_{ADC} = 10 Hz

AD7190 Sinc^4, Chop Disabled, f_{ADC} = 10 Hz, t_{SETTLE} = 400 ms
50 Hz & 60 Hz Rejection: >120 dB



- **Summary**
  - **Best Simultaneous 50 / 60 Hz (±1Hz) Rejection: > 120 dB**
    - Sinc^4 filter gives the widest rejection notch
  - **Highest 1st Stop-Band Attenuation >50dB**
  - **Longest Settling Time (T_{settle}) of 4 / f_{ADC} = 400 ms**

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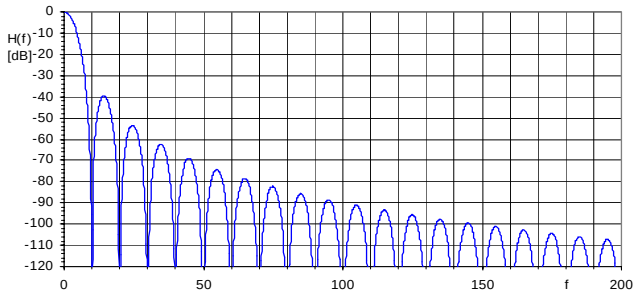
The next few slides compare the different filter types on the AD719x in terms of 50/60 Hz rejection. For each filter type, the maximum output data rate that give simultaneous 50/60 Hz rejection is used. Along with the rejection, the stopband attenuation and settling time are also listed.

When the sinc4 filter is selected with chop disabled, an output data rate of 10 Hz gives simultaneous 50/60 Hz rejection. The rejection at 50/60 Hz +/-1 Hz is in excess of 120 dB.

The stopband attenuation is also good at 50 dB. The setting time is quite long. It equals 400 ms.

Sinc^3 Filter, Chop Disabled
Simultaneous 50 / 60 Hz Rejection, f_{ADC} = 10 Hz

AD7190 Sinc^3, Chop Disabled, f_{ADC} = 10 Hz, t_{SETTLE} = 300 ms
50 Hz Rejection: 103 dB, 60 Hz Rejection: 105 dB



- **Summary**
  - **Very Good Simultaneous 50 / 60 Hz (±1Hz) Rejection: > 100 dB**
    - Sinc^3 filter gives a less wide rejection notch than Sinc^4 filter
  - **High 1st Stop-Band Attenuation = 40dB**
  - **Long Settling Time (T_{settle}) of 3 / f_{ADC} = 300 ms (shorter than Sinc^4)**

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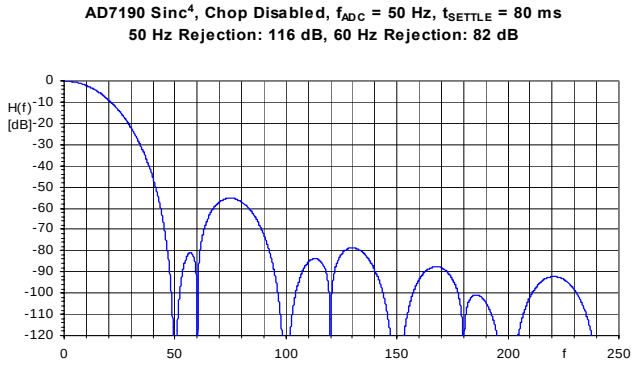
When the sinc3 filter is used with chop disabled, an output data rate of 10 Hz is again required for simultaneous 50/60 Hz rejection. Since the sinc3 notches are not as wide as the sinc4 notches, the 50/60 Hz rejection is reduced to 100 dB. The stopband attenuation is also less at 40 dB. However, the settling time is 300 ms compared with 400 ms for the sinc4 filter.

Sinc^4 Filter, Chop Disabled – REJ60
Simultaneous 50 / 60 Hz Rejection, f_{ADC} = 50 Hz



- **Summary**
  - **Simultaneous 50 / 60 Hz (±1Hz) Rejection: > 80 dB**
    - Sinc^4 filter gives the deepest rejection notch
  - **Highest 1st Stop-Band Attenuation > 50dB**
  - **Shorter Settling Time (T_{settle}) of 4 / f_{ADC} = 80 ms**

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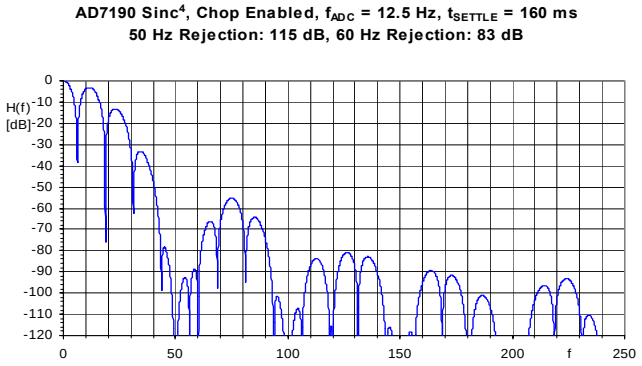
There is a bit REJ60 on the AD719x devices which places a first order notch at 60 Hz when the first notch of the sinc filter is at 50 Hz. So, again using the sinc4 filter with chop disabled, the output data rate can be increased to 50 Hz which results in the first notch of the sinc filter being at 50 Hz. Enabling the REJ60 bit places a notch at 60 Hz. With this configuration, the rejection at 50/60 Hz is 80 dB. The stopband attenuation is 50 dB and the settling time is 80 ms. In summary, the rejection is degraded compared to the first sinc4 example shown. However, using the REJ60 bit allows a higher output data rate which translates to a smaller settling time (80ms).

Sinc^4 Filter, Chop Enabled

Simultaneous 50 / 60 Hz Rejection, f_{ADC} = 12.5 Hz



- **Summary**
  - **Simultaneous 50 / 60 Hz (±1Hz) Rejection: > 80 dB**
    - Minimizes offset and offset drift
  - **Low 1st Stop-Band Attenuation ~10dB**
  - **Medium Settling time of 2 / f_{ADC} = 160 ms**

When the sinc4 filter is used and chopping is enabled, an output data rate of 12.5 Hz gives simultaneous 50/60 Hz rejection. In this case, the 50/60 Hz rejection is in excess of 80 dB. The stopband attenuation is poor at 10 dB. The settling time is 160 ms. So, the settling time is good when the above configuration is used. However, the stopband attenuation is not. So, there is a trade-off between 50/60 Hz rejection, stopband attenuation and settling time.

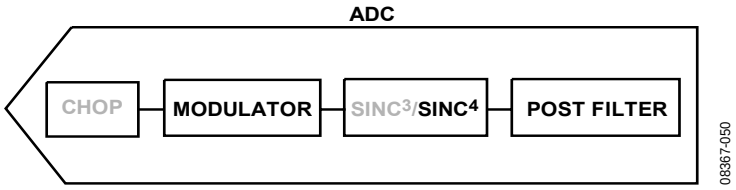
Fast Settling – AD7193, AD7194

- **Customers require 50/60 Hz rejection for mains-powered applications.**
  - **Output Data rate = 50/60 Hz max to achieve this rejection**
- **Along with rejection, minimum settling time required**
  - **Output Data Rate = fADC**
  - **Wish to have settling time = 1/fADC**
- **Useful in PLC applications where the number of channels being converted per second is increasing**

The AD7193 and AD7194 have one extra filter option – the fast settling mode.

Customers require 50/60 Hz rejection to rejection any interference from the mains power supply. In addition, they require the minimum settling time. A output data rate of 50 Hz places a notch at 50 Hz, giving 50 Hz rejection. Ideally, a customer would like the settling time to be 1/50 = 20 ms. This is useful in multi-channel applications such as PLC since a smaller settling time means that the number of channels that can be converted per second is increased.

Fast Settling – AD7193, AD7194



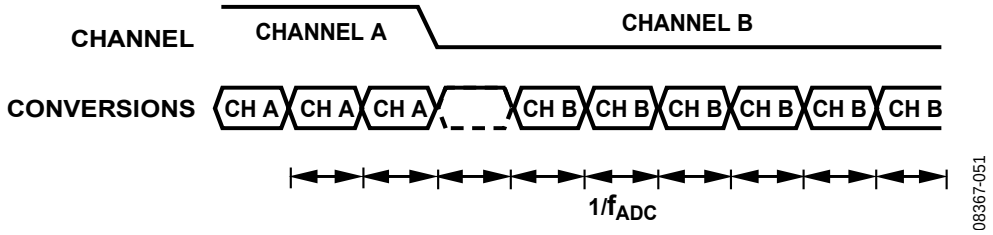
- **Averaging Block included after sinc^3/sinc^4 filter**
- **Can average by 2, 8 or 16**
- **Settling time approximately equals inverse of first notch**

The AD7193 and AD7194 have a post filter after the sinc3/sinc4 filter. This post filter allows the user to average the output from the sinc filter by 2, 8 or 16. By using this averaging, the settling time approximately equals the inverse of the filter filter notch. Therefore, a notch can be placed at 50 Hz, for example, and the corresponding settling time equals 1/50 = 20 ms approximately.

AD7193 & AD7194: Fast Settling Mode

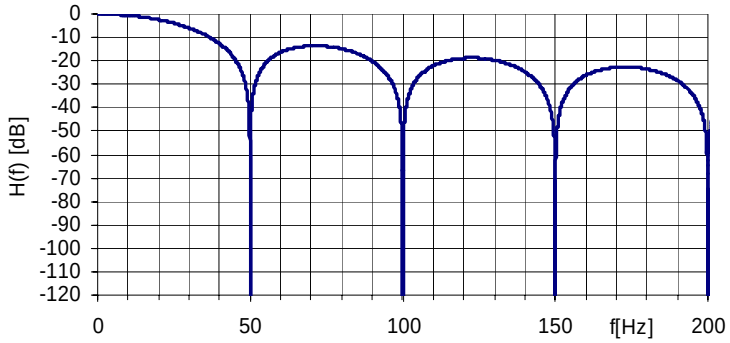
- **Settling Time approximately equals inverse of first filter notch**
  - **50 Hz notch with settling time approximately 1/50 = 20 ms**
  - **60 Hz notch with settling time approximately 1/60 = 16.6 ms**

- $f_{ADC} = f_{CLK}/((N + Avg - 1) \times 1024 \times FS[9:0])$
- $t_{SETTLE} = 1/f_{ADC}$
- **Part operates as zero latency ADC**



The complete equation for the output data rate and corresponding settling time is given above. A point of interest is that the ADC operates as a zero latency ADC when the fast settling mode is used. So, the conversion time is equal to the settling time. This means that extra time is not required to generate the first conversion after a channel change.

Sinc^4 Filter, Fast Settling



- **FS = 6: First Notch due to Sinc filter is at 800 Hz**
- $f_{NOTCH} = f_{CLK}/(1024 \times FS[9:0])$
- **Average by 16: notches at multiples of 800 Hz/16 = 50 Hz**
  - **Output Data Rate = 42.1 Hz**
  - **Settling Time (T_{settle}) = 23.8 ms**
  - **50 (±1Hz) Rejection: > 40 dB**

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In fast settling mode, 50 Hz rejection can be achieved as follows:

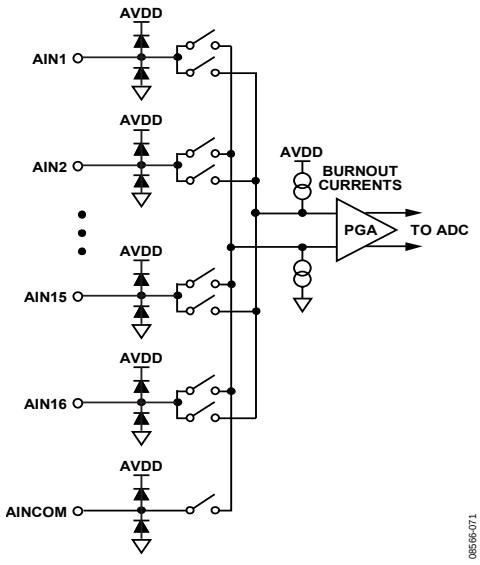
The FS bits in the mode register are set to 6 so that the first notch of the sinc filter is placed at 800 Hz. Averaging by 16, notches are placed at 800/15 = 50 Hz and multiples of 50 Hz. The output data rate equals 42.1 Hz with the settling time equal to 1/42.1 = 23.8 ms. So, the settling time achievable while still getting 50 Hz rejection is much faster than the previous configurations. First order notches are placed at 50 Hz, 100 Hz, etc. Therefore, the rejection is only 40 dB. The rejection is a lot less than achieved with the previous configurations.

Filter Options Summary

- **AD719x Family offers flexibility**
- **Filter type selected determines**
  - **Rms noise**
  - **50 Hz/60 Hz rejection**
  - **Settling Time**
  - **Stopband Attenuation**
  - **Trade-off required between rejection, settling time, noise**

In summary, the AD719x family have a lot of different configurations which offers flexability to the user. However, the filter type affects the rms noise, the 50/60 Hz rejection, the settling time and stopband attenuation. So, a trade-off is needed amount the different parameters.

X-Muxing (AD7194)

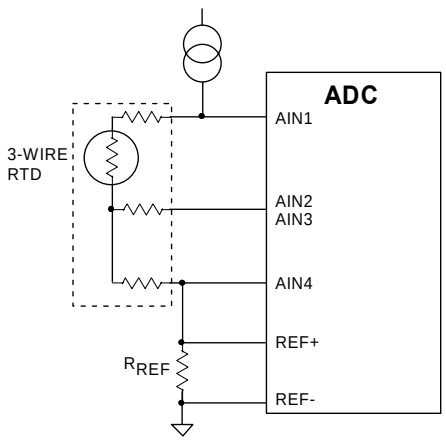


- **Any input pin can be selected as the positive input**
- **Any input pin can be selected as the negative input**
- **AINCOM can be a negative input only**
- **No channel sequencer**

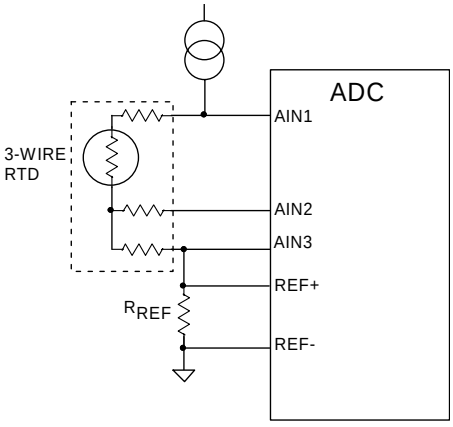
The AD7194 has x-muxing rather than having dedicated analog input pins. Therefore, any pin can be configured to be a positive analog input and any input pin can be configured to be a negative input. The pin AINCOM can be a negative input only. X-muxing offers a lot of flexibility. To accommodate the x-muxing, the AD7194 does not have the channel sequencer as this would complicate the design considerably.

X-Muxing vs. Dedicated Inputs

Less pins used with x-muxing for 3-wire RTD



Dedicated Input Pins



X-muxing

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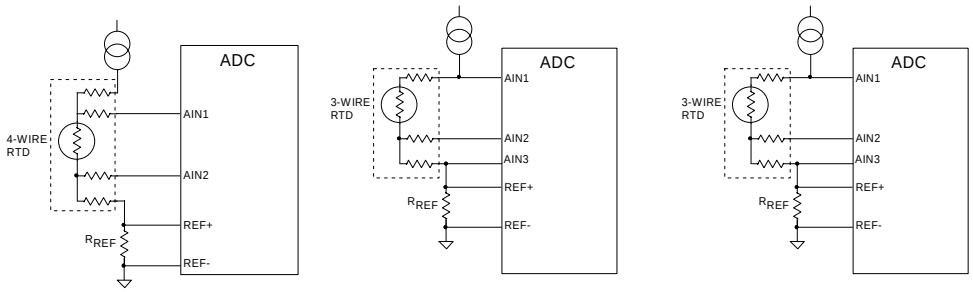
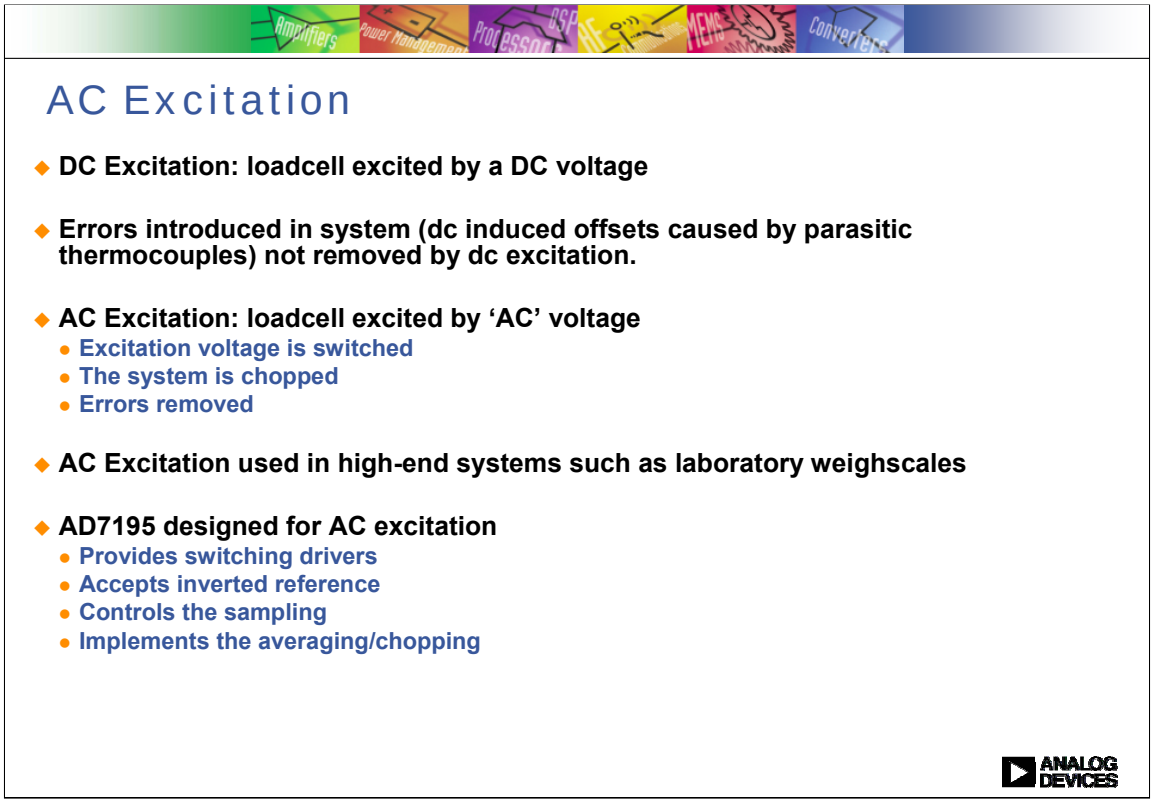
The above slides compares the connections between a 3-wire RTD and an ADC when the ADC has dedicated analog input pins and x-muxed inputs. When dedicated input pins are used, 4 pins are needed to interface to the RTD. When using x-muxing, the pin count is reduced to 3. Therefore, x-muxing reduced the number of input pins needed to interface to the sensor.

Other X-Muxing Benefits



- **X-Muxing allows customer to design generic input module**
  - **Same PCB can be used for 3-wire and 4-wire RTDs**
- **X-muxing also useful for diagnostics**

X-muxing also allows a user to develop a generic input module which can accommodate 3 and 4 wire RTDs – the same PCB can be used. Finally, x-muxing is useful for diagnostic purposes also.



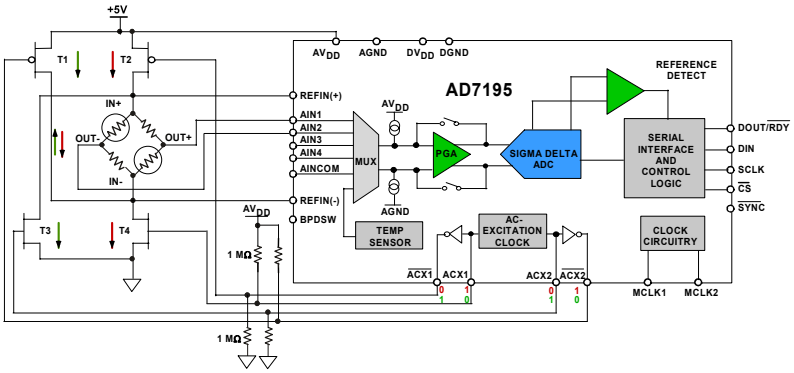
The final section discusses ac excitation. The loadcell example shown earlier used dc excitation where the loadcell is excited by a constant dc voltage. Errors are introduced into the sytem due to dc induced offsets caused by parasitic thermocouples. These errors are not compensated for when the system is dc excited. With ac excitation, the loadcell is excited by an 'ac' voltage i.e. the voltage to the loadcell is switched. So, the system is effectively chopped. This removes the dc induced offsets.

Ac excitation is used in high end systems such as laboratory scales where very high precision is required.

The AD7195 is designed for ac excited systems. It provides the switching drivers which drive external transistors, it accepts an inverted reference. It controls the switching, the sampling and the averaging/chopping. The only external components required are the transistors.

AD7195 – Application Example

Weigh Scale Loadcell using AC Excitation



- **AC Excitation chops the signal path, removing these offsets.**
  - Phase A: transistors T2 and T4 on, T1 and T3 off
  - Phase B: transistors T1 and T3 on, T2 and T4 off (signal through loadcell inverted)
    - Voltage at AIN and reference voltage inverted
  - ADC averages the 2 conversions, removing the dc induced offset

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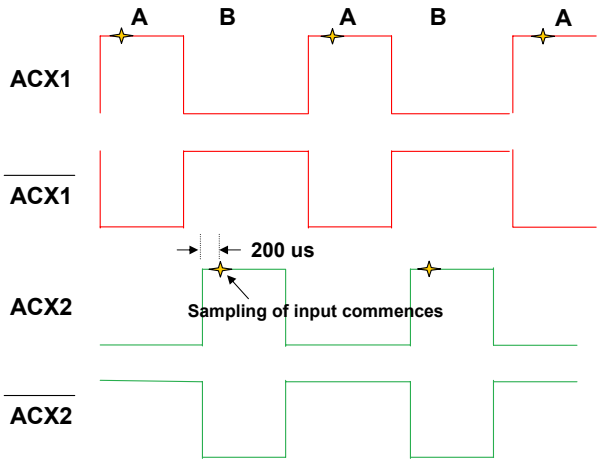
This slide shows the connections between the AD7195 and the loadcell when ac excitation is used. In phase A, transistors T2 and T4 are turned on, T1 and T3 are turned off. So, the excitation voltage is applied to the top of the bridge. In phase B, T2 and T4 are turned off while T1 and T3 are turned on. The excitation voltage is now applied to the bottom of the bridge so that the voltage at AIN and Vref are inverted. The ADC samples the analog input during phase A and phase B. The 2 conversions are then averaged, removing the dc induced offsets.

AD7195 Signals during AC Excitation



- **ACX1 and ACX2 signals are non-overlapping**
  - No short circuiting
- **After switching, delay of 200 us (100 uS at 4.8 kHz) before analog input sampled**
  - Allows analog input to settle
- **1 MΩ pull-up/down resistors prevent short circuiting during power-up.**

The signals ACX1, \ACX1, ACX2 and \ACX2 control the switching of the transistors T1 to T4. ACX1 and ACX2 are non-overlapping. Therefore, short circuiting cannot occur when switching the transistors on and off.

After switching, there is a delay of 200 us before the ADC begins sampling the analog inputs. This period of time is allowed for the analog input to settle. When the 4.8 kHz output data rate is used, the delay is reduced to 100 us.

1 Mohm pull-up/pull-down resistors are recommended as there is the possibility of short circuiting during power up.

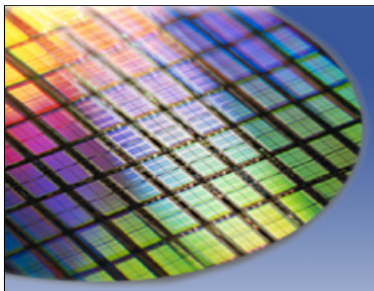
AC vs DC Excitation

- **P-P Resolution: ½ LSB increase when ac excitation used**

  AD7195
- **Throughput reduced by 1/4 (sinc^4 filter) or 1/3 (Sinc^3 filter) when AC excitation used**
  - **For example, Sinc^4, Chop Disabled**
    - Maximum output data rate = 4.8 kHz (DC Excitation)
    - Maximum output data rate = 1.2 kHz (AC Excitation)

As stated previously, ac excitation removes any dc induced offsets. Due to the averaging, the p-p resolution is also improved by 0.5 LSBs.

The disadvantage of ac excitation is the reduced output data rate. The output data rate is reduced by a factor of 4 when the sinc4 filter is used and by a factor of 3 when the sinc4 filter is used. Therefore, if the maximum output data rate equals 4.8 kHz when dc excitation is used, the output data rate is reduced to 1.2 kHz when ac excitation is used (sinc4 filter). This is due to the averaging of consecutive conversions.



— AGENDA —

- Introduction
- AD719x Features
- **Wrap-Up**

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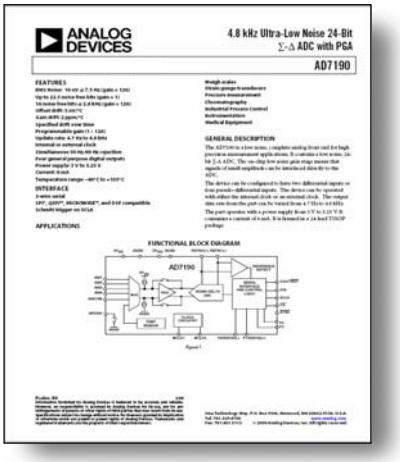
Design Tools

- **Datasheets**
- **Samples**
- **Evaluation / Demo Kit**
- **Application Notes**
  - AN-0979: Digital Filtering Options
  - AN-1069: Zero Latency
  - AN-1084: Channel Switching
- **Filter Models**
- **Circuits from the Lab**
  - CN-0102: Weigh Scale design using AD7190
  - CN-0118: Weigh Scale design using AD7191
  - CN-0119: Weigh Scale design using AD7192
  - CN-0155: Weigh Scale design using AD7195
- **www.analog.com/sigmadelta**
- **http://processcontrol.analog.com/en/segment/pcia.html**
- **http://instrumentation.analog.com/en/segment/im.html**



Samples and an evaluation board are available for each product. Excel models which show the filter response for the different filter types and output data rates are also available. The model also indicates the output data rate, settling time and 50/60 Hz rejection for the configuration selected.

There are several ‘Circuits from the Lab’ notes available which show the performance of the AD719x family in a specific application.

Finally, several application notes are available on the web which discuss specific features of the AD719x family, for example, the switching time when several analog input channels are being used.