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Chopping on the AD7190, AD7192, AD7193, AD7194, and AD7195
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INTRODUCTION

Chopping is a technique used to minimize offset error, offset error drift, and other low frequency errors. This application note describes how chopping is implemented and highlights the benefits of chopping.

OFFSET ERRORS

Offset voltage errors arise at many points within a signal processing chain, such as the temperature-dependent thermocouple voltage that arises when two dissimilar metals are joined. Within an integrated circuit such as an ADC, there are numerous sources of internal offset errors, such as offset due to the instrumentation amplifier, charge injection onto the sampling capacitor when a sampling switch is closed, or interference from EMI radiation. These offsets are generally undesirable and are problematic if they change with temperature since a one-time calibration is not sufficient to remove offset errors across all temperatures and power supplies.

CHOPPING

An offset that arises within the various amplifiers of the Σ-Δ modulator can generally be nulled out, either by local chopping or auto-zeroing the amplifier. However, other offset errors cannot be removed by these methods. The solution implemented on these ADCs is to chop the entire analog signal chain within the ADCs. This removes any offset and low frequency errors, resulting in extremely low offset errors and offset error drift. The chopping scheme is shown in Figure 1.
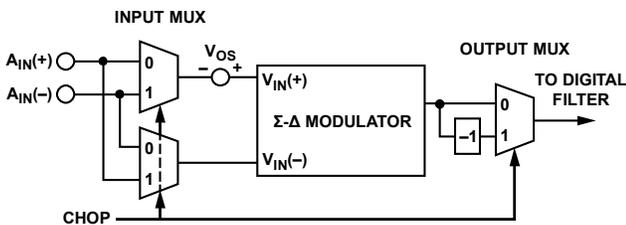

Figure 1. Chopping

The differential input to the modulator is alternately inverted (or chopped) at the input multiplexer and an ADC conversion is performed for each phase of chop. The modulator chopping is reversed in the output multiplexer before passing to the digital filter.

If the offset in the Σ–Δ modulator is represented as V_{OS}, then the output when chop is 0 is

$$(A_{IN}(+) - A_{IN}(-)) + V_{OS}$$

and the output when the chip is 1 is

$$-[(A_{IN}(-) - A_{IN}(+)) + V_{OS}]$$

The error voltage, V_{OS}, is removed by averaging these two results in the digital filter giving

$$(A_{IN}(+) - A_{IN}(-))$$

which equals the differential input voltage without any offset term.

RESULT/CALIBRATION

The effect is to virtually eliminate any offset errors arising within the ADC, and more importantly, to minimize any offset drift due to temperature. The drift of these ADCs is specified as ±5 nV/°C typical. In fact, it is practically unmeasurable. The entire analog circuitry is chopped from the input multiplexer to the modulator output. ADC offset calibrations are, therefore, not required.

The offset error specification of the ADC is ±0.5 µV typical. This is measured with 0 V applied externally to the part sitting in a PCB socket and, therefore, mostly comprises thermocouple errors due to different metals used in the various contacts (PCB track, solder, lead frame, bond wire, die metallization, and so on).

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REVISION HISTORY

10/11—Revision 0: Initial Version

UNDERSTANDING THE STEP RESPONSE

Since the ADC needs to perform a conversion for chop = 0 and chop = 1, the first output from the ADC takes two conversion periods ($2 \times t_{ADC}$) so there is a settling time of two conversion periods for the first output. Subsequent outputs occur every conversion period (t_{ADC}).

The delay of two conversions occurs after a channel is changed, after the PGA is changed, or after an ADC mode change (for example, after exiting power-down, so that no intermediate/invalid outputs are produced—the first output after a channel change is 100% settled to the new channel voltage.)

If the analog input undergoes a step change external to the ADC, say, for example, if a sensor output changes suddenly or an external multiplexer is switched, the ADC does not automatically detect that a change has occurred. It produces outputs that are a weighted average of the new input and the old input, unless the ADC is instructed to start a fresh conversion by means of interrupting the converter when the external multiplexer is switched, then restarting the ADC so that it produces an output $2 \times t_{ADC}$ later.

There is nothing unusual about the ADC producing intermediate values after a change in the input signal. This behavior is identical to that of an analog filter. If a step change is applied to the input of an analog low-pass filter, for a period of time the output reflects a combination of the old analog input and the new analog input. It is only after a sufficient number of time constants have elapsed that the output of the filter fully reflects the new input value.
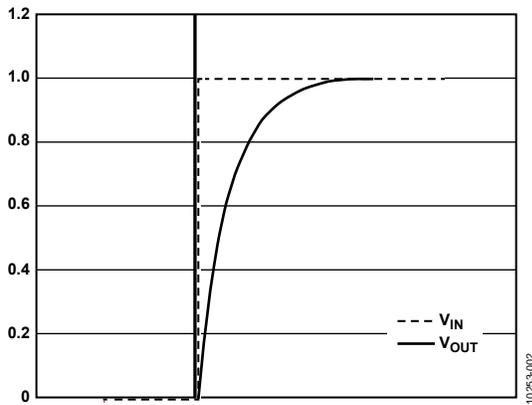

Figure 2. Analog Filter Step Response

These Σ-Δ ADCs contain a low-pass filter with a given 3 dB frequency and settling time, therefore its response is similar in discrete time, although with a finite duration impulse/step response.

The only characteristic of these ADCs that may be unexpected is that there can be two intermediate outputs after a change in analog input (zero latency mode disabled). This is a conse-

quence of chopping. A chopped ADC output is the average of the current ADC conversion and the previous conversion.

If the analog input changed part way through an ADC conversion period, then the current ADC conversion reflects a combination of the old analog input and the new input, and the averaged result is an intermediate value.

The next (unaveraged) conversion accurately reflects the new input. However, when averaged with the previous conversion, it does not yet give the final value, thus it produces the second unsettled output. Only the third output is fully settled (see Figure 3).
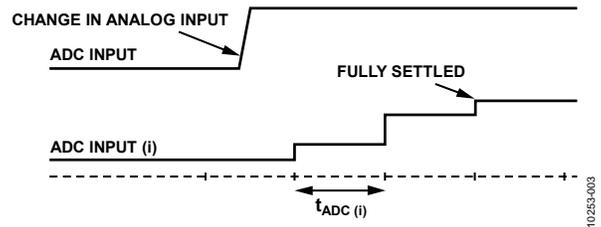

Figure 3. Asynchronous Change in Analog Input Voltage

OUTPUT DATA RATE

These ADCs include a sinc[3] filter and a sinc[4] filter. The filter is selected using the Single bit. The filter order affects the output data rates that are available from the ADC. Consult the AN-1084 Application Note, which discusses the output data rate and set-tling time for the different filter options.

FREQUENCY RESPONSE

Chopping also impacts the frequency response but primarily in a beneficial way. The action of the average by 2 places notches in the response at odd multiples of $f_{ADC}/2$, f_{ADC} being the output data rate. These notches can provide improved 50 Hz/60 Hz rejection. For example, if the output data rate is equal to 12.5 Hz and the sinc[4] filter is selected, the sinc filter places a notch at 50 Hz, whereas the chopping places a notch at 56.25 Hz. The notch at 56.25 Hz provides rejection at 60 Hz.
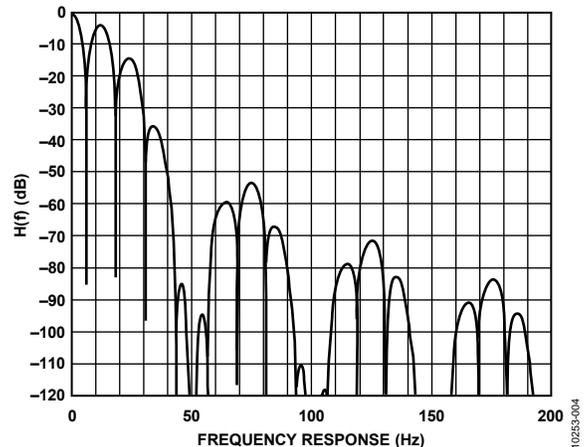

Figure 4. Frequency Response (Sinc4, 12.5 Hz Output Data Rate, REJ60 = 0)).

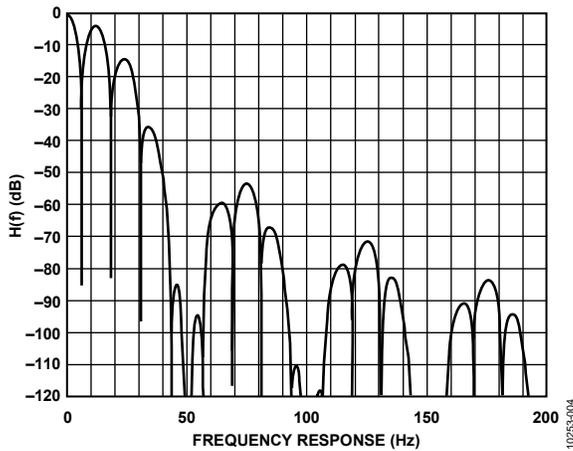If Bit REJ60 is set to 1, a first order notch is placed at 60 Hz, which improves the 50 Hz/60 Hz rejection.

Figure 5. Frequency Response (Sinc⁴, 12.5 Hz Output Data Rate, REJ60 = 1).

Table 1 shows the rejection that is achieved when the sinc³ or sinc⁴ filter is selected for both REJ60 = 0 and REJ60 = 1.

Table 1. Rejection at 50 Hz/60 Hz for Sinc³ and Sinc⁴ Filters

Sinc Filter Order	Sinc³	Sinc⁴
FS[9:0]	96	96
Output Data Rate	16.6 Hz	12.5 Hz
50/60 Hz Rejection (±1 Hz)		
REJ60 = 0	53 dB	63 dB
REJ60 = 1	73 dB	83 dB

RMS NOISE

The averaging performed as part of the chopping improves the rms noise. The noise improves by the square root of 2 which equates to 0.5 LSBs improvement in peak-to-peak resolution and effective resolution.

CONCLUSION

The primary purpose of chopping is the elimination of offset errors. On these ADCs from Analog Devices, Inc., the chopping does an excellent job of removing offsets. In addition, chopping has other benefits such as the improvement in rms noise and the extra notches in the filter response, which can be used for 50/60 Hz rejection.

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