

AD7292 DAC Disable Function Timing

by Norma O'Mahony

INTRODUCTION

The [AD7292](#) contains all the functionality required for general-purpose monitoring of analog signals and control of external devices, integrated into a single-chip solution.

The [AD7292](#) features an 8-channel, 10-bit SAR ADC, four 10-bit DACs, a $\pm 1^{\circ}\text{C}$ accurate internal temperature sensor, and 12 GPIOs to aid system monitoring and control.

DAC outputs VOUT0 to VOUT3 feature an output voltage range up to 5 V (LSB of 4.88 mV). The DAC output buffer can be controlled via software using the GPIO2/DAC DISABLE0 and GPIO4/DAC DISABLE1 subregisters within the configuration register bank, or via hardware using the GPIO2/DAC DISABLE0 and GPIO4/DAC DISABLE1 pins.

This application note describes the timing associated with the DAC disable function of the [AD7292](#).

DAC DISABLE OUTPUT TIMING MEASUREMENT HARDWARE CONFIGURATION

The measurements described in this application note were taken using the [EVAL-AD7292SDZ](#) evaluation board and evaluation software in conjunction with the [EVAL-SDP-CB1Z](#) system demonstration platform board. Refer to [UG-449](#) for detailed setup and software installation instructions.

Evaluation Board Modification

The effects on the DAC disable timing, due to varying the DAC output load capacitance, was examined. To accomplish this, two minor modifications to the [EVAL-AD7292SDZ](#) evaluation board were required. The [EVAL-AD7292SDZ](#) evaluation board Bill of Materials, by default, calls for C13 and C14 to be

unpopulated. Populating these two capacitor spaces allows for load capacitance to be added to VOUT0 and VOUT1. C13 and C14 were populated with 100 pF and 330 pF capacitors, respectively.

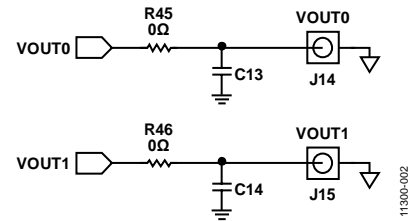


Figure 1. VOUT0 and VOUT1 Load Capacitance Modification (C13 = 100 pF, C14 = 330 pF)

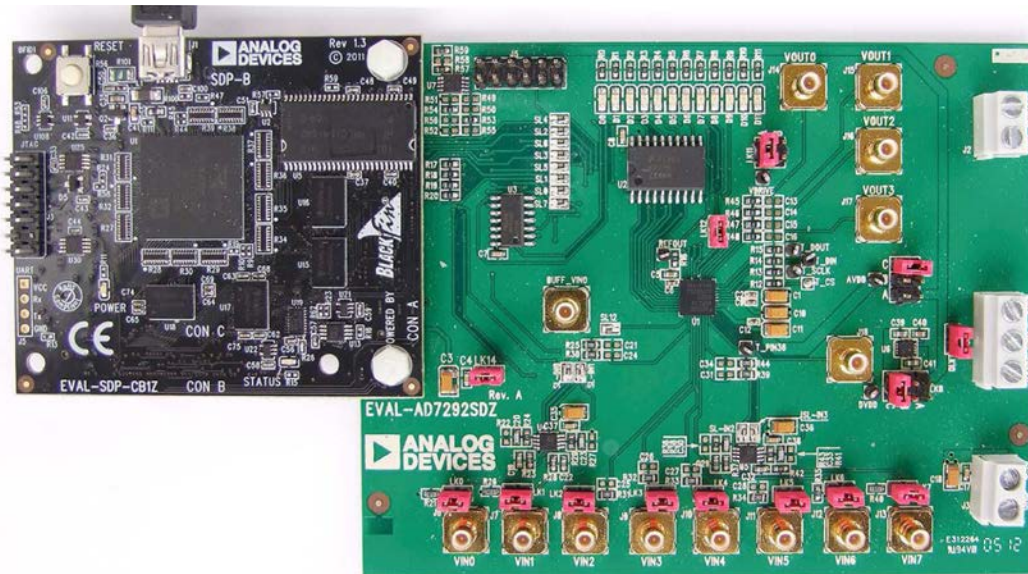


Figure 2. Hardware Configuration—Evaluation Board Setup

SOFTWARE CONFIGURATION

The Registers tab within the evaluation software allows the user to configure the internal AD7292 registers.

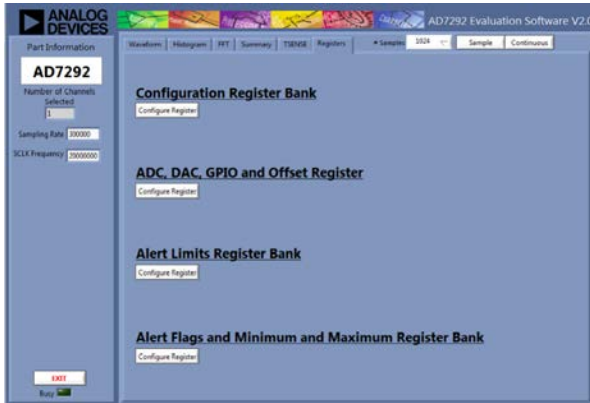


Figure 3. Registers Tab Within EVAL-AD7292SDZ Evaluation Software

**ADC, DAC, GPIO, and OFFSET Register Settings
DAC Buffer Enable Register (0x0A)**

On power up, the DAC output buffers are disabled by default. Bits D0 to D3 are set to 1 to enable the DAC output buffers.

DAC Channel Registers (0x30 to 0x33)

The DAC outputs, VOUT1, VOUT2, and VOUT3 were set to 3 V by writing to Bits[D6:D15] of the DAC Channel Register.



Figure 4. ADC, DAC, GPIO, and OFFSET Register

Configuration Register Bank Settings

GPIO2/DAC DISABLE0 and GPIO4/DAC DISABLE1

The contents of the GPIO2/DAC DISABLE0 register was unchanged, resulting in the DAC DISABLE function being disabled. Once the DAC disable timing was to be examined, Bits[D0:D2] were set, thus disabling the DAC outputs, VOUT0 to VOUT3. The GPIO4/DAC DISABLE1 register could be used to perform the same function.

Note that the default DAC disable mode Control Bits D1 and D2 within the General Sub-Register were unchanged from their default value resulting in a disable mode of 1kΩ and 100 kΩ resistors in parallel to ground.

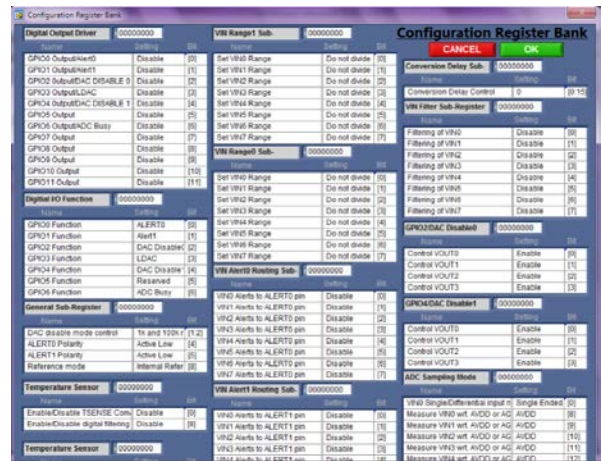


Figure 5. Configuration Register Bank

11300-003

11300-004

11300-005

MEASUREMENT RESULTS

DAC Disable Timing

When the DAC disable timing was to be examined, Bits[D0:D2] of the GPIO2/DAC DISABLE0 register were set to 1, thus disabling the DAC outputs, VOUT0 to VOUT3. The time taken for the DAC outputs to decrease from 3 V to 1 V was captured using a Tektronix TDS 3054 oscilloscope (see Figure 6).

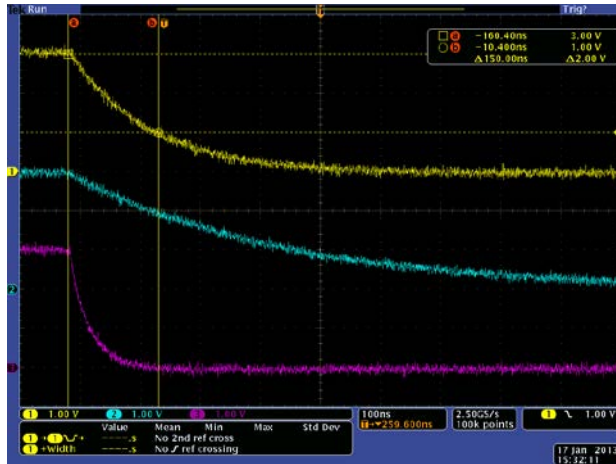


Figure 6. DAC Disable Timing Oscilloscope Plot

Table 1. DAC Disable Timing

DAC Output	Load Capacitance	Oscilloscope Trace	Time for VOUTx to Decrease from 3 V to 1 V (Typ)
VOUT0	100 pF	Yellow	150 ns
VOUT1	330 pF	Blue	380 ns
VOUT2	0 pF	Pink	40 ns

DAC Enable Timing

For completeness, the timing in the reverse direction was also measured. The DAC outputs were reenabled by writing 0 to Bits[D0:D2] of the GPIO2/DAC DISABLE0 register. The time taken for the DAC outputs to increase from 1 V to 3 V was captured (see Figure 7).

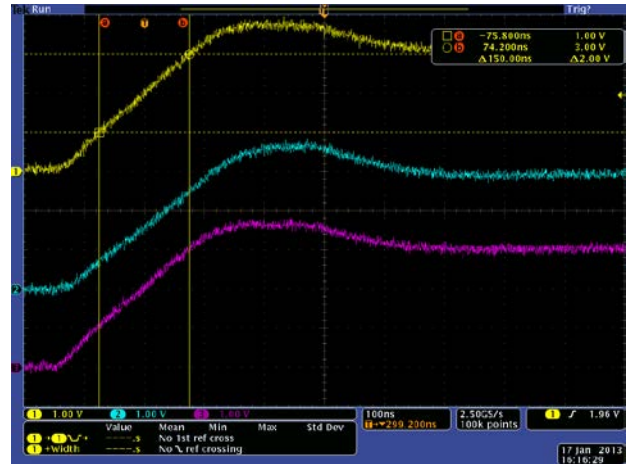


Figure 7. Reverse Timing

Table 2. DAC Enable Timing

DAC Output	Load Capacitance	Oscilloscope Trace	Time for VOUTx to Decrease from 3 V to 1 V (Typ)
VOUT0	100 pF	Yellow	150 ns
VOUT1	330 pF	Blue	164 ns
VOUT2	0 pF	Pink	150 ns

REVISION HISTORY

2/13—Revision 0: Initial Version