AN-1361
APPLICATION NOTE

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AD7293 Closed-Loop for Power Amplifier Drain Current Control

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INTRODUCTION

The AD7293 from Analog Devices, Inc., includes four complete closed-loop power amplifier (PA) drain current controllers on one chip. It offers functionality for monitoring and control of current, voltage, and temperature integrated into a single lead frame chip scale package (LFCSP) solution that is serial port interface (SPI) compatible.

The device features a 4-channel, 12-bit successive approximation register (SAR), analog-to-digital converter (ADC), eight 12-bit digital-to-analog converters (DACs) (four bipolar and four unipolar with configurable output ranges), a ±1.25°C accurate internal temperature sensor, and eight general-purpose input/output (GPIO) pins. The device also includes limit registers for alarm functions and four high-side current sense amplifiers to measure current across external shunt resistors. These amplifiers can be optionally set to operate as part of four independent closed-loop drain current controllers.

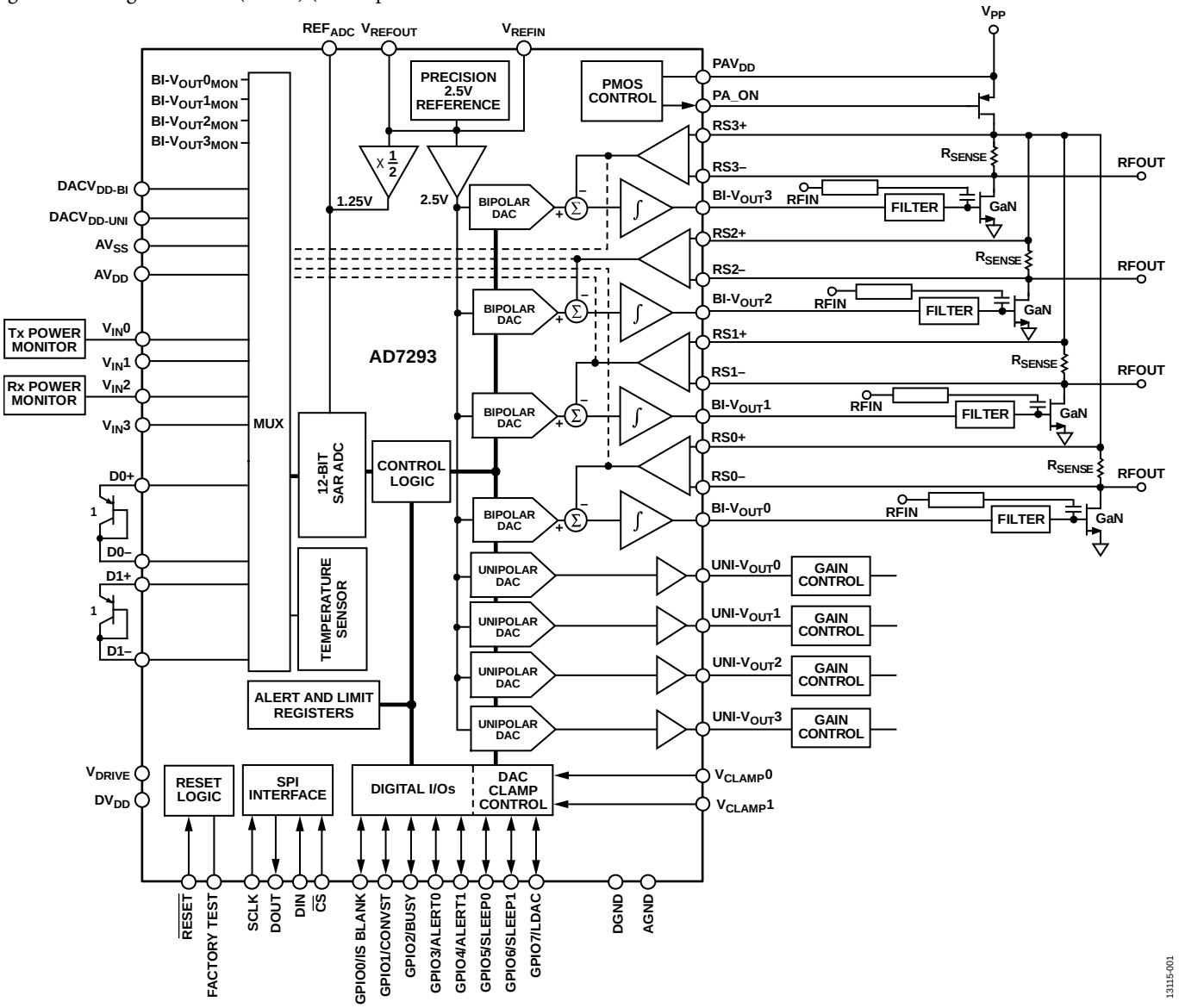

Figure 1. Typical High Power Amplifier (HPA) Monitor and Control Application Diagram

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REVISION HISTORY

9/2016—Revision A: Initial Version

CLOSED-LOOP CURRENT CONTROL

A high accuracy, 2.5 V internal reference is provided to drive the DACs and the ADC. The 12-bit ADC monitors and digitizes an internal temperature sensor, and two inputs for external diode temperature sensors are included.

The bipolar DACs, as well as the four current sensors in the AD7293, can be configured to operate as four independent closed-loop drain current controllers. The bipolar DAC sets the power amplifier (PA) current, and it maintains this constant current. The BI-V_{OUT}2 pin creates a loop with RS2+ and RS2−, for example. Changes in current are seen as a voltage across the current sense resistor, and the current sense amplifier voltage is fed back to the summing amplifier. The current sense amplifier voltage is compared against the DAC voltage and, if there is an error, the integrator resolves the output of the device, adjusting the gate voltage of the external PA until the error in the loop is zero.

Follow the defined power-up sequence in the AD7293 data sheet to ensure the PA is protected during power-up and that registers are used to tune the loop function. This application note is an in depth exploration of the configuration options for the AD7293 closed-loop mode.

The measurement results, simulations, and guidelines are provided to assist radio designers in making decisions about the configuration of the AD7293, as well as making choices about the external circuitry. The HMC1099 gallium nitride (GaN) broadband power amplifier is referenced as the PA.

CLOSED-LOOP CONSIDERATIONS

The AD7293 contains circuitry to implement closed-loop control of the drain current in an RF power amplifier. This circuitry consists of the following:

- A DAC to define the target current, represented as a voltage, V_{SET}, between 0 V and 1.25 V
- A summing node to calculate the difference between the target current and the actual current
- An integrator, with programmable time constant, τ_I
- A current sense amplifier to measure the voltage, V_{SENSE}, across a sense resistor, R_S, located in series with the PA drain

At the gate of the PA, a network is required to combine the low frequency bias signal generated by the integrator with the high frequency radio frequency (RF) signal. The current control loop is represented by a low-pass filter with time constant as follows:

$$R_G C_G = \tau_G$$

where τ_G is typically in the range of 5 µs ≤ τ_G ≤ 50 µs.

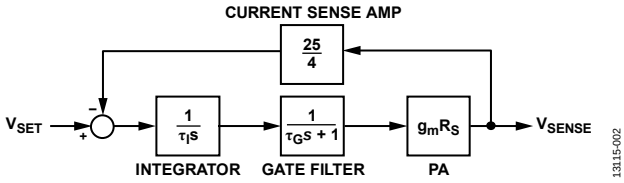

Figure 2. Diagram of System

From Figure 2, the closed-loop transfer function can be determined using the following equation:

$$V_{SENSE} = \frac{4g_m R_S}{4\tau_I \tau_G s^2 + 4\tau_I s + 25 g_m R_S} V_{SET}$$

where g_m is the transconductance of the PA.

To extract the damping ratio, ζ, use the following equation:

$$\zeta = \sqrt{\frac{\tau_I}{25 g_m R_S \tau_G}}$$

To achieve critical damping (ζ = 1, the fastest possible settling with no overshoot), use the following equation:

$$\tau_I = 25 g_m R_S \tau_G$$

If a damping ratio of less than 1 is chosen, use the following equation to predict the overshoot:

$$overshoot\,(\%) = 100e^{\left(\frac{-\zeta\pi}{\sqrt{1-\zeta^2}}\right)}$$

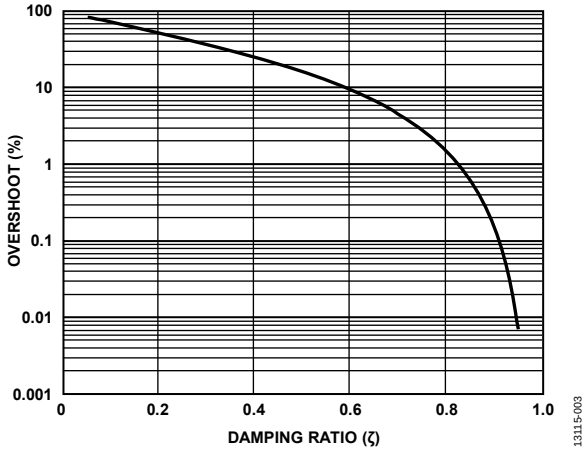

Figure 3. Overshoot vs. Damping Ratio for a Second-Order System

R_{SENSE} SELECTION

The steady state value of V_{SENSE} is given by the following equation:

$$V_{SENSE} = (4/25)V_{SET}$$

Therefore, for the maximum value of V_{SET}, 1.25 V, V_{SENSE} = 0.2 V.

V_{SENSE} sets an upper limit on the value of R_S.

$$R_S \leq 0.2/I_{DS(MAX)}$$

where $I_{DS(MAX)}$ is the drain current at the maximum required PA gain.

In some cases, it may be desirable to choose a smaller value for R_S, for the following benefits:

- Reduced power dissipation in the sense resistor
- Improved loop dynamics
- Common sense resistor value for multiple PA types
- Design margin to guarantee that maximum gain can always be reached

However, these benefits are at the expense of dynamic range and setpoint resolution.

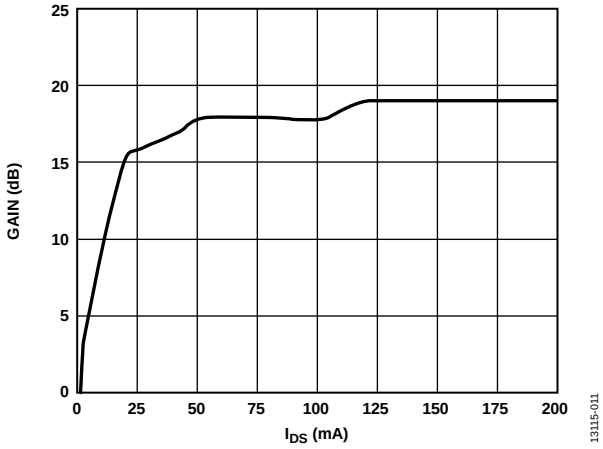

Figure 4. PA Gain vs. Drain Current (I_{DS}) of HMC1099 PA

PA TRANSCONDUCTANCE

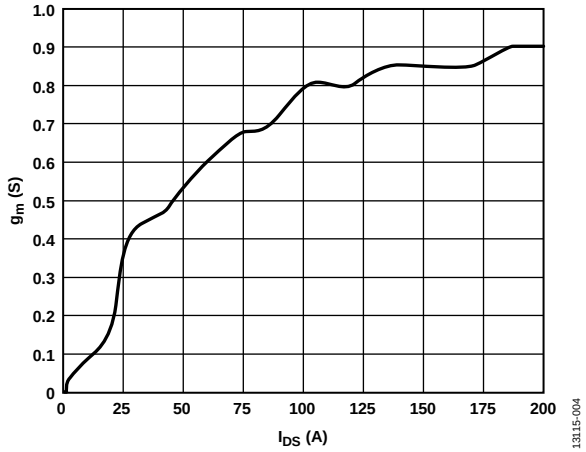

Figure 5. PA Transconductance (g_m) vs. Drain Current (I_{DS}) of HMC1099 PA

The transconductance of the PA varies as a function of drain current. In terms of loop damping, the worst case is when g_m is highest. Therefore, after the maximum PA gain required is determined, use the value of g_m at this gain to select τ_I.

WORKED EXAMPLE

Using the example of Figure 4, set the gain to a maximum of 18.5 dB. The gate filter network has a time constant, τ_G, of 30 µs.

$$I_{DS\,(18.5dB)} = 0.1 \text{ A}$$

Therefore, select R_S as follows:

$$R_S = 0.2/0.1 = 2\ \Omega$$

Based on Figure 5,

$$g_{m\,(18.5dB)} = 0.8 \text{ S}$$

This equation gives a target value for τ_I as follows:

$$\tau_I = 25 g_m R_S \tau_G$$

$$\tau_I = 25 \times 0.8 \times 2 \times 30\ \mu s$$

$$\tau_I = 1.2 \text{ ms}$$

Table 1 shows the settings available in the AD7293.

Table 1. Integrator Time Constant vs. Overshoot

Code	Integrator Time Constant (τ_I)	Calculated Damping Ratio for This Example	Overshoot (%)
1	2.352 ms	1.4	0.0
2	1.218 ms	1.01	0.0
3 (default)	840 µs	0.84	0.77
4	650 µs	0.74	3.15
5	538 µs	0.67	5.87
6	462 µs	0.62	8.35
7	408 µs	0.58	10.68

The default setting for τ_I of Code 3 (840 µs) results in an overshoot of 0.77% for a step change in setpoint, which is typically acceptable. If no overshoot is required, implement any of the following actions:

- Reduce R_S to 1.4 Ω (reduced dynamic range, setpoint resolution)
- Choose τ_I of Code 2 for slower settling (see Table 1)
- Change the gate filter to give τ_G = 21 µs (increased noise from control loop)

ADDING A THIRD POLE

It may be useful to add a filter at the input to the current sense amplifier to reject high frequency disturbances (see Figure 6).

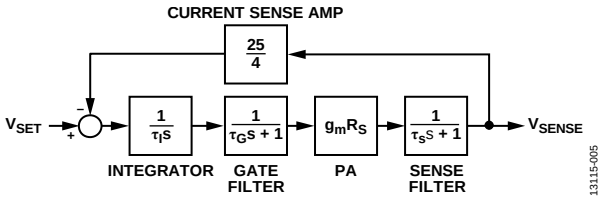

Figure 6. Current Control Loop with Additional Filter at Current Sense Input

The resulting transfer function is

$$V_{SENSE} = \frac{4g_m R_S}{4\tau_I \tau_G \tau_S s^3 + 4\tau_I (\tau_G + \tau_S) s^2 + 4\tau_I s + 25 g_m R_S} V_{SET}$$

For an existing two-pole system with $\zeta = 1$, set $\tau_S \leq (1/10)\tau_G$ to avoid affecting the loop response.

Use a computer simulation to predict the effect of adding a third pole.

Based on the values chosen in the Worked Example section, Figure 7 shows a transient simulation of the effect of the sense filter, for a step change of V_{SET} from 0 V to 1 V.

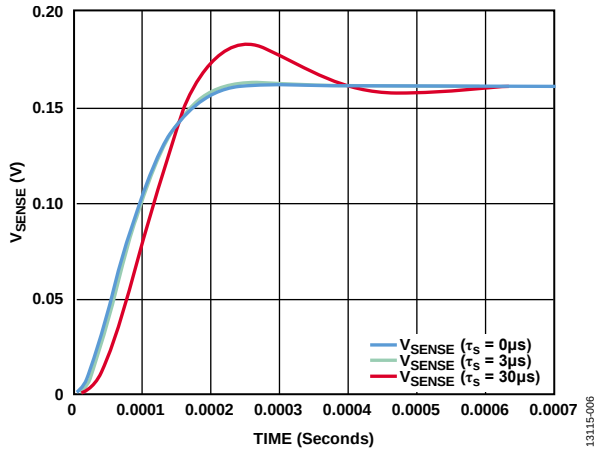

Figure 7. Overshoot Introduced by Third Pole at Current Sense Input

CLOSED-LOOP UPDATE RATE

The preceding analysis in the Worked Example section assumes that all the components in the loop operate in continuous time. In the AD7293, the current sense amplifier and integrator sample their inputs with a period of 16.8 µs. This sampling results in the voltage at the integrator output consisting of discrete steps, which can be observed as a tone of frequency, 1/16.8 µs ≈ 60 kHz, during V_{SENSE} transitions. This tone can be reduced in amplitude by the gate filter, so that it does not affect the PA output.

The sampling introduces a criterion for loop stability, even with only two poles in the loop.

$$\tau_I / g_m R_S > 52.5\ \mu s$$

where:

$\tau_I = 840$ µs.

$g_m = 0.8$.

$R_S = 2\ \Omega$.

Therefore, $\tau_I / g_m R_S = 840/0.8 \times 2 = 525$ µs.

POWER AMPLIFIER GATE CURRENT CONSIDERATIONS

The gate current of the power amplifier is a function of the drive level. Typically, the gate current increases close to compression if the radio is running at 6 dB from compression. In normal operation, gate currents of greater than 2 mA are not expected in either direction for output powers less than 1 dB compression point (P1dB) minus 6. The AD7293 can comfortably supply this level of current.

The AD7293 can source current, but it is important to note that the gate current changes as a function of the compression level, and this must be kept in mind when characterizing the radio.

Power dissipation must be considered at high current levels, such as 20 mA × 5 V × 4 channels = 400 mW. The AD7293 package has a θ_{JA} of 27°C/W.

The bipolar DAC output channels are capable of providing a significant amount of current to the gate of the power amplifier while also maintaining linearity performance, as shown in Figure 8, when the power amplifier is running close to compression. However, take care to ensure the system functions as expected.

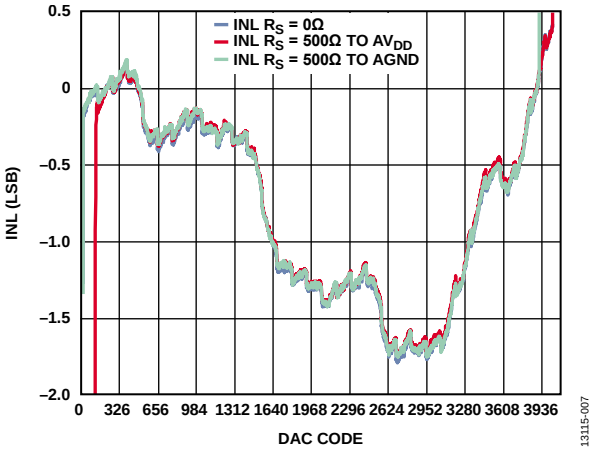

Figure 8. Bipolar DAC Integral Nonlinearity (INL), R_S = 500 Ω to AV_{DD}, 0 Ω, and 500 Ω to AGND

CLAMPING AND PROTECTION

A protection circuit is implemented that clamps the bipolar DAC voltage outputs to −5 V (AV_{SS}) when the 5 V supply fails. Typically, the trip point is between 3.5 V and 4 V. This clamp switch has a 500 Ω to 600 Ω resistance associated with it. Consider this resistance when examining the PA drain current considerations.

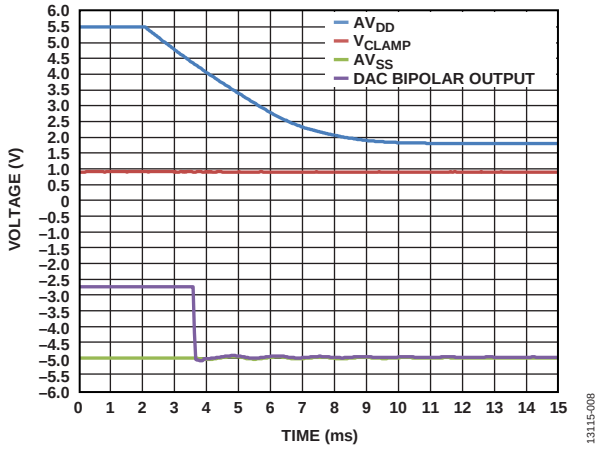

Figure 9. Bipolar DAC Output on Removing AV_{DD}

On the AD7293, the bipolar DAC outputs are clamped to −3 × $V_{CLAMP}x$ during power-up. This clamp ensures that when the AD7293 controls a depletion mode device, the PA is not turned on to full power when the AD7293 is powered up. Figure 10 shows the typical settling time for the bipolar DAC output to clamp. Figure 11 shows the typical settling time for the bipolar DAC output to wake up from clamping.

This protection mechanism can also be triggered to protect the device in the event of a fault via a digital GPIOx/SLEEPx pin or triggered internally via an internal alert when limits are exceeded.

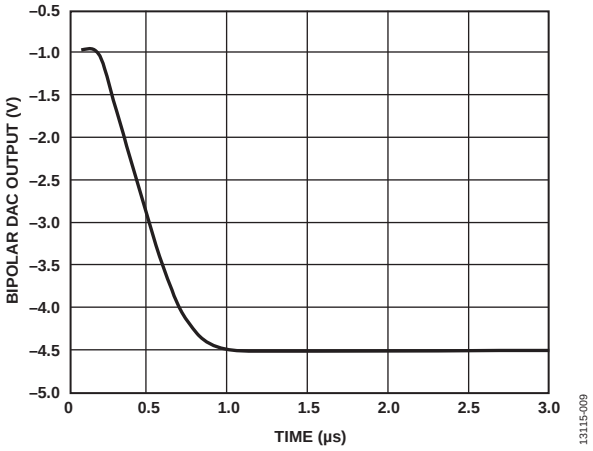

Figure 10. Closed Loop to Clamp Settling Time, $V_{CLAMP}x$ = 1.5 V

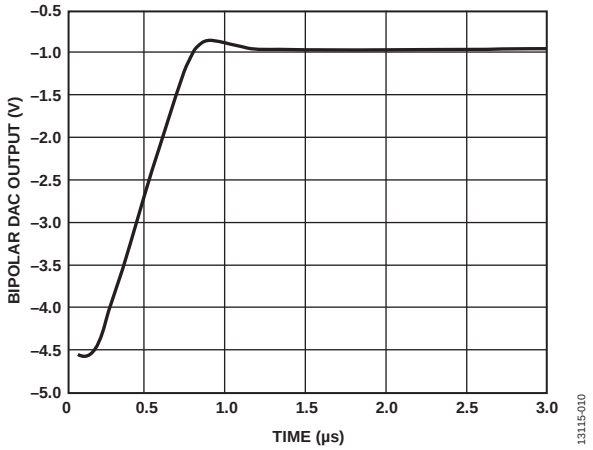

Figure 11. Wake Up from Clamp Settling Time, $V_{CLAMP}x$ = 1.5 V

POWER-UP SEQUENCING

See the AD7293 data sheet for instructions on which registers to write to during power-up to protect the PA.

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