ANALOG DEVICES

AN-284
APPLICATION NOTE

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Implement Infinite Sample-and-Hold Circuits Using Analog Input/Output Ports

by Mike Byrne

Sample-and-hold circuits are used in a variety of applications where the status of a parameter at a particular point in time needs to be acquired and held for some time after the measurement instant. The term infinite sample-and-hold is given to sample-and-hold circuits that are required to hold the acquired signal for a relatively long period of time. This type of circuit is particularly useful in monitoring changes in parameters over periods of time versus a fixed or "held" reference level. This reference level may be updated occasionally, hence the need for the sample-and-hold function. It is also useful in peak-detecting circuits where the held output provides an analog representation of the peak analog input voltage. This application note discusses the use of three 8-bit analog input/output ports, the AD7569, AD7669 and AD7769, in the implementation of infinite sample-and-hold circuits.

The block diagram for the AD7569 is shown in Figure 1, while the block diagram for the AD7669 is shown in Figure 2. The AD7769 block diagram is illustrated in Figure 3. The AD7569 contains on-chip track/hold, reference, buffer amplifiers as well as an 8-bit DAC and an 8-bit ADC. The AD7669 is similar but contains two DACs and one ADC. The AD7769 has two input channels and two output channels. The AD7569 and AD7669 operate from a single +5 V supply or from ±5 V supplies, while the AD7769 operates from +5 V and +12 V supplies. For more detailed information on these parts, see Table I and consult the respective data sheets.

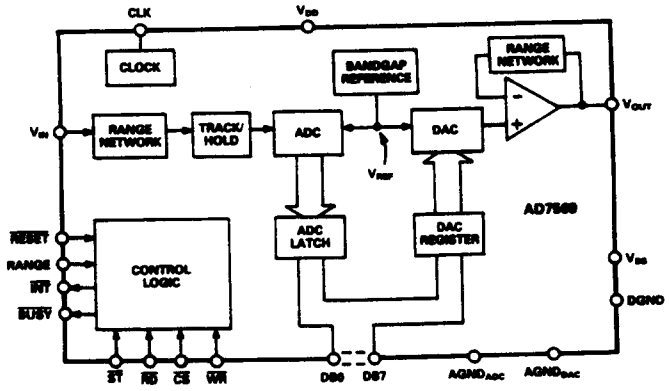


Figure 1. AD7569 Functional Block Diagram

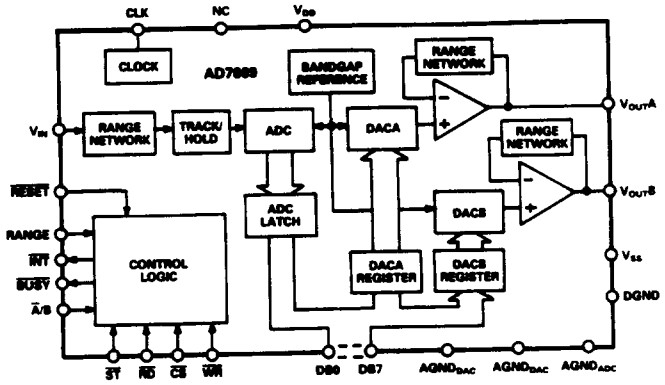


Figure 2. AD7669 Functional Block Diagram

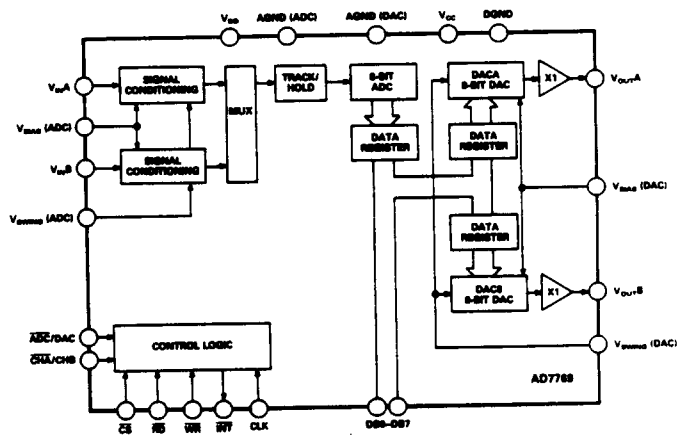


Figure 3. AD7769 Functional Block Diagram

PRINCIPLE OF OPERATION

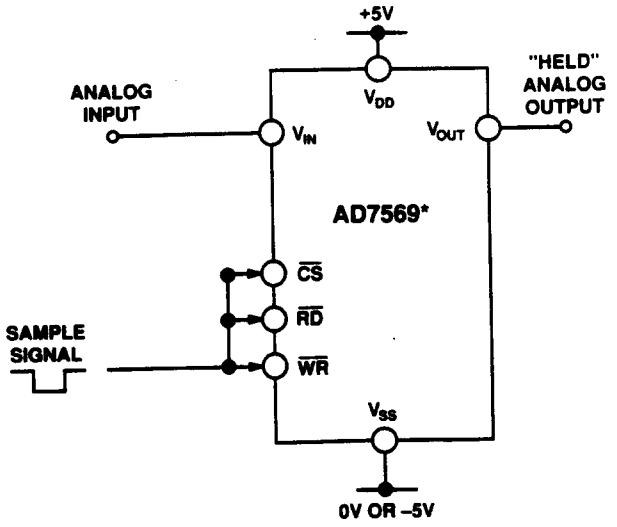
The basic principle of operation of the infinite sample-and-hold circuits described here is the same regardless of which part is used to implement the function. The input signal to be held is converted to digital form using the on-chip track/hold and ADC. This digital data is restored to analog form using the associated DAC contained on the same chip. This scheme has a number of advantages over traditional schemes which store the value on a hold capacitor. Firstly, because the stored voltage is recreated using a DAC, the circuit does not suffer from any droop problems associated with storing voltages on capacitors for relatively long periods of time. Additionally, the entire sample-and-hold circuit comes in a single dual-in-line package with no external components required to implement the basic sample-and-hold function. Also, when the circuit is not being used for the sample-and-hold function, it provides a DAC and ADC function for the user.

INPUT/OUTPUT CHANNELS

The AD7569, AD7669 and AD7769 allow a number of different input and output voltage ranges, operate from different power supplies and contain different numbers of input/output channels. Table I provides a quick reference as to the differences between the parts to allow selection of the one most suitable for a particular application.

SINGLE-CHANNEL INFINITE SAMPLE-AND-HOLD USING AD7569

The circuit of Figure 4 illustrates the implementation of a single-channel infinite sample-and-hold circuit using the AD7569. No additional components are required to implement the function with the AD7569. The external sample signal drives the $\overline{CS}$, $\overline{RD}$ and $\overline{WR}$ inputs of the AD7569 (see timing diagram in Figure 5). The input signal is held and the ADC conversion is initiated on the falling edge of $\overline{CS}$ and $\overline{RD}$. Data from a previous conversion is output to the data bus. The $\overline{WR}$ input is also low



*ADDITIONAL PINS OMITTED FOR CLARITY

Figure 4. Single-Chip, Single-Channel, Infinite Sample-and-Hold Using AD7569

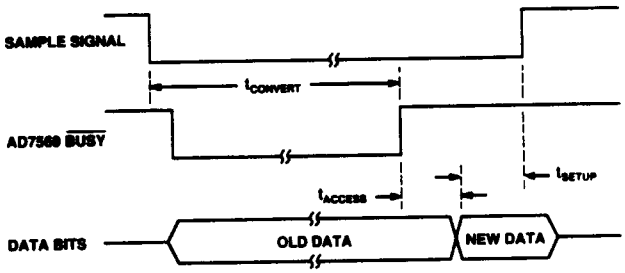


Figure 5. Timing Diagram for Circuit of Figure 4

	AD7569	AD7669	AD7769
Power Supplies	+5 V or ±5 V (for Bipolar Ranges)	+5 V or ±5 V (for Bipolar Ranges)	+5 V and +12 V
No. of Input Channels	1	1	2
No. of Output Channels	1	2	2
Input Voltage Ranges	0 to +1.25 V, 0 to +2.5 V, ±1.25 V, ±2.5 V	0 to +1.25 V , 0 to +2.5 V, ±1.25 V, ±2.5 V	V_{BIAS} (ADC) ± V_{SWING} (ADC)*
Output Voltage Ranges	Same as Input Ranges	Same as Input Ranges	V_{BIAS} (DAC) ± V_{SWING} (DAC)**
Conversion Time	2 µs	2 µs	2.6 µs

*V_{BIAS} (ADC) voltage range is +2 V to +6.8 V; V_{SWING} (ADC) voltage range is +2 V to +3 V.
**V_{BIAS} (DAC) voltage range is +3 V to +6.8 V; V_{SWING} (DAC) voltage range is +2 V to +3 V.

Table I. Selection Table

at this point, but since the $\overline{WR}$ input is rising edge triggered no data is written to the DAC register and nothing happens to the DAC output at this time. When the conversion is complete, data from the conversion is placed on the data bus; the sample signal is then brought high and data from the conversion is latched to the DAC register on the rising edge of $\overline{WR}$. The sample signal must be as long as the ADC conversion time plus the ADC data access time plus the data setup time required by the DAC register. Operating at +25°C means that the AD7569 requires a sample pulse of 2.12 μs. This is the effective acquisition time of the infinite sample-and-hold function, i.e., the time it takes the infinite sample-and-hold to acquire a new sample. This should not be confused with the acquisition time of the track/hold on the AD7569 which starts when $\overline{BUSY}$ goes high and is 200 ns typical.

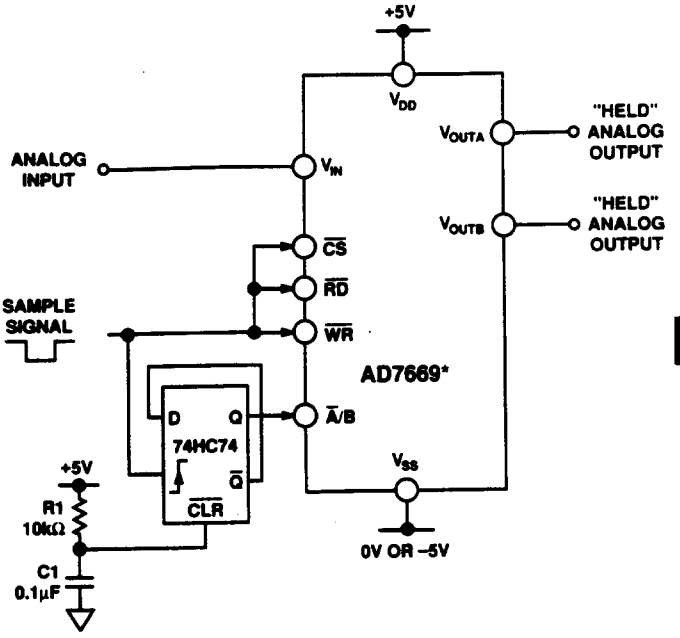
The output from the DAC provides a low impedance output voltage source which corresponds to the sampled analog input. The output voltage will be held until the DAC register is updated. The full-scale matching between the ADC and DAC ensures a typical error of less than 1% between the analog input voltage and the "held" output voltage. If necessary, the gain and offset differences can be adjusted out during initialization or calibration cycles by adjusting the ADC offset and full-scale errors using an external op amp.

Using an external gate on the $\overline{WR}$ input, the ADC can continue to provide an A/D function while the held analog value is maintained on the DAC output. This gate would only allow the $\overline{WR}$ input to become active when the DAC output is to be updated with a new sampled value.

DUAL-OUTPUT-CHANNEL INFINITE SAMPLE-AND-HOLD USING AD7669

A similar scheme is used to implement an infinite sample-and-hold function using the AD7669 (see Figure 6). This time there are two output channels to which the digital data can be transferred. Selection of the output to be updated is achieved using the $\overline{A}$/B input of the AD7669. In the circuit of Figure 6, each successive conversion is stored to alternate DAC registers, i.e., the first to DAC A register, the second to DAC B register, the third to DAC A, and so on. Updating of the $\overline{A}$/B line takes place at the end of conversion on the rising edge of the sample input. A power-on reset on the 74HC74 (R1 and C1 in Figure 6) ensures that the first conversion result is stored in the DAC A register. An alternative method is to use an external control line to drive the A/B input which allows flexibility in choosing which output the conversion result is to be transferred to.

The timing requirements for the incoming sample pulse are similar to those outlined for the AD7569. The sample pulse width must again be as long as the ADC conversion time plus the ADC data access time plus the DAC register data setup time, resulting in an acquisition of 2.12 μs for the infinite sample-and-hold function.



*ADDITIONAL PINS OMITTED FOR CLARITY

Figure 6. Infinite Sample-and-Hold Using AD7669

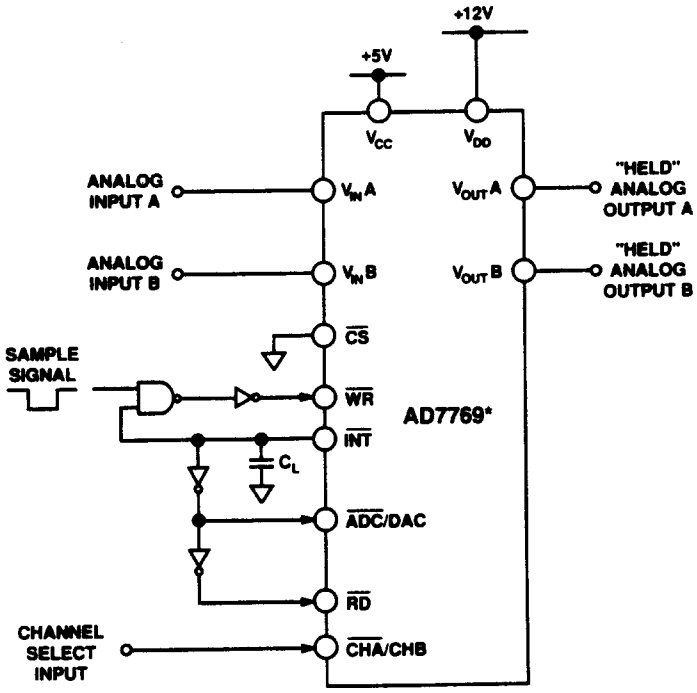
DUAL-CHANNEL INFINITE SAMPLE-AND-HOLD USING AD7769

The control logic required to turn the AD7769 into an infinite sample-and-hold differs slightly from those outlined for the AD7569 and AD7669. Unlike the previous cases where the same signal is used to drive the $\overline{RD}$ and $\overline{WR}$ signals of the part, separate signals must be generated here because the AD7769 $\overline{WR}$ input controls both the ADC conversion start and DAC register updates. The $\overline{ADC}$/DAC control input determines whether a DAC write or a conversion start takes place when $\overline{WR}$ is active. The $\overline{WR}$ line, therefore, must be pulsed twice in the infinite sample-and-hold application, first to initiate conversion on the ADC and second to transfer data to the DAC register. The $\overline{RD}$ signal to activate the ADC latches must be generated when conversion is complete. The $\overline{INT}$ output of the AD7769, which becomes active when conversion is complete, is used to generate this $\overline{RD}$ signal. Figure 7 shows the circuit used to configure the AD7769 as a dual infinite sample-and-hold.

The timing diagram for the circuit is shown in Figure 8. When the input sample signal is pulsed low, the $\overline{WR}$ input of the AD7769 goes low two gate delays later; and since the $\overline{ADC}$/DAC input is low, conversion is initiated on the rising edge of this signal. $\overline{INT}$ goes low when conversion is complete. One gate delay later, the $\overline{ADC}$/DAC line goes high; and a further gate delay later, the $\overline{WR}$ and $\overline{RD}$ inputs go low. $\overline{RD}$ going low places data on the data bus, and this data is written to the respective DAC register on the rising edge of $\overline{WR}$. $\overline{INT}$, and hence $\overline{RD}$ and $\overline{WR}$, is driven high by $\overline{RD}$ going low. The delay between $\overline{RD}$ and $\overline{INT}$ is dependent on the capacitance on the $\overline{INT}$ pin (C_L in Figure 7). A capacitor in the range 50 pF to 100 pF guarantees a $\overline{WR}$ pulse width which

gives sufficient time for the ADC data access time plus the DAC register data setup time. The $\overline{ADC}$/DAC line returns low one gate delay before the $\overline{WR}$ line goes high when writing data to the DAC register. However, internal delays on the AD7769 ensure that data is written correctly to the DAC register. The resulting acquisition time for the infinite sample-and-hold is a sum of the ADC conversion time plus the ADC access time plus the DAC register setup time (the time from the sample input going high to the AD7769 $\overline{WR}$ and $\overline{RD}$ inputs going high). In the circuit of Figure 7, the width of the AD7769 $\overline{WR}$ and $\overline{RD}$ pulses varies slightly with value of C_L giving slight variations in the acquisition time which is typically 2.75 μs.

The AD7769 contains two input ADC channels and two output DAC channels. Selection of either of the DAC channels (or either of the ADC channels) is achieved using the $\overline{CHA}$/CHB input. This input is driven from an external control line and should not change for the duration of the ADC conversion and the DAC update. As a result $V_{OUT}A$ will hold the $V_{IN}A$ signal while $V_{OUT}B$ will represent the input voltage on $V_{IN}B$.



*ADDITIONAL PINS OMITTED FOR CLARITY

Figure 7. Dual Infinite Sample-and-Hold Using the AD7769

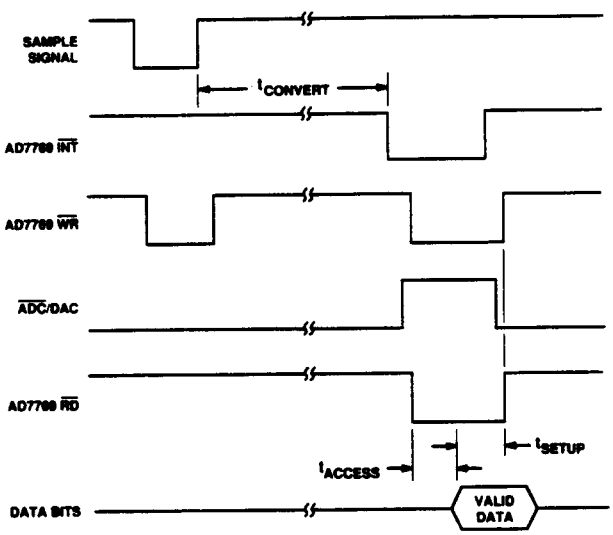


Figure 8. Timing Diagram for Circuit of Figure 7