AN-793
APPLICATION NOTE

One Technology Way • P.O. Box 9106 • Norwood, MA 02062-9106, U.S.A. • Tel: 781.329.4700 • Fax: 781.461.3113 • www.analog.com

ESD/Latch-Up Considerations with *i*Coupler Isolation Products

by Rich Ghiorse

INTRODUCTION

Analog Devices, Inc., *i*Coupler® products offer an alternative isolation solution to optocouplers with superior integration, performance, and power consumption characteristics. An *i*Coupler isolation channel consists of CMOS input and output circuits and a chip scale transformer (see Figure 1). Because digital isolators employ CMOS technology, they can be vulnerable to latch-up or electrostatic discharge (ESD) damage during system-level ESD, surge voltage, fast transient, or other overvoltage conditions.

This application note provides guidance for avoiding these problems. Examples are presented for various system-level test configurations showing mechanisms that may impact performance. For each example, recommended solutions are given.

COMPONENTS vs. SYSTEMS

Simply put, a component is a single integrated device with interconnects while a system is a nonintegrated device built from several interconnected components. In almost all cases, the distinction between a component and a system is obvious. However, the differences between component and system tests may not be so obvious. Further, component specifications may not directly indicate how a device will perform in system-level testing. ESD testing is a good example of this.

ESD, surge, burst, and fast transient events are facts of life in electronic applications. These events generally consist of high voltage, short duration spikes applied directly or indirectly to a device. These events arise from interaction of the device to real-world phenomena, such as human contact, ac line perturbations, lightning strikes, or common-mode voltage differences between system grounds.

Component-level ESD testing is most useful in determining a device's robustness to handling by humans and automated assembly equipment prior and during assembly into a system. Component-level ESD data is less useful in determining a device's robustness within a system subjected to system-level ESD events. There are two reasons for this.

- System- and component-level ESD testing have different objectives. Component-level testing seeks to address conditions typically endured during component handling and assembly. System-level testing seeks to address conditions typically endured during system operation.
- The specific conditions a component is subjected to during system-level testing can be a strong function of the board/module/system design in which it resides. For example, long inductive traces between a system and component ground can actually impose a more severe voltage transient onto a component than is imposed on the system at the test point.

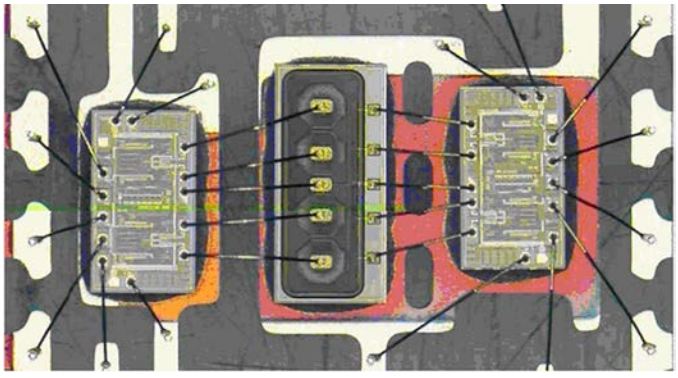

Figure 1. Quad Isolator

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REVISION HISTORY

8/14—Rev. 0 to Rev. A

Changes to Introduction Section 1
Changes to Injected ESD Current Section 5
Changes to Table 3 8

7/06—Revision 0: Initial Version

TEST RESULTS

Table 1 summarizes the ESD test results for the ADuM1400/ADuM1401/ADuM1402 quad isolator. One might conclude from Table 1 that these digital isolators can only be used in systems with ESD ratings of < 4 kV. In reality, it is quite common for these products to be used in systems that pass 15 kV ESD levels per IEC 61000-4-2.

The difference is in the test methods:
The component-level tests call for direct application of ESD events to the pins or body of an unpowered device, while system-level tests call for application ESD events to various locations in the system accessible to external ESD occurrences. Furthermore, the specific waveforms used in component-level and system-level testing differ.

Table 1. ADuM1400/ADuM1401/ADuM1402 ESD Test Results[1]

ESD Model	First Pass Voltage (V)	First Fail Voltage (V)
Human Body Model	3,500	4,000
Field Induced Charge Device Model	1,500	2,000
Machine Model	200	400

[1] For complete information on Analog Devices ESD testing, refer to the Analog Devices Reliability Handbook.

To accurately predict the performance in a system, the designer needs to understand the nature of the system tests and weigh how they impact the product at the component level. Table 2 lists common system-level tests used in isolated applications. Several examples of these tests are discussed in the IEC 610000-4-5 ESD Testing, IEC 610000-4-2 Surge Testing, and IEC 610000-4-4 Transient ad Burst Testing Examples sections.

Table 2. Common System Tests Used in Isolated Applications

Test Standard	Purpose	Test Voltage (V rms)[1]
IEC 61000-4-2	ESD	2,000 to 15,000
IEC 61000-4-4	Fast Transient/Burst	500 to 4,000
IEC 61000-4-5	Surge	500 to 4,000

[1] IEC 61000-4 tests include compliance levels; the test voltages shown are the ranges for level 1 (lowest) through level 4 (highest) compliance.

CIRCUIT MODEL FOR ANALYZING SYSTEM TEST PERFORMANCE

Figure 2 shows a circuit model of a digital isolator, which is useful to understand the impact of system-level testing. The L1, L2, L3, and L4 inductors are due largely to package pins and bond wires, while Capacitor C1 is due to the stray capacitance across the isolation barrier. The inductance values are approximately 0.2 nH. The capacitance value is approximately 0.3 pF per isolation channel.

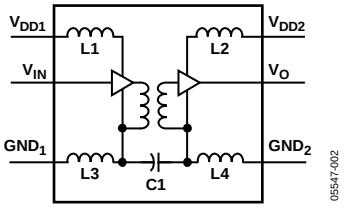

Figure 2. Circuit Model Useful in Analyzing System Designs

LATCH-UP IN CMOS DEVICES

Inherent in a CMOS process are parasitic PNP and NPN transistors configured as silicon control rectifiers (SCR). Latch-up is a condition that comes about when this parasitic SCR is triggered. This causes a low resistance to appear from V_{DD} to ground, and a subsequent large current to be drawn through the device. This excessive current lays open the possibility of damage due to electrical overstress (EOS).

Damage caused by latch-up can range from complete destruction of the device to parametric degradation. More insidious are latent failures that could affect operation later in a system's lifetime. An excellent treatise on the subject of latch-up in general can be found in the *Analog Dialogue* 35-05 (2001) article, "Winning the Battle Against Latch-Up in CMOS Switches." While this article specifically addresses problems with CMOS switches, it is generally applicable to all CMOS devices, including digital isolators.

The use of ceramic bypass capacitors to minimize supply noise between V_{DD} and ground is highly recommended in all applications. Choose capacitors with a value between 0.01 µF and 0.1 µF and place them as close as possible to the device. Even with adequate bypassing, latch-up problems may still occur in some applications. Placing a 200 Ω resistor in series with V_{DD} is also helpful. This limits the supply current to 25 mA in 5 V applications, which is below the latch-up trigger current. However, depending on the supply current being drawn, this series resistance can reduce the supply voltage at the device pin to an unacceptable level. This is most likely to be a concern when operating at high data rates that involve high supply currents.

Usually the mechanism that causes latch-up is an overvoltage condition beyond the part's absolute maximum rating (>7.0 V or <–0.5 V for most products). Once a device is integrated into a system the source of the overvoltage is not always clear. However, it is usually manageable once understood.

IEC 61000-4-2 ESD TESTING

A block diagram of the IEC 61000-4-2 ESD test is shown in Figure 3. In this test, ESD contact or air discharges are applied at various points on a system chassis. This gives rise to several mechanisms that can cause latch-up problems. These include injected current via one of the grounds as well as inductive coupling from ESD currents in the system chassis or in printed wiring board traces.

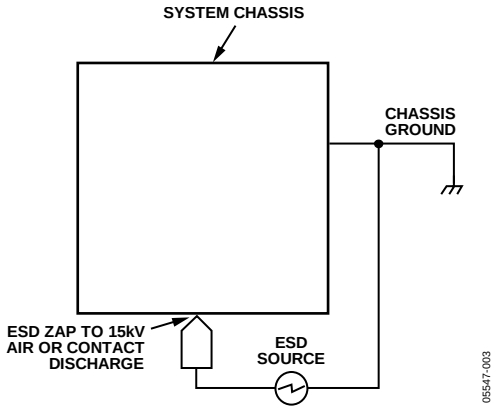

Figure 3. IEC 61000-4-2 ESD Test

INJECTED ESD CURRENT

The first possible mechanism for latch-up is one in which excessive ESD current is injected into a ground. Figure 4 shows a situation where an isolator is used as a floating output (the same mechanism can be present in a floating input configuration). In this instance, the chassis impedance, $Z_{CHASSIS}$, gives rise to an injected current during an ESD discharge. This current flows in the loop formed by L3, C2, L4, and C_{STRAY}. C_{STRAY} is the capacitance from the shield of an output cable to chassis ground. The larger the value of C_{STRAY}, the larger the injected current and the consequent internal noise voltage appearing across L4. If this voltage forces GND_2 beyond its absolute maximum rating, then latch-up could occur.

The following measures are recommended to avoid current injection difficulties:

- Minimize the chassis impedance to ground.
- Minimize C_{STRAY}, the cross-isolation barrier capacitance.
- If possible place a resistor, R_S, in series with V_{DD1} and V_{DD2} to limit latch-up trigger current. The recommended resistor value is 200 Ω.
- If it's not possible to place R_S as recommended, place a transient voltage suppressor (TVS) with an optional resistor, R_S, in series with the TVS and each V_{DD} pin. The recommended R_S value is between 50 Ω and 200 Ω. The TVS should trigger at the absolute maximum voltage rating of the product and limit the current into the power supply nodes, V_{DD1} and V_{DD2}. Do not use a series resistor on the V_{ISO} output pin for *iso*Power devices.
- Place a 50 Ω resistor between chassis ground and GND_1. This reduces $I_{INJECTED}$ and ultimately V_{NOISE}.
- Place a transient absorbing Zener diode from the connection to chassis ground. This clamps the noise voltage to within the Zener voltage.

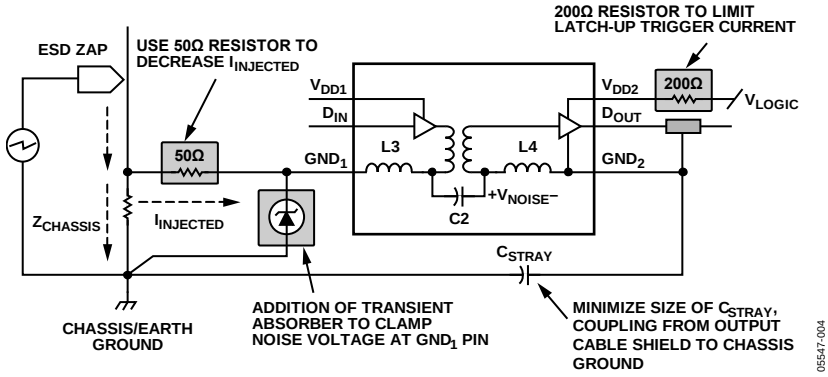

Figure 4. Injected ESD Current Mechanism and Recommended Solutions

INDUCTIVE COUPLING FROM ESD CURRENT

One consideration is the possibility of inductive coupling from the ESD current present in the printed wiring board or system chassis. Inductive pickup on *i*Coupler transformers from external magnetic fields is not a problem in the vast majority of applications; however, there have been rare instances in IEC 61000-4-2 ESD testing where this phenomenon has been noted. Solutions to this problem are straightforward.

Figure 5 and Figure 6 shows an ESD test setup and the paths of currents I_{ESD} and I_1 caused by an ESD strike. These currents can be very large, and induce large magnetic fields on the application printed wiring board and chassis. The placement and geometry of ground traces, ground circuit connections, board location, and orientation within the chassis are all critical in minimizing inductive pickup from the radiated magnetic fields.

Figure 5 shows a poor layout, which uses a thin ground trace near the device. It also shows a ground loop that allows some of I_{ESD} to flow through the board ground circuit as I_1. Close proximity and narrow trace widths increase the magnitude of the induced magnetic field. If strong enough, this can cause latch-up as previously discussed. Figure 6 shows an optimal design using a wide ground plane further away from the device and a single point ground which prevents I_{ESD} from flowing in the board ground circuit. When designing ground circuits, it is always helpful to think in terms of current paths.

When designing the chassis for the system, it is important to minimize impedance of the chassis ground connection. It is also helpful to mount printed circuit boards as far away from the edge of the chassis as possible, and to have the board oriented so that devices are parallel to any radiated magnetic fields as depicted in Figure 7.

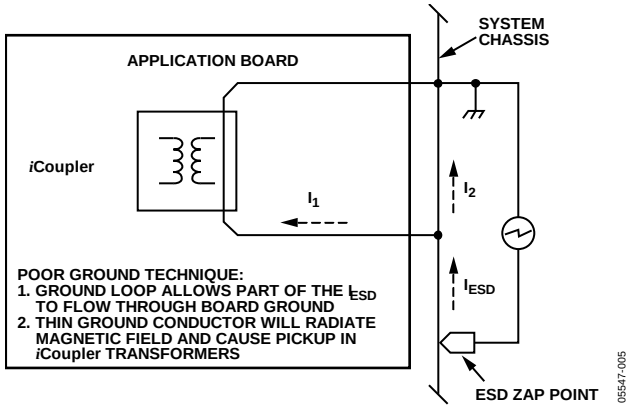

Figure 5. Poor Ground Layout Example of a Board Ground Circuit

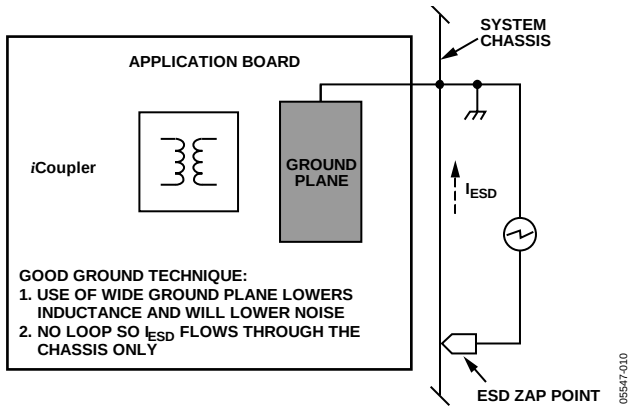

Figure 6. Good Ground Layout Example of a Board Ground Circuit

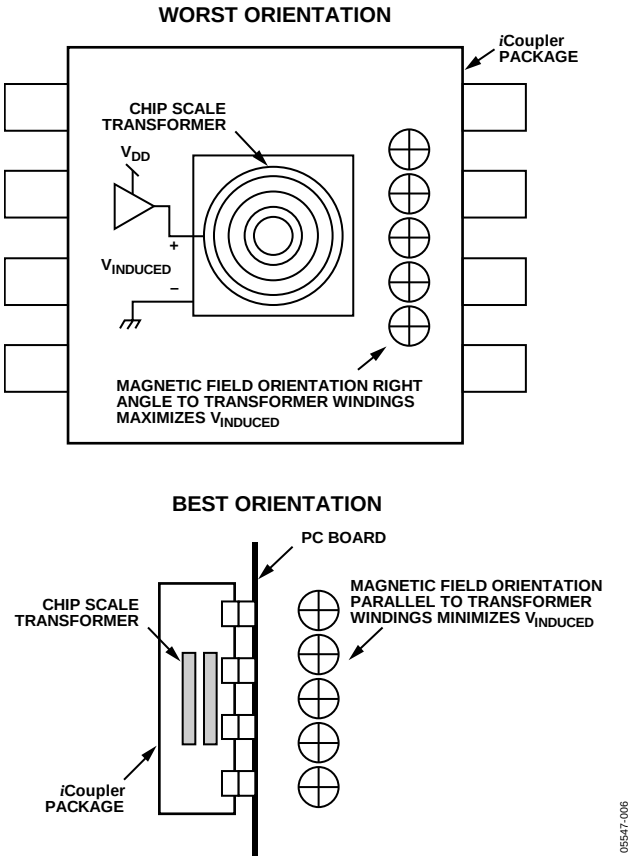

Figure 7. External Magnetic Field Interaction with i*Coupler Transformers*

If inductive coupling is a problem, recommended solutions include the following:

- Properly design the ground system to avoid ground loops.
- Use a ground plane instead of single narrow traces.
- Orient print wiring boards away from chassis boundaries.
- If possible, orient the device parallel to external magnetic fields as depicted in Figure 7.

IEC 61000-4-5 SURGE TESTING

Surge testing per IEC 61000-4-5 is another common system-level test in industrial and instrumentation applications. Figure 8 depicts an isolator in a surge test configuration showing associated bypass and stray capacitances. V_{TEST} is the surge test voltage appearing between earth ground and the board's local ground GND_1. This test typically has test voltages up to 4 kV. As shown in Figure 8, if excessive stray capacitance exists across the isolation barrier, the voltage at V_{DD1} can be driven above its absolute maximum rating and damage the device.

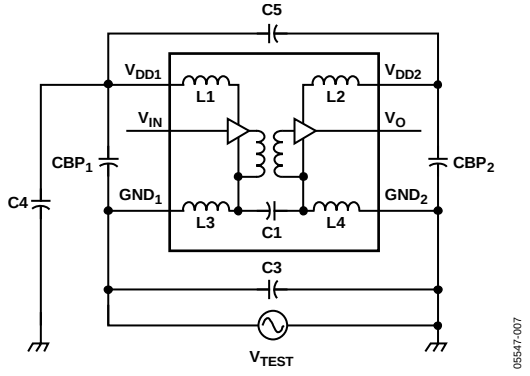

Figure 8. Isolator in IEC 61000-4-5 Surge Test Setup

Figure 9 shows the model reduced for easier analysis of circuit. The simplified schematic ignores negligible effects of lead inductances and lumps C_{STRAY} as a computed element (Equation 1).

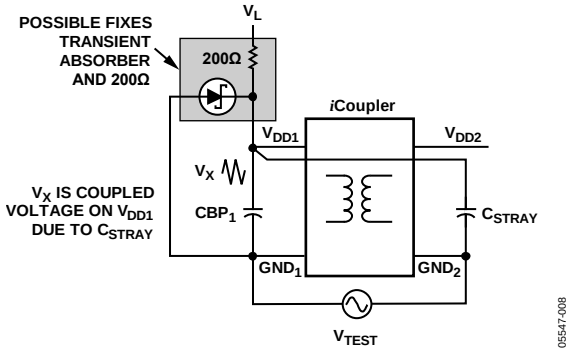

Figure 9. Simplified Equivalent Circuit of Figure 8

Using Figure 9, and ignoring inductances, C_{STRAY} is given as

$$C_{STRAY} = C4 + \frac{C_{BP2} \times C5}{C_{BP2} + C5} \quad (1)$$

The coupled voltage, V_X, is calculated using a simple capacitor divider

$$V_x = V_{TEST} \times \frac{C_{STRAY}}{C_{STRAY} + C_{BP1}} \quad (2)$$

Equation 2 shows that making C_{STRAY} small compared to C_{BP1} can minimize V_X. For example, with a test voltage of 4 kV and a bypass capacitance of 0.01 µF, even the moderate amount of 10 pF of stray capacitance would create a coupled V_{DD1} voltage of 4 V. When imposed on top of the normal supply voltage, this would induce latch-up. In such a situation, increase the bypass capacitance, C_{BP1}, to 0.1 µF to reduce the coupled voltage to 0.4 V—a much safer value. Do the following for best results:

- Minimize capacitances between digital isolator floating grounds and system grounds.
- Provide adequate bypassing with good quality ceramic bypass capacitors with values large enough to minimize the induced voltage at the supply pins.
- Ensure V_{DD1} and V_{DD2} are free from noise spikes.
- If possible add a 200 Ω resistor in series with V_{DD1} to limit parasitic SCR trigger current.
- Use a transient-absorbing Zener diode across V_{DD1}.

IEC 61000-4-4 FAST TRANSIENT AND BURST TESTING EXAMPLE

Fast transient and burst testing per IEC 61000-4-4 is another common system-level test that can cause problems if good design practice is not followed. This test couples high voltage fast edge signals onto system ac mains.

Figure 10 shows a simplified circuit diagram of a fast transient test setup. The main mechanism for problems here is interwinding capacitance of the system power supplies transformers. This stray capacitance can couple fast transient signals from the ac mains to the supply pins. If the voltage impressed on the supplies is high enough, then maximum rated supply voltages can be exceeded and latch-up is possible.

The best preventive measures in this example are:

- Use low interwinding capacitance supplies.
- Minimize supply noise by using adequate bypassing.
- Use Zener diode clamps across the supplies to clamp noise voltages.

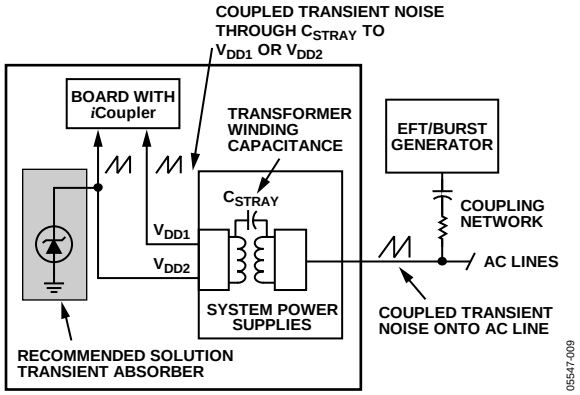

Figure 10. IEC 61000-4-4 Fast Transient/Burst Test Setup

ESD-HARDENED DIGITAL ISOLATORS

To better support the use of digital isolators in harsh applications, Analog Devices has introduced a line of ESD-hardened products. The ESD-hardened series takes advantage of improved circuit designs and layouts to increase robustness to ESD events. These products are pin- and specification-compatible with the standard isolator series counterparts. For many installed applications, the standard products perform well and meet robustness requirements. Therefore, both the standard isolators and the ESD-hardened series continue to be offered.

The part numbering for the ESD-hardened series is analogous to that of the standard product. Table 3 gives examples of the part numbering for the two product families.

Table 3. Part Numbering Examples for Various Standard and ESD-Hardened *i*Coupler Products

Standard Products	ESD-Hardened Products
ADuM1100	ADuM3100
ADuM1200	ADuM3200
ADuM1201	ADuM3201
ADuM1300	ADuM3300
ADuM1301	ADuM3301
ADuM1400	ADuM3400
ADuM1401	ADuM3401
ADuM1402	ADuM3402

INSIDE THE ESD-HARDENED SERIES

Several design enhancements are incorporated into the ESD-hardened series to create a more robust device. Specific improvements include:

- ESD protection cells added to all input/output interfaces.
- Key metal trace resistances reduced using wider geometry and paralleling of lines with vias.
- The SCR effect inherent in CMOS devices minimized by use of guarding and isolation techniques between PMOS and NMOS devices.
- Areas of high electric field concentration eliminated using 45° corners; on metal traces.
- Supply pin overvoltage prevented with larger ESD clamps between each supply pin and its respective ground.

CONCLUSION

By following the guidelines in this application note, designers can be assured of success in their application of digital isolators at the system level. Problems with system-level tests can be anticipated using the lumped-element circuit model presented. With this model and a good understanding of the various system tests, designers can avoid problems by employing the preventive techniques suggested in this application note. In situations where the recommendations cannot be implemented due to cost, system design, or other considerations, the ESD-hardened family provides an alternative method of avoiding ESD/latch-up problems.

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