ANALOG DEVICES

AN-209
APPLICATION NOTE

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8th Order Programmable Low Pass Analog Filter Using Dual 12-Bit DACs

by Bill Slattery

INTRODUCTION

This application note describes the design of a low pass analog filter whose cutoff frequency can be programmed from 100Hz to 50kHz. The filter is designed as a plug in expansion board for IBM PC AT/XT* or compatibles. A high order filter function is implemented, giving a very fast roll-off in the transition band. This design realizes an 8th order function with a roll-off equalling 48dB/octave. The note also discusses some of the tradeoffs and practical limitations which must be considered when designing a filter.

The design is based on a 2nd order universal active filter, as shown in Figure 1. The required performance is achieved by cascading four of these 2nd order stages.

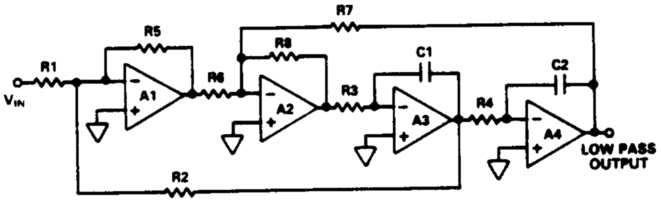

Figure 1. Universal Active Filter

The cutoff frequency of the filter is determined by R3, R4, C1 and C2. Digital control of the cutoff frequency is achieved by replacing resistors R3 and R4 in each stage by CMOS Multiplying Digital to Analog Converters (DACs). The DAC is in effect configured as a digitally programmable resistance.

To have accurate control of cutoff frequency, R3 and R4 within each stage must be closely matched. This is best achieved by replacing these two resistors with a monolithic dual 12-bit DAC. Analog Devices produces a range of suitable dual 12-bit DACs, the AD7537, AD7547 and AD7549. Since these have two DACs on one chip, DAC resistance matching will be in the order of 0.5%. Additionally, the use of 12-bit DACs ensures excellent resolution over the wide range of cutoff frequencies which can be programmed to the filter.

Applications for this filter include Industrial Process Control, Automatic Test Equipment (ATE), Sonar Signal Processing, Instrumentation, Audio Systems and Data Acquisition Systems. In Digital Signal Processing (DSP) applications, it can be used as the front end, low pass, anti-alias filter.

THE FILTER FUNCTION

A 2nd order low pass filter function is given by

$$\frac{V_{OUT}(s)}{V_{IN}(s)} = \frac{A_O \omega_O^2}{s^2 + \frac{\omega_O}{Q} s + \omega_O^2} \qquad (1)$$

where $s = j\omega$

ω_O = 3dB bandwidth (cutoff frequency)

Q = circuit Q factor

A_O = gain at $\omega = \omega_O$

The universal active filter shown in Figure 1 has a 2nd order low pass transfer function given by

$$\frac{V_{OUT}(s)}{V_{IN}(s)} = \frac{\frac{R5\,R8}{R1\,R6}\left(\frac{1}{C1\ R3}\right)^2}{s^2 + \frac{R5\,R8}{R2\,R6}\left(\frac{1}{C1\ R3}\right)s + \left(\frac{1}{C1\ R3}\right)^2} \qquad (2)$$

when $R3 = R4$

$R7 = R8$

and $C1 = C2$

By comparing coefficients between Equations (1) and (2) we see that

$$A_O = \frac{R5\,R8}{R1\,R6} \qquad (3)$$

$$Q = \frac{R2\,R6}{R5\,R8} \qquad (4)$$

$$\omega_O = \frac{1}{C1\,R3} \qquad (5)$$

hence $f_O = \frac{1}{2\pi C1\,R3}$ (filter cutoff frequency) (6)

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*IBM PC AT/XT is a trademark of International Business Machines Corp.

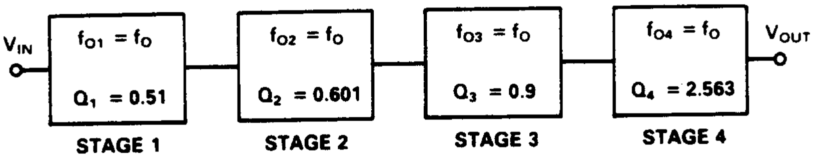


Figure 2. Block Diagram of 8th Order Butterworth Filter

8th Order Butterworth Filter Function

In realizing a particular 8th order filter function, each 2nd order stage is individually programmed to a specific cutoff frequency, f_O and Q. Values of f_O and Q for different filter types can be found using tables or software routines which are widely available (References 1 and 2).

The design discussed in this application note implements a unity gain, Butterworth filter function. The cutoff frequency which must be programmed to each stage is the same as the overall filter cutoff frequency f_O. The Qs of each stage, however are not the same. Figure 2 shows the required values of f_O and Q for each stage.

Since the gain of each stage is unity ($A_O = 1$), Equations (3) and (4) can now be solved using the values of Q given in Figure 2, to yield the required resistor values. Table I lists the required resistor values of each stage.

	Stage 1	Stage 2	Stage 3	Stage 4
R1	39k	150k	120k	12k
R2	20k	82k	82k	33k
5	12k	82k	82k	3.9k
6	10k	1.8k	2.7k	10k
R7	33k	3k	3k	33k
R8	33k	3k	3k	33k

1% tolerance resistors should be used.

Table I. Resistor Values for Each Stage of This 8th Order Butterworth Filter

DIGITAL CONTROL OF CUTOFF FREQUENCY

The cutoff frequency of the filter is determined by C1, C2, R3 and R4. However, since C1 = C2 and R3 = R4, the cutoff frequency f_O can be expressed in the form shown in Equation (6).

Digital control over cutoff frequency is achieved by replacing R3 and R4 with one of the following configurations:

1. The AD7537 DAC.
2. The AD7537 DAC in series with a padding resistance R_{PAD}.

The principal difference between the AD7537, AD7547 nd AD7549 is in their loading structure. The AD7537 is nosen for this design, see Figure 3. Its 2 byte (8 + 4) loading structure makes it ideal to use with a microprocessor based system which has an 8-bit data bus. The IBM PC AT/XT or compatible is just such a system.

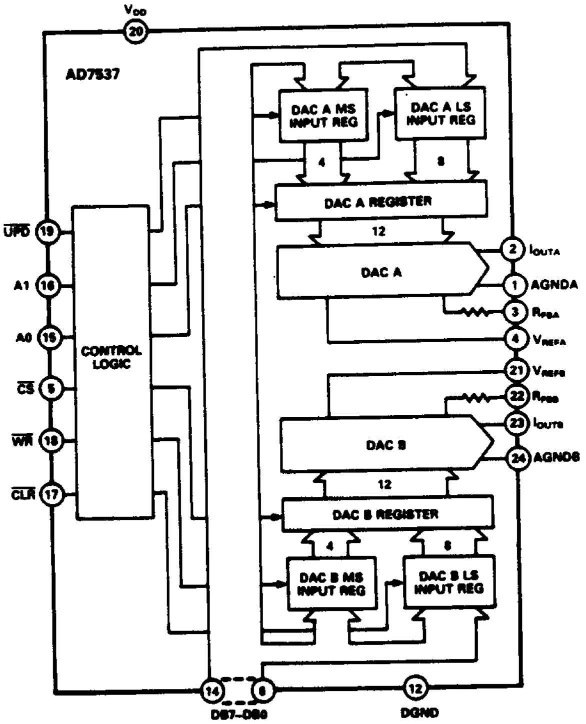


Figure 3. Functional Block Diagram of AD7537

The AD7537 is a dual 12-bit current output DAC which comes in a space saving 24-pin 0.3" wide package. The AD712 op amp is chosen for this design. It is a high performance, low-cost dual op amp. Its large Gain Bandwidth Product ensures excellent performance of the filter for cutoff frequencies up to and beyond 50kHz. (For more detailed information on the AD7537 and AD712 consult the relevant data sheets.)

Design (1)

Figure 4 shows how R3 and R4 are replaced by the AD7537 dual DAC. The AD7537 is now in effect a pair of programmable resistors.

The equivalent resistance of a DAC in this configuration is given by

$$R_{EQ} = \frac{R_{DAC}}{D} \tag{7}$$

where R_{DAC} is the DAC ladder resistance

and D is the digital fraction programmed to the DAC. D is given by

$$D = \frac{N}{2^n} \tag{8}$$

where n = resolution of DAC in bits
(in this case n = 12)
N = DAC digital code (decimal 1 to 4095)

Since R3 is now replaced by R_{EQ} we can write

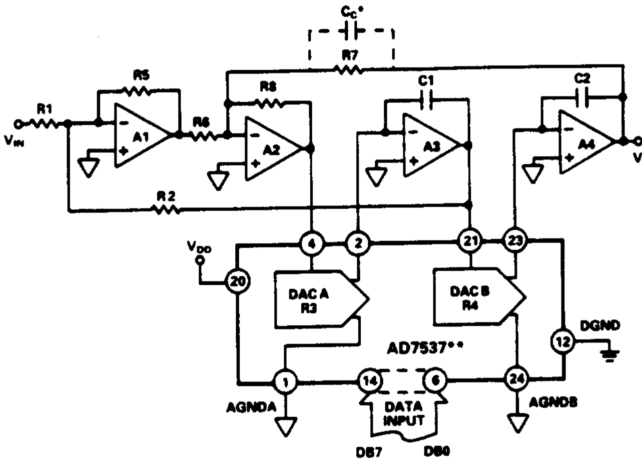
$$f_O = \frac{1}{2\pi C1\, R_{EQ}} \qquad (9)$$

Choosing $C1 = 220pF$ and $R_{DAC} = 14k$

and solving between Equations (7), (8) and (9), the cutoff frequency can be written as a function of the decimal code N.

$$f_O = (0.01262 \cdot N)\ kHz \qquad (10)$$

In practice the cutoff frequency can now be programmed between 100Hz and 50kHz with a resolution of 13Hz.



*See "GAIN BANDWIDTH PRODUCT SECTION".
**ADDITIONAL CIRCUITRY OMITTED FOR CLARITY.

Figure 4. Single Stage of Programmable Filter Using an AD7537

For a known DAC ladder resistance, a stage can be accurately programmed to a specific cutoff frequency. The two frequency controlling resistors are effectively matched to within 0.5%, since both are in one monolithic package. However, to achieve an overall accurate filter cutoff frequency, the DACs in each of the four stages must have similar DAC ladder resistances. DAC ladder resistance can vary between 9k and 20k with a typical value of 14k, for different AD7537s.

Design (2)

One solution that can be adopted to avoid using specially selected AD7537s is to use a padding resistance R_{PAD} in series with the DAC ladder resistance as shown in Figure 5. A large value of R_{PAD}, 100k, is used. This has the effect of desensitizing the variations in DAC ladder resistance. This means that the specified variation in DAC ladder resistance now has an insignificant effect on the overall filter performance.

The equivalent resistance of a DAC in this configuration is given by

$$R_{EQ} = \frac{R_{DAC} + R_{PAD}}{D} \qquad (11)$$

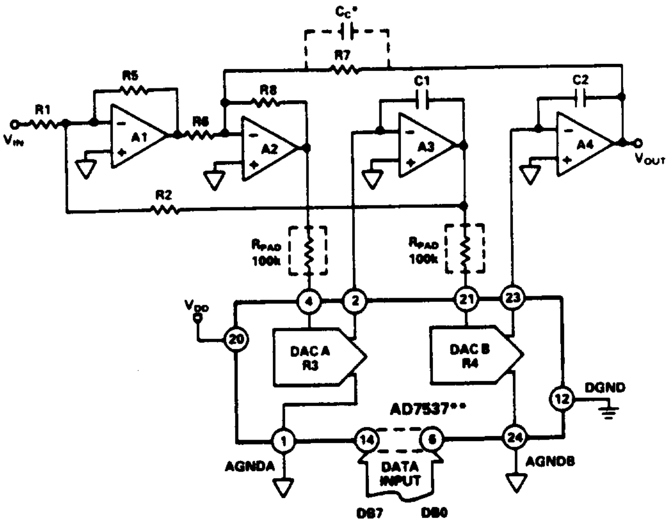
Choosing $C1 = 22pF$, $R_{PAD} = 100k$ and $R_{DAC} = 14k$

and solving between Equations (8), (9) and (11), the cutoff frequency can be written as a function of the decimal code N.

$$f_O = (0.01549 \cdot N)\ kHz \qquad (12)$$

The cutoff frequency can now be programmed between 100Hz and 50kHz with a resolution of 16Hz.

It should be noted that since we are using DACs whose ladder resistance can vary between 9k and 20k, the above expression for f_O will be accurate to within ±4.5%. If the padding resistance R_{PAD} was not used, f_O could vary by up to ±30% of the programmed value. Design 1 does not have this problem since DACs whose ladder resistance is known to be 14k are used. Cost and accuracy tradeoffs must be considered when choosing either of the two design options.



*See "GAIN BANDWIDTH PRODUCT SECTION".
**ADDITIONAL CIRCUITRY OMITTED FOR CLARITY.

Figure 5. Single Stage of Programmable Filter Using an AD7537 and Series Resistances R_{PAD}

GAIN BANDWIDTH PRODUCT

A compensation capacitor C_C must be used on the 4th Stage of the filter. This is required to reduce effects caused by Gain Bandwidth Product limitations. The value of capacitance depends on the type of function implemented and the design option choosen.

For this 8th Order Butterworth Filter, the value of the capacitor can vary between 15pF and 47pF

Design (1) – Use 15pF

Design (2) – Use 47pF.

DIGITAL INTERFACE

The filter circuit can be built on a standard IBM prototype card and plugged directly into the expansion slot on the main board of an IBM PC AT/XT or compatible. The prototype board basically consists of buffers and some circuitry which generates an enable line $\overline{EN}$. Figure 7 shows the interface layout used. Each AD7537 is addressed ($\overline{CS}$) using a 74LS138 (3 to 8 line decoder). Address lines A3 to A5 as well as the $\overline{EN}$ and $\overline{IOW}$ lines are used to decode each address. The valid addresses which can be used are HEX300 to HEX31F.

Since the AD7537 is a dual 12-bit DAC, data is loaded to each DAC with a 2-byte (8+4) loading instruction. Address lines A0 to A1 select DAC A and DAC B, see Figure 3, as well as selecting the low and high bytes of data. The address decoder also generates the $\overline{UPD}$ line which is used to update the data in all the DACs.

An IBM Basic program for this Butterworth filter is given in Table A1, Appendix 1. The program is run by inputting the required cutoff frequency in kHz as well as the values of R_{DAC}, R_{PAD}, and C1. The program calculates and outputs the relevant digital code to each of the DACs. Figure 6 gives a flow diagram representation of the program used.

PERFORMANCE

Plots of amplitude and phase response as well as a plot of the noise spectrum for the 8th Order Butterworth Filter are given in Appendix 2.

Figure A1 shows the amplitude response of the filter using Design 1. Plots for four different cutoff frequencies are given in this figure. The programmed cutoff frequency is found to be within 3% of the actual cutoff frequency achieved, for each of the four cases. Passband ripple is in the order of 0.2dB. Stop-band rejection is greater than 100dB, except for frequency components between 2kHz and 4kHz, and at 41kHz and 1MHz, where rejection is in the order of 90dB. The reduction in attenuation at lower frequencies is mainly due to the increased value of DAC equivalent resistance R_{EQ}. As the value of resistance increases, so too does the level of noise increase. In practice, frequencies below 500Hz should not be programmed to the filter with the component values used in this design option. Cutoff frequencies of less than 500Hz can however be achieved if larger values of capacitance C1 are used. This effectively reduces the range of selectable cutoff frequencies but allows lower cutoff frequencies with a reduced noise floor to be programmed to the filter. At high frequencies, greater than 10MHz, it is found that there is less attenuation; attenuation reduces below 90dB. This is due both to gain bandwidth limitations of the op amp and feedthrough across the system.

Figure A2 shows the amplitude response for various cutoff frequencies, using Design 2. Again we can see that the pass band ripple is less then 0.2dB. The accuracy of the cutoff frequency however will vary by about 4.5% from the programmed cutoff frequency. Also, it should be noted that in using Design 2 stopband rejection will be reduced to about 70dB. This is due to increased noise caused by the large value of padding resistance R_{PAD}. This can be reduced somewhat by using low noise resistors.

Figure A3 is a plot of the noise spectrum at the output of the filter, using Design 1. The cutoff frequency is programmed at 50kHz, and the input is grounded. The largest noise component in our system occurs at about 41kHz and has an amplitude of −54.8dBm* (0.4mV). Since the filter is present in a noisy environment, i.e., the board of an IBM PC AT/XT or compatible, it is not surprising that there should be noise present in the system. In practice, there is a minimum input signal level that can be applied to the filter to achieve a specific Signal-to-Noise Ratio (SNR) in the filter's pass band. In this design, using the noise component at 41kHz, an SNR greater than 90dB can be achieved by applying input signal levels of greater than 1.3V rms.

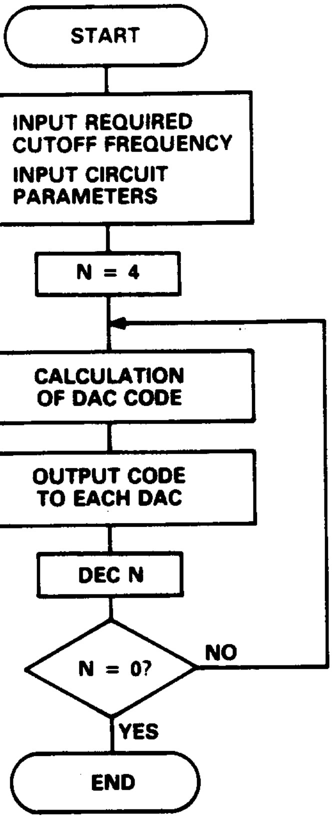


Figure 6. Flow Diagram Representation of Control Algorithm

Figure A4 is a plot of the filter's phase response. The phase response of the system determines the Group Delay of the filter.

$$\text{Group Delay} = \frac{1}{2\pi}\frac{d\phi}{df}$$

Thus a linear phase response implies a constant group delay. The phase response plot shown exhibits some slight nonlinearity. This is as expected for a Butterworth filter function. If phase response is an important design consideration, a different filter function should be considered, eg., Bessel. (References 1 and 2.)

PERFORMANCE EXTENSION

1. The frequency range of this filter can be extended to 100kHz, using Design 1, by simply replacing the 220pF capacitors in each stage by 110pF capacitors. Stopband attenuation of 85dB and passband ripple of less than 0.2dB is achieved over the full range.
2. A Chebychev response can be achieved by using different values of R1 and R2 in each stage. R1 and R2 can be evaluated by solving Equations (3) and (4) for the values of Q given in Figure 8. Figure 8 gives the cutoff frequency f_O and Q for each stage of a 0.2dB ripple 8th Order Chebychev Filter. It should be noted that for a Chebychev filter the cutoff frequency of each stage is

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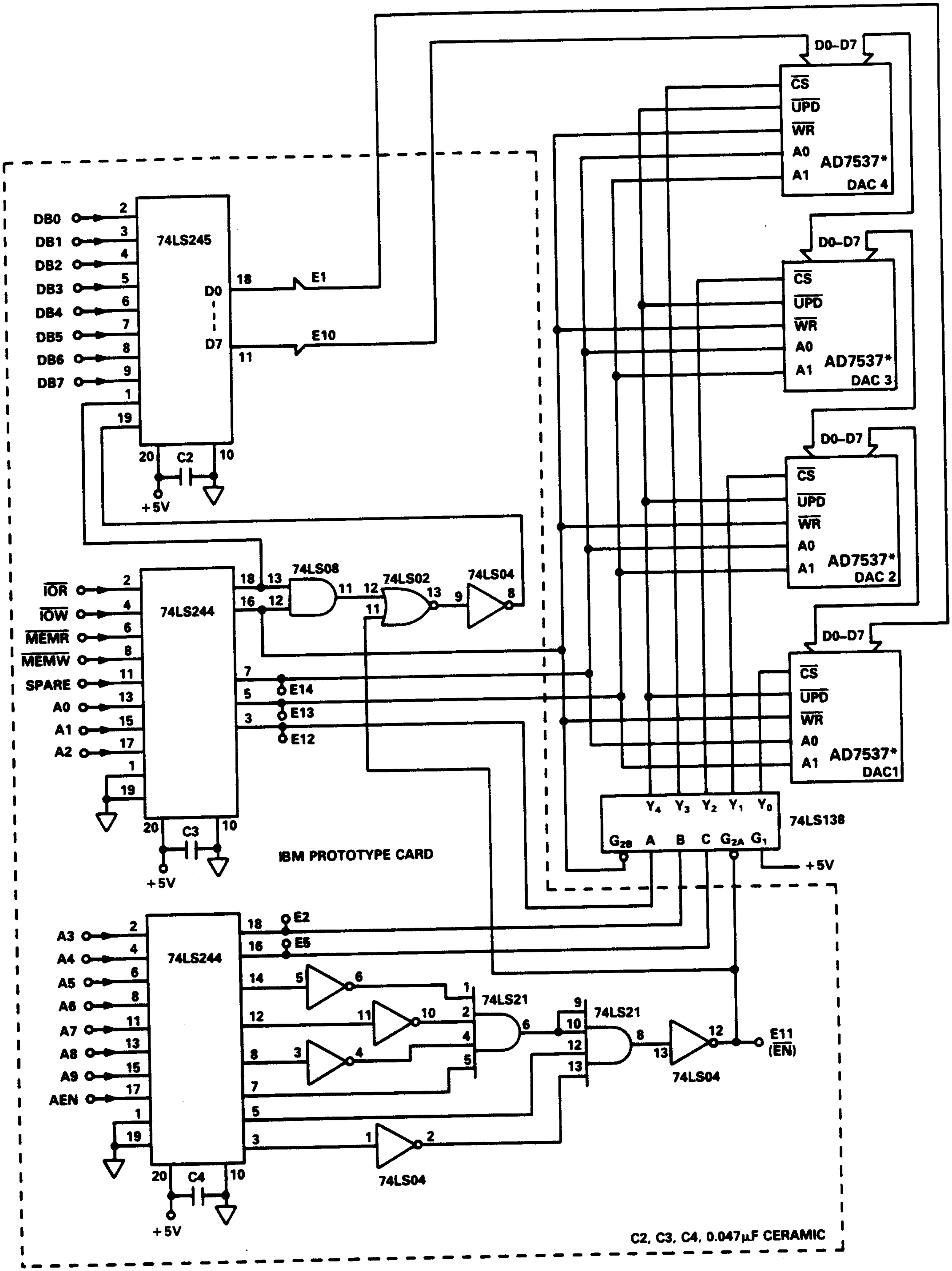
*Measured with respect to 50Ω.



*ADDITIONAL CIRCUITRY OMMITED FOR CLARITY.

Figure 7. IBM PC AT/XT Digital Interface

not the same as the overall filter cutoff frequency, as was the case with the Butterworth filter. The remainder of the design proceedure is the same as that outlined for the Butterworth filter. An IBM Basic program for this Chebychev filter is given in Table A2, Appendix 1. This program tunes each individual stage to its particular cutoff frequency so that a specified overall filter cutoff frequency is achieved.

3. Programmability over filter type (i.e., Butterworth, Chebychev, Bessel, etc.) as well as cutoff frequency can be achieved by replacing R1 and R2 of each stage by an AD7537. This gives us total software control over all the filter parameters.

CONCLUSION

Filtering in the analog domain has many inherent advantages over filtering in the increasingly popular digital domain. Analog filtering is a continuous time process whereas digital filtering is a sampled data process. Digital filters require extensive software routines to implement such algorithms as FIR and IIR filters. The analog filter utilizes digital processing power to control the filter while giving analog performance.

This application note deals with the IBM PC AT/XT or compatible as the digital controller for the analog filter. The filter could equally be controlled using any other microprocessor. Suggested microprocessor interfaces are given in the AD7537, AD7547 and AD7549 data sheets.

ACKNOWLEDGEMENTS

To Mike Curtin for suggesting the original design idea. To Sean Morley for his help in building and testing the circuit.

REFERENCES

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2. M.E. Van Valkenburg, "Analog Filter Design." Holt-Saunders Publication Number: ISBN 4-8338-0091-3.
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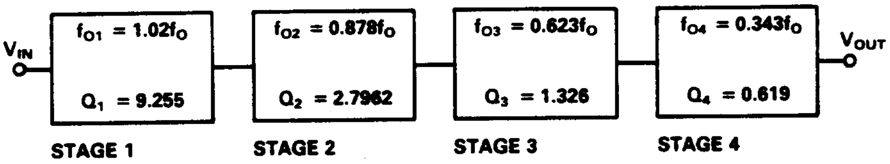

Figure 8. Block Diagram of 8th Order Chebychev Filter

APPENDIX 1

```
10  CLS
20  PRINT “8th-Order Low-Pass Butterworth Filter”
30  PRINT
40  INPUT “F0 (kHz) (500Hz . . . . 48kHz)                  = ” ;FO
50  F0 = F0*1000
60  PRINT
70  INPUT “RDAC(Kohms) (14K TYPICALLY)                     = ” ;RDAC
80  RDAC = RDAC*1000
90  PRINT
100 INPUT “RPAD(Kohms) (0 FOR DES.1, 100K FOR DES.2)       = ” ;RPAD
110 RPAD = RPAD*1000
120 PRINT
130 INPUT “C(pFarads) (220pF FOR DES.1, 22pF FOR DES.2)    = ” ;C
140 C = C*1E-12
150 REQ = 1/2/22*7/FO/C
160 N = 4096*(RPAD + RDAC)/REQ
170 PRINT                                                  = ” ;HEX$(N);“H”
180 PRINT “CODE
190 N = INT (N)
200 N1 = INT(N/256)'   MSB
210 N2 = N-N1*256 '   LSB
220 ADDR = &H300
230 FOR C = 0 TO 3
240 OUT ADDR,N2
250 OUT ADDR + 1,N1
260 OUT ADDR + 2,N2
270 OUT ADDR + 3,N1
280 ADDR = ADDR + 4
290 NEXT C
300 OUT &H310,0 'UPDATE DACS
310 END
```

Table A1. IBM Basic Program for 8th Order Butterworth Filter

```
10  CLS
20  PRINT “8th-Order Low-Pass Chebychev Filter”
30  PRINT
40  INPUT “F0 (KHz)                                        = ” ;FO
50  F0 = F0*1000
60  PRINT
70  INPUT “RDAC (Kohms)  (14K TYPICALLY)                   = ” ;RDAC
80  RDAC = RDAC*1000
90  PRINT
100 INPUT “RPAD(Kohms)  (0 FOR DESIGN 1)                   = ” ;RPAD
110 RPAD = RPAD*1000
120 PRINT
130 INPUT “C(pFarads)  (220pF FOR DES. 1)                  = ” ;C
140 C = C*1E-12
150 FOR I = 0 TO 3
160 READ X
170 FC = X*FO
180 REQ = 1/2/22*7/FC/C
190 N = 4096*(RPAD + RDAC)/REQ
200 PRINT
210 PRINT “CODE” ;I;”                                      = ”;HEX$(N);“H”
220 N = INT(N)
230 N1 = INT(N/256) '   MSB
240 N2 = N-N1*256 '   LSB
250 ADDR = &H300
260 ADDR = ADDR + I*4
270 OUT ADDR,N2
280 OUT ADDR + 1,N1
290 OUT ADDR + 2,N2
300 OUT ADDR + 3,N1
310 NEXT I
320 OUT &H310,0'UPDATE DACS
330 END
340 DATA 1.02,.878,.623,.343
```

Table A2. IBM Basic Program for 8th Order Chebychev Filter

APPENDIX 2

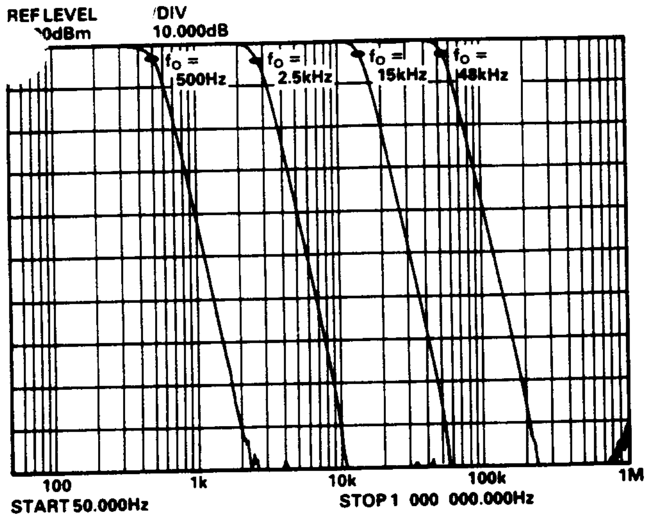

Figure A1. Amplitude Response of Butterworth Filter for Various Cutoff Frequencies Using Design 1

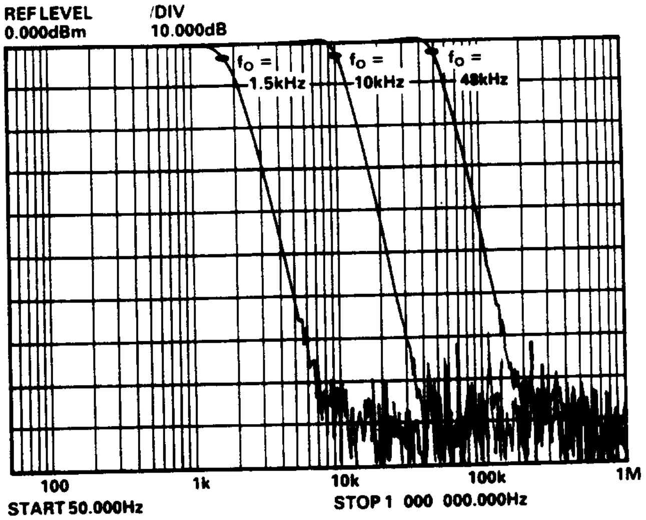

Figure A2. Amplitude Response of Butterworth Filter for Various Cutoff Frequencies Using Design 2

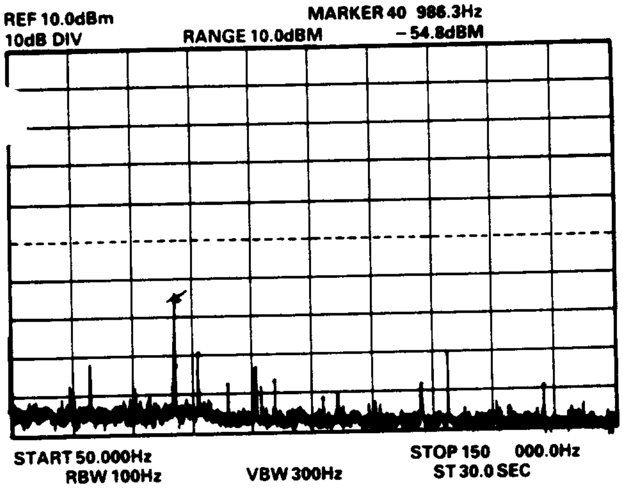

Figure A3. Noise Spectrum of Filter

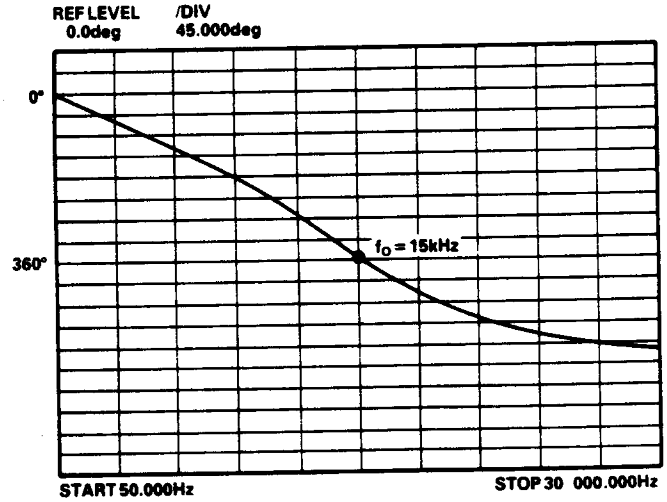

Figure A4. Typical Phase Response of Butterworth Filter