ANALOG DEVICES

AN-310
APPLICATION NOTE

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Single Supply 12-Bit DAC Circuits Using the AD7568

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This application note suggests a number of different circuit configurations in which a CMOS D/A converter can be used to generate a variety of popular output voltage ranges. All of the circuits work off of positive supplies only and feature the AD7568, an octal 12-bit current-out CMOS DAC. Figures 1–4 show the DACs being operated in their current-steering mode, while Figures 5–7 show operation in the voltage-switching mode. A previous application note, AN-225, covered the issues involved in using current-out DACs in the voltage-switching mode, and the reader is referred to this for additional information.

In the output voltage expressions for Figures 1 to 7, the term D represents the fractional equivalent of the DAC digital input code in decimal, N. For a 12-bit DAC, D = N/4095 and can vary from 0 to 4095/4096, i.e., D can almost, but never quite, equal unity. However, in order to allow easy comparisons between the different circuits, D is assumed to range from 0 to 1. It should be remembered that the output voltage expressions evaluated with D = 1 are in fact 1 LSB higher than is theoretically possible.

Although the AD7568 is a +5 V only device and is specified in the normal current-steering mode with the I_{OUT1} and I_{OUT2} outputs at 0 V, the DACs still work well with their current outputs biased above 0 V. For instance with I_{OUT1} and I_{OUT2} raised above ground by up to 1.23 V, a typical bandgap value, the DACs remain monotonic to 12 bits.

In the voltage switching mode configuration I_{OUT1} can be raised above I_{OUT2} by up to 1.23 V and 12-bit DAC monotonicity is still assured. This performance is maintained even if the I_{OUT2} output is itself at 1.23 V above ground.

Appendix 1 shows some typical linearity performance curves for the AD7568 under various biasing conditions.

Current-Steering Mode

Figure 1 shows the simplest circuit in this mode. The DAC reference input, V_{REF}, is shown tied to 0 V, but it can be biased to any positive voltage up to twice the value of V1 to change the full scale output voltage.

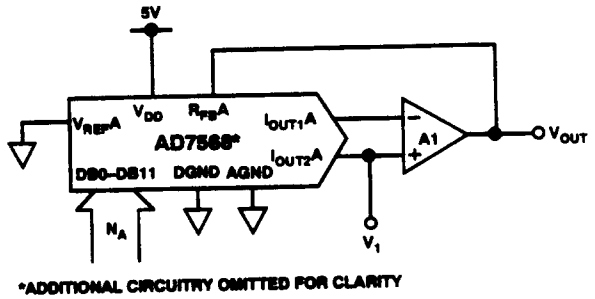

Figure 1. Simple Current Steering Mode Circuit

For the circuit of Figure 1, the output voltage is given by:

$$V_{OUT} = V_1 (1 + D)$$

For example, if V_1 = 1.23 V, the output voltage goes from 1.23 V at D = 0 to 2.46 V at D = 1. This circuit is very limited in its output voltage range, and consequently gain is generally added around the op amp to extend the performance. A circuit to multiply the output voltage range by some gain factor is shown in Figure 2.

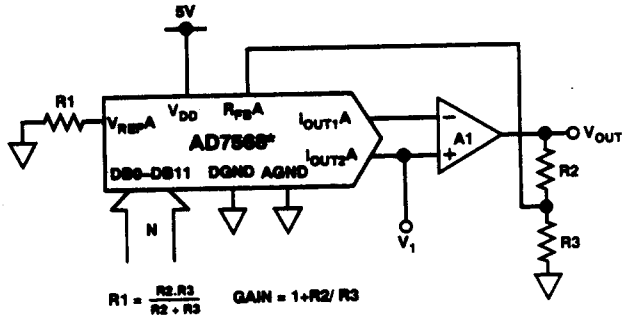

Figure 2. Adding Gain to Circuit of Figure 1

Using three external resistors is the recommended way (Reference 1) of adding gain to the standard configuration without requiring a large gain adjustment range or compromising the circuit's temperature coefficient. The resistors R1, R2 and R3 should all have similar temperature coefficients, but they need not match the temperature coefficient of the DAC.

For the circuit of Figure 2, the output voltage is given by:

$$V_{OUT} = V_1(1 + D)(1 + R2/R3)$$

Similar to the circuit of Figure 1, the interesting feature f this circuit is its voltage doubling nature regardless of the gain factor—the all 1s code output voltage is double the all 0s code output voltage. For instance, with V_1 = 1.23 V and R2 = R3 (Gain Factor = 2), the output voltage varies from 2.46 V at D = 0 to 4.92 V at D = 1.

However simple voltage doubling may not be to everyone's requirement. If R3 in Figure 2 is returned to V_1 instead of 0 V, then the all 0s code output voltage avoids being multiplied by the added gain factor and is simply V_1. Figure 3 shows this configuration.

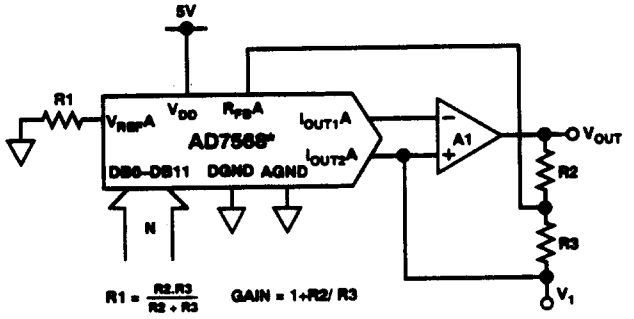

Figure 3. Avoiding Gain Factor Multiplication of All 0s Code Output Voltage

For the circuit of Figure 3, the output voltage is given by:

$$V_{OUT} = V_1 + V_1 \cdot D(1 + R2/R3)$$

In this instance, with V_1 = 1.23 V and R2 = 2R3 (Gain Factor = 3), the output voltage range is from 1.23 V at the all 0s code to 4.92 V at the all 1s code.

The facility to apply a second voltage to the V_{REF} input of the DAC allows the output voltage range to be closely tailored to requirements. As an example, Figure 4 generates an output voltage of 2.5 V to 7.5 V, i.e., 5 V ± 2.5 V.

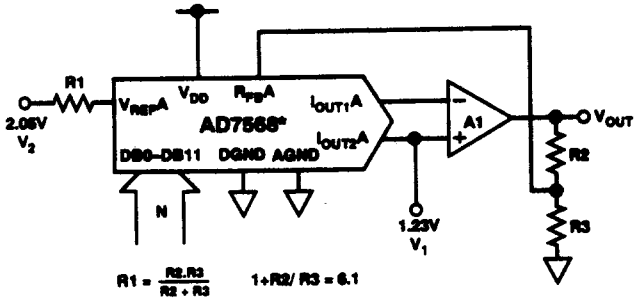

Figure 4. Circuit to Generate 5 V ± 2.5 V Output

For the circuit of Figure 4, the output voltage is given by:

$$V_{OUT} = V_1(1 + R2/R3) + (V_1 - V_2)D(1 + R2/R3)$$

The gain factor is chosen to produce the high-side 7.5 V output with V_1 again equal to 1.23 V. This value is then used in the above expression to solve for V_2 when the output voltage is at its low-side value of 2.5 V. A feature of this particular circuit is that V_2 is greater than V_1, and hence the output voltage vs. code transfer function is inverted, i.e., all 0s code produces 7.5 V output; all 1s code produces 2.5 V output.

Voltage-Switching Mode Circuits

Figure 5 is discussed in the previously mentioned AN-225 but is reproduced here to show the suitability of the AD7568 in voltage-switching mode applications for 5 V-only systems.

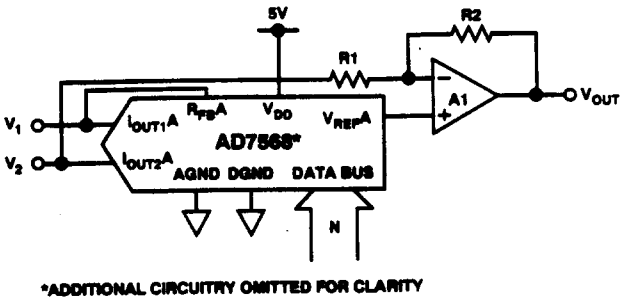

Figure 5. Voltage-Switching Mode Operation

For the circuit of Figure 5, the output voltage is given by:

$$V_{OUT} = V_2 + (V_1 - V_2)(1 + R2/R1)D$$

If R1 = R2 and the voltage sources are two bandgaps where the V_1 bandgap is with respect to V_2, i.e., V_1 is 2.46 V above ground, the output voltage over the code range is as follows:

When D = 0,

$$V_{OUT} = 1.23\ V$$

When D = 1/2,

$$V_{OUT} = 2.46\ V$$

When D = 1,

$$V_{OUT} = 3.69\ V$$

The output voltage is of the form 2.46 V ± 1.23 V. In this circuit the output voltage swings 1.23 V up and down around an effective bias point of 2.46 V. This type of output is commonly termed a V_{BIAS}/V_{SWING} output and is very popular in the hard disk and optical disk drive industry. Using bandgaps for V_1 and V_2, the minimum output voltage of Figure 5 is 1.23 V. If it is important to have 0 V as the minimum output voltage, this can be easily achieved by returning R1 in Figure 5 not to $I_{OUT2}A$, but to $I_{OUT1}A$. In addition R1 must be made equal to R2. The output voltage expression for this configuration is:

$$V_{OUT} = V_2 + (V_1 - V_2)(2D - 1)$$

This is of the form 1.23 V ± 1.23 V, i.e., now when D = 1/2, V_{OUT} = 1.23 V and not 2.46 V.

Figure 5 can also be rearranged to generate a V_{BIAS} level higher than either 1.23 V or 2.46 V by tying the DAC feedback resistor to $V_{REF}A$ instead of $I_{OUT1}A$. The output voltage expression under these conditions is given by;

$$V_{OUT} = V_2 + (1/2)(V_1 - V_2)(1 + R2/R1)(1 + D)$$

If R2 = 3R1, the above expression simplifies to;

$$V_{OUT} = 1.23\ V + 2.46(1 + D)$$

This is of the form 4.92 V ± 1.23 V.

This highlights the fact that although the DAC itself is limited to a 5 V power supply, it can control output voltages higher than this.

Programmable V_{BIAS} Level

Some applications require a variable V_{BIAS} level and a constant V_{SWING} level. For the circuit of Figure 6 the output voltage is given by;

$$V_{OUT} = V_2 (1 + D_B)(1 + R2/R1) - V_1(2D_A - 1)(R2/R1)$$

With R1 = R2 the output voltage simplifies to:

$$V_{OUT} = 2V_2 (1 + D_B) - V_1(2D_A - 1)$$

where D_A and D_B are fractional representations of the digital codes to DACs A and B respectively. When $V_1 = V_2 = 1.23$ V, the output voltage swings 1.23 V (determined by D_A) around a bias level which is programmable (via D_B) from 2.46 V to 4.92 V. Note that there is a code inversion effect in this circuit also. For a given V_{BIAS} level the output voltage is at its minimum with all 1s in DAC A and vice versa.

Using bandgaps for V_1 and V_2, the minimum output voltage of Figure 6 is 1.23 V. If 0 V is the minimum output voltage required, this can be easily achieved by tying the DAC B feedback resistor, $R_{FB}B$, to $V_{REF}B$. This has the effect of halving the voltage at the noninverting input of A2. The output voltage now swings ±1.23 V (determined by D_A) around a bias level which is programmable (via D_B) from 1.23 V to 2.46 V.

Also note in Figure 6 that if DAC B is removed and V_2 is applied directly to the noninverting input of A2, the output voltage will be of the form 2.46 V ± 1.23 V. In comparison with Figure 5 which has a similar output voltage signal this configuration requires one more op amp and two matched resistors but only one bandgap reference ($V_1 = V_2$).

Programmable Full-Scale Level

Another common requirement is for a circuit which can have programmable full-scale V_{SWING} levels while retaining the same V_{BIAS} value. Such a circuit is shown in Figure 7.

With R1 = R2 the output voltage for Figure 7 is given by:

$$V_{OUT} = V_2 + D_A (V_1 - V_2) (2D_B - 1)$$

When $V_1 = V_2 = 1.23$ V and the V_1 bandgap is with respect to V_2, i.e., V_1 is 2.46 V above ground, the output voltage swings ±1.23 V maximum around a bias level of 1.23 V. The full-scale V_{SWING} voltage is set by D_A to be between 1.23 V and 0 V theoretically.

REFERENCES

1. Brokaw P., "Input Resistor Stabilizes MDACs Gain," *EDN*, January 7, 1981, pp. 210–211.

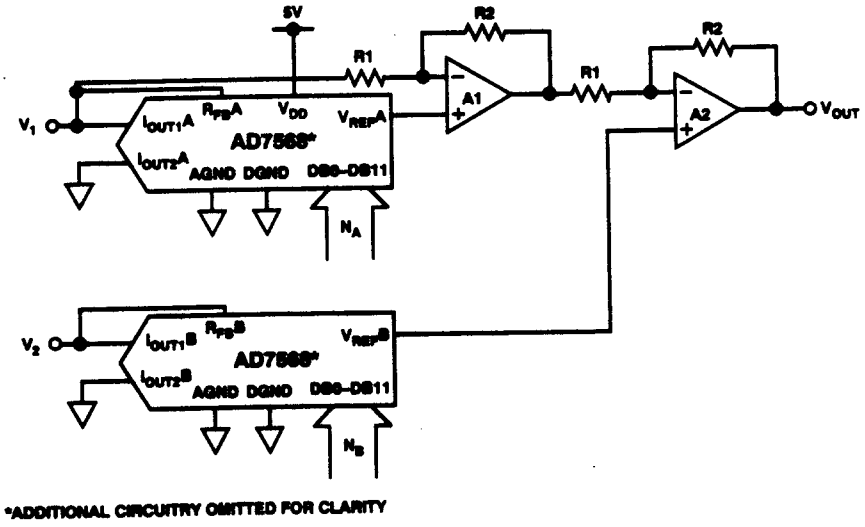

Figure 6. Programmable V_{BIAS} Level

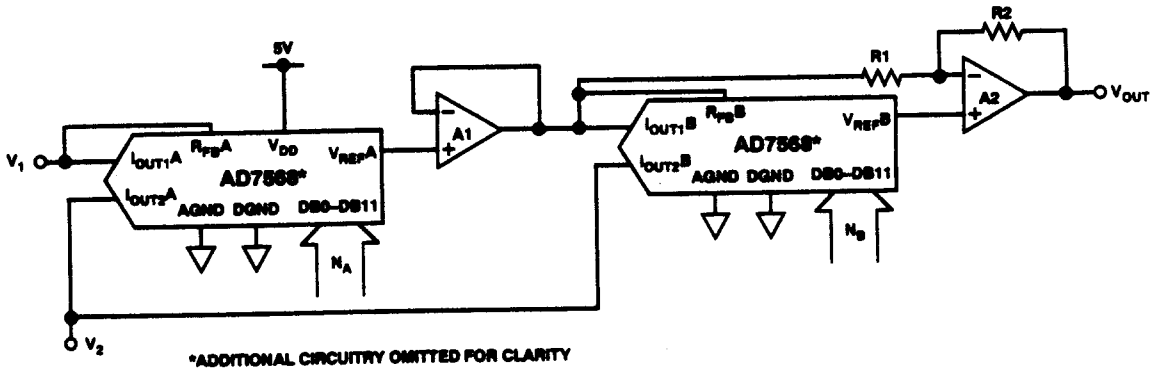

Figure 7. Programmable Full-Scale V_{SWING} Level

Appendix 1

Figures A1–A6 show typical linearity plots of the AD7568 tested in both the Figure 1 and Figure 5 configurations of this application note. The plots of Figures A1–A2 were generated using the Figure 1 circuit and use the same DAC channel within the AD7568 to show temperature effects on the linearity performance. The plots of Figures A3–A4 were generated using the Figure 5 circuit and again the same DAC channel within the AD7568 is used to show temperature effects on the linearity performance. Similarly for Figures A5–A6, the same channel is recorded. For every plot the DAC V_{DD} is +4.75 V and 1 LSB = 300 microvolts. The worst case conditions, in linearity terms, occur at low power supplies and high temperatures.

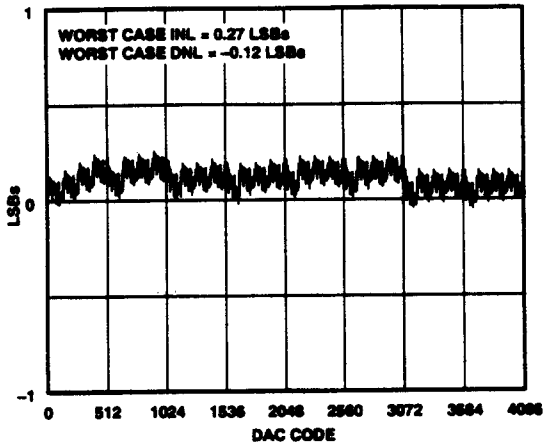

Figure A1. Current-Steering Mode Linearity with V_1 = 1.23 V and T_A = +25°C

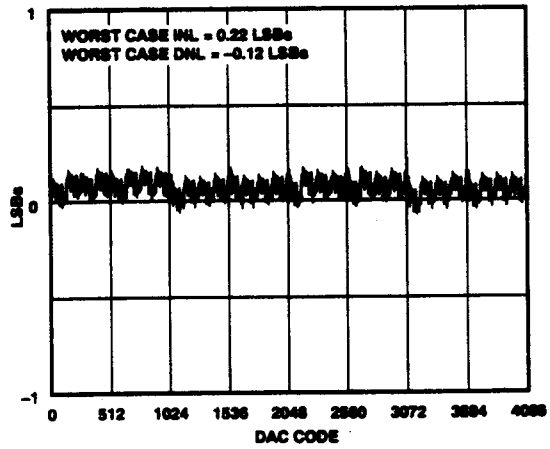

Figure A2. Current-Steering Mode Linearity with V_1 = 1.23 V and T_A = +85°C

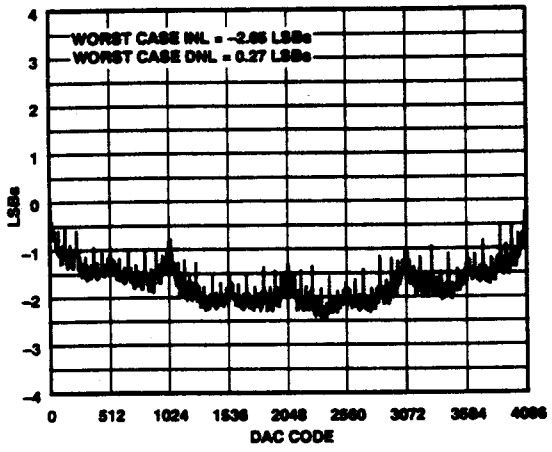

Figure A3. Voltage-Switching Mode Linearity with V_1 = 1.23 V, V_2 = 0 V and T_A = +25°C

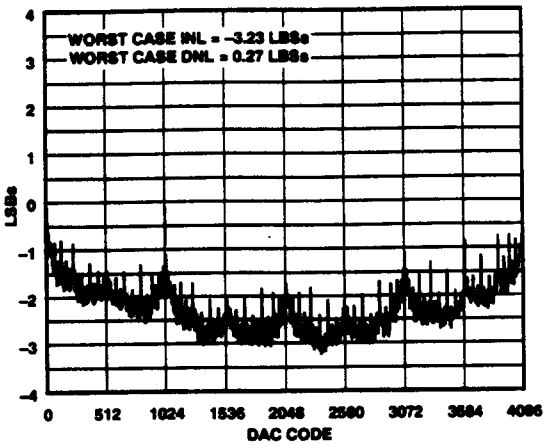

Figure A4. Voltage-Switching Mode Linearity with V_1 = 1.23 V, V_2 = 0 V and T_A = +85°C

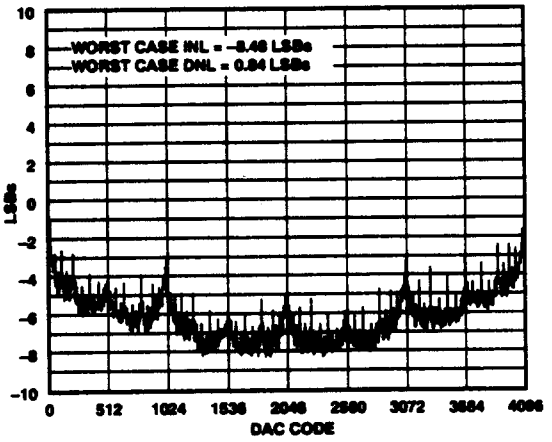

Figure A5. Voltage-Switching Mode Linearity with V_1 = 1.23 V, V_2 = 1.23 V and T_A = +25°C

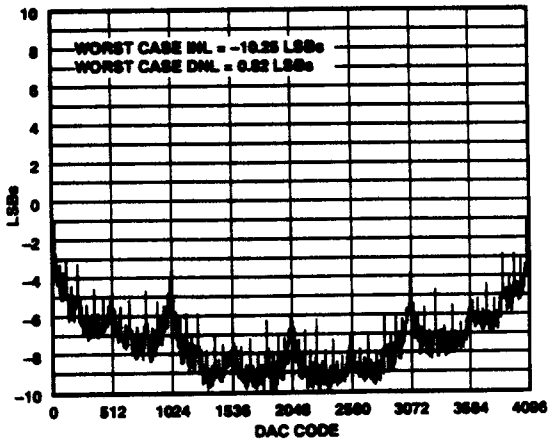

Figure A6. Voltage-Switching Mode Linearity with V_1 = 1.23 V, V_2 = 1.23 V and T_A = +85°C