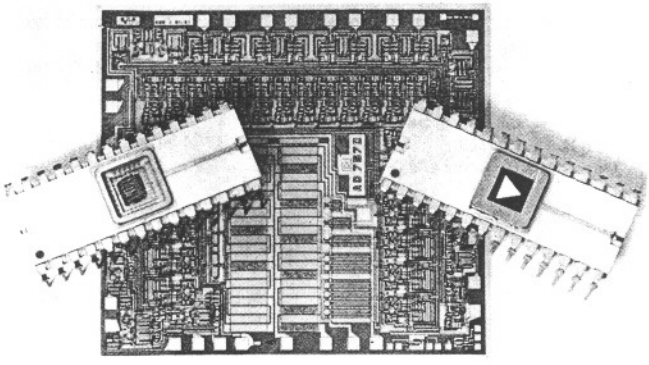
CMOS 10-Bit Monolithic A/D Converter

AD7570

FEATURES

- 8- and 10-Bit Resolution
- 20μs Conversion Time
- Microprocessor Compatibility
- Very Low Power Dissipation
- Parallel and Serial Outputs
- Ratiometric Operation
- TTL/DTL/CMOS Logic Compatibility
- CMOS Monolithic Construction



GENERAL DESCRIPTION

The AD7570 is a monolithic CMOS 10-bit successive approximation A/D converter on a 120 by 135 mil chip, requiring only an external comparator, reference and passive clocking components. Ratiometric operation is inherent, since an extremely accurate multiplying DAC is used in the feedback loop.

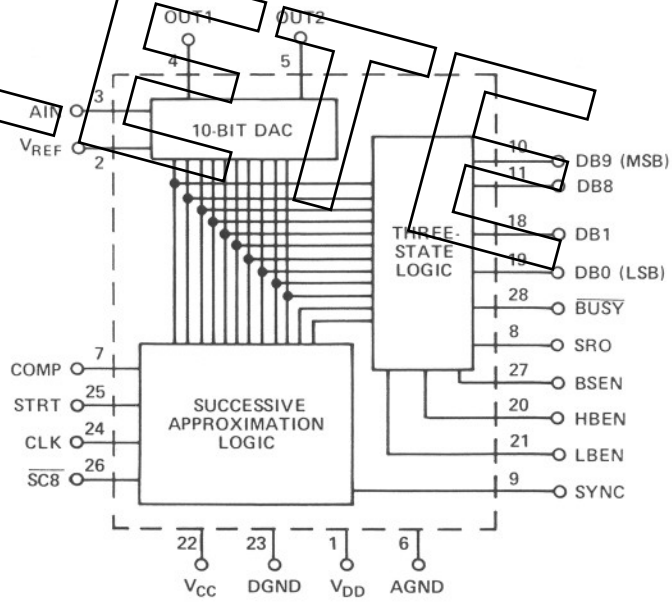
The AD7570 parallel output data lines and Busy line utilize three-state logic to permit bussing with other A/D output and control lines or with other I/O interface circuitry. Two enables are available: one controls the two MSBs; the second controls the remaining 8 LSBs. This feature provides the control interface for most microprocessors which can accept only an 8-bit byte.

The AD7570 also provides a serial data output line to be used in conjunction with the serial synchronization line. The clock can be driven externally or, with the addition of a resistor and a capacitor, can run internally as high as 0.6MHz allowing a total conversion time (8 bits) of typically 20μs. An 8-bit short cycle control pin stops the clock after exercising 8 bits, normally used for the "J" version (8-bit resolution).

The AD7570 requires two power supplies, a +15V main supply and a +5V (for TTL/DTL logic) to +15V (for CMOS logic) supply for digital circuitry. Both analog and digital grounds are available.

The AD7570 is a monolithic device using a proprietary CMOS process featuring a double layer metal interconnect, on-chip thin-film resistor network and silicon nitride passivation ensuring high reliability and excellent long term stability.

FUNCTIONAL DIAGRAM



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SPECIFICATIONS (V_{DD} = +15V, V_{CC} = +5V, V_{REF} = ±10V unless otherwise noted)

PARAMETER[1]	VERSIONS	T_A = +25°C	OVER SPECIFIED TEMP. RANGE	TEST CONDITIONS
ACCURACY				
Resolution	J	8 Bits min	8 Bits min	$\overline{SC8}$ = Logic "0"
	L	10 Bits min	10 Bits min	$\overline{SC8}$ = Logic "1"
Relative Accuracy	J, L	±1/2LSB max	±1/2LSB max	f_{CLK} = 100kHz
Differential Nonlinearity	J, L	1LSB max	1LSB max	See Figure 5
Gain Error	J, L	0.3% Reading typ		
Gain Temperature Coefficient	J, L	5ppm Reading per °C typ	10ppm Reading per °C max	
ANALOG INPUTS				
Analog Input Resistance	J, L	10kΩ typ	5kΩ min, 20kΩ max	
Analog Input Resistance Tempco	J, L	-150ppm/°C typ		
Reference Input Resistance	J, L	10kΩ typ	5kΩ min, 20kΩ max	
Reference Input Resistance Tempco	J, L	-150ppm/°C typ		
ANALOG OUTPUTS				
Output Leakage Current (OUT1, OUT2)	J, L	10nA typ	200nA max	$V_{OUT1, 2}$ = 0V DB0 through DB9 = Logic "1"
Output Capacitance OUT1	J, L	120pF typ		
OUT2	J, L	40pF typ		
OUT1	J, L	40pF typ		DB0 through DB9 = Logic "0"
OUT2	J, L	120pF typ		
DIGITAL INPUTS				
V_{INL}[2]	J, L	+1.4V typ, +0.8V max	+0.8V max	V_{CC} = +5V
V_{INH}[2]	J, L	+2.4V min, +1.4V typ	+2.4V min	
V_{INL}[2]	J, L	+1.5V max	+1.5V max	V_{CC} = +15V
V_{INH}	J, L	+13.5V min	+13.5V min	
I_{INL}, I_{INH}[3]	J, L	±0.1µA typ, ±10µA max		V_{IN} = 0 to V_{CC}
CLK Input Current	J, L	+0.4mA typ, +1mA max		During Conversion V_{CC} = +5V; 2.4V ≤ V_{IN} ≤ V_{CC}
CLK Input Current	J, L	+1.7mA typ, +3mA max		During Conversion V_{CC} = +15V; 10V ≤ V_{IN} ≤ V_{CC}
CLK Input Current	J, L	±1µA typ		V_{CC} = +5V to +15V Conversion Complete or CLK IN ≤ V_{INL}
C_{IN}	J, L	2pF typ		
DIGITAL OUTPUTS				
V_{OUTL}	J, L	+0.5V max	+0.8V max	V_{CC} = +5V, I_{SINK} = 1.6mA
V_{OUTH}	J, L	+2.4V min	+2.4V min	V_{CC} = +5V, I_{SOURCE} = 40µA
V_{OUTL}	J, L	+1.5V max	+1.5V max	V_{CC} = +15V, I_{SINK} = 3mA
V_{OUTH}	J, L	+13.5V min	+13.5V min	V_{CC} = +15V, I_{SOURCE} = 1mA
C_{OUT} (Floating) (SYNC, SRO, $\overline{BUSY}$, and DB0 through DB9)	J, L	5pF typ		V_{CC} = +5V to +15V SRO and SYNC; Conversion Complete $\overline{BUSY}$; BSEN = Logic "0" DB0–DB9; HBEN, LBEN = Logic "0"
I_{LKG} (Floating) (SYNC, SRO, $\overline{BUSY}$ and DB0 through DB9)		±5nA typ		V_{CC} = +5V to +15V SRO and SYNC; Conversion Complete $\overline{BUSY}$; BSEN = Logic "0" DB0–DB9; HBEN, LBEN = Logic "0" V_{OUT} = 0V and V_{CC}
DYNAMIC PERFORMANCE				
Conversion Time	J	20µs typ, 40µs max	40µs max	See Figure 5
	L	40µs typ, 120µs max	120µs max	
Internal CLK Frequency (See Figure 2, and Section 6 of Pin Function Description)	J, L	100kHz typ		V_{CC} = +5V; CLK Duty Cycle = 50%, R = 33k, C = 760pF
	J, L	100kHz typ		V_{CC} = +15V, CLK Duty Cycle = 50%, R = 10k; C = 2500pF
LBEN, HBEN Propagation Delay				V_{CC} = +5V
t_{ON}	J, L	650ns typ		LBEN, HBEN = 0V to +3V
t_{OFF}	J, L	200ns typ		Data Bit Load = 5k, 16pF Measured from 50% of Enable Input to 50% Point of Data Bit Output
BSEN Propagation Delay				V_{CC} = +5V
t_{ON}	J, L	450ns typ		BSEN = 0V to +3V
t_{OFF}	J, L	200ns typ		$\overline{BUSY}$ Load = 5k, 16pF Measured from 50% Point of BSEN Input Waveform to 50% Point of $\overline{BUSY}$ Output Waveform
Convert Start (STRT)[4] Pulse Duration Requirement	J, L	0.5µs min		

PARAMETER[1]	VERSIONS	T_A = +25°C	OVER SPECIFIED TEMP. RANGE	TEST CONDITIONS
POWER SUPPLIES				
V_{DD}	J, L	+5V to +15V typ		See Figures 3 and 4
V_{CC}	J, L	+5V to V_{DD} typ		
I_{DD}	J, L	0.2mA typ, 2mA max		V_{DD} = +15V, f_{CLK} = 0 to 100kHz Continuous Conversion (80% Duty Cycle)
I_{CC}	J, L	0.02mA typ, 2mA max		V_{CC} = +5V, f_{CLK} = 0 to 100kHz Continuous Conversion (80% Duty Cycle)
	J, L	0.1mA typ, 2mA max		V_{CC} = +15V, f_{CLK} = 0 to 100kHz Continuous Conversion (80% Duty Cycle)

[1] "J" version parameters specified for $\overline{SC8}$ = 0.
[2] V_{INL} and V_{INH} specifications applicable to all digital inputs except COMP. COMP terminal must be driven with CMOS levels (i.e., comparator output pullup must be tied to V_{CC}).
[3] I_{INL}, I_{INH} specifications not applicable to CLK terminal. See "CLK input current" in specifications table.
[4] STRT falling edge should not coincide with CLK in falling edge.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND . . . . . +17V
V_{CC} to GND. . . . . +17V
V_{CC} to V_{DD} . . . . . +0.4V
V_{REF} to GND. . . . . ±25V
Analog Input to GND. . . . . ±25V
Digital Input Voltage Range . . . . . V_{DD} to GND

I_{OUT1}, I_{OUT2} . . . . . -0.3V, V_{DD}
Power Dissipation (package)
up to +50°C. 1000mW
Derate above +50°C by. . . . . 10mW/°C
Operating Temperature. . . . . -25°C to +85°C
Storage Temperature . . . . . -65°C to +150°C

CAUTION:

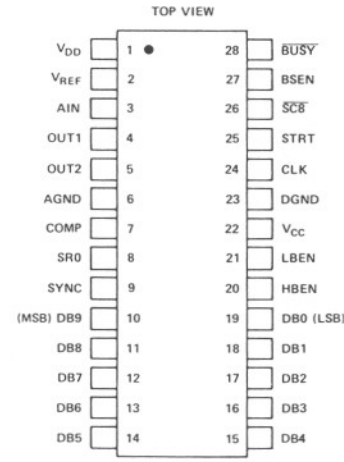
1. Do not apply voltages higher than V_{CC} or less than GND to any input/output terminal except V_{REF} or AIN.
2. The digital control inputs are zener protected; however permanent damage may occur on unconnected units under high energy electrostatic fields. Keep unused units in conductive foam at all times.
3. V_{CC} should never exceed V_{DD} by more than 0.4V, especially during power ON or OFF sequencing.

ORDERING INFORMATION

Resolution	Temperature Range
	-25°C to +85°C
8-Bit	AD7570J
10-Bit	AD7570L

Suffix D: Ceramic Package

PIN CONFIGURATION



TYPICAL PERFORMANCE CHARACTERISTICS

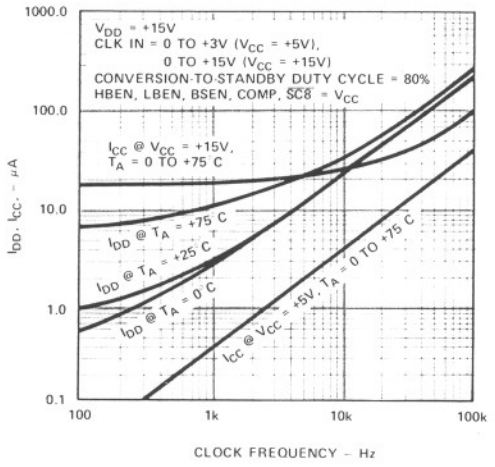


Figure 1. I_{DD}, I_{CC} vs. f_{CLK} at Different Temperatures

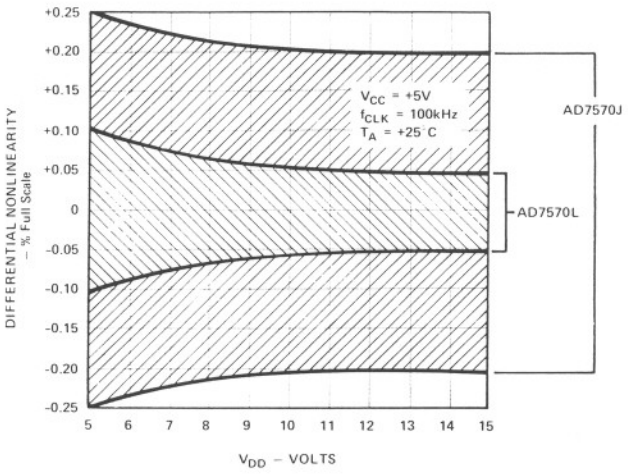


Figure 3. Differential Nonlinearity vs. V_{DD}

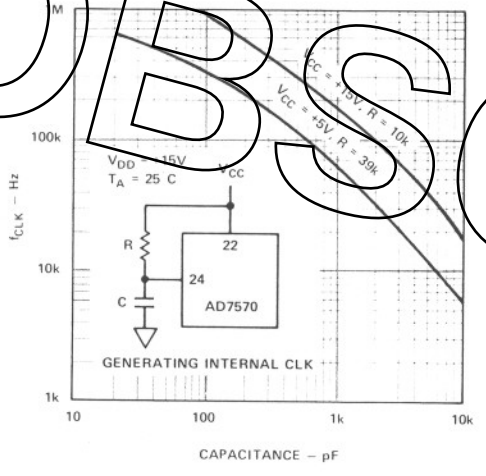


Figure 2. f_{CLK} vs. R and C at V_{CC} = +5V, +15V

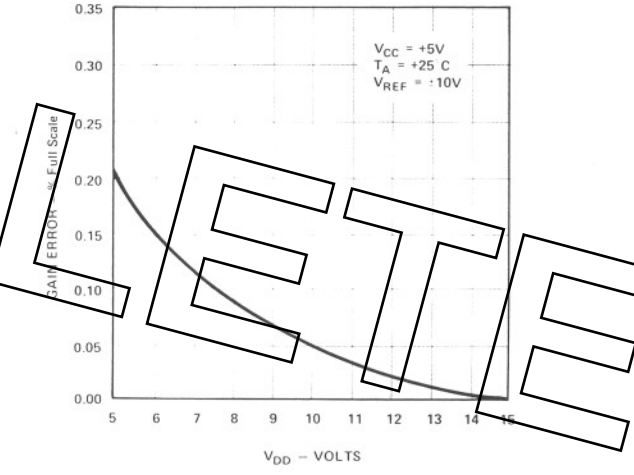


Figure 4. Gain Error vs. V_{DD} (Normalized for V_{DD} = 15V)

TEST CIRCUITS

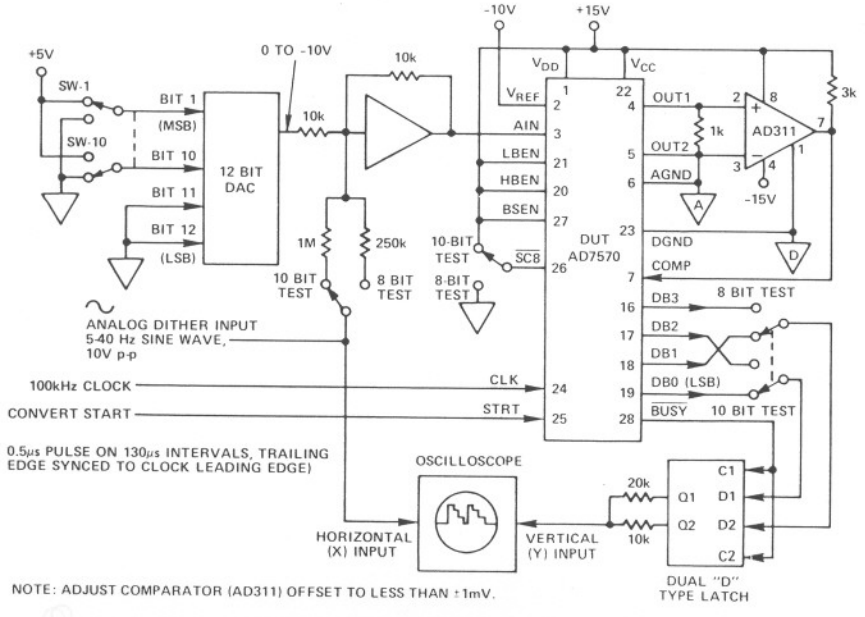
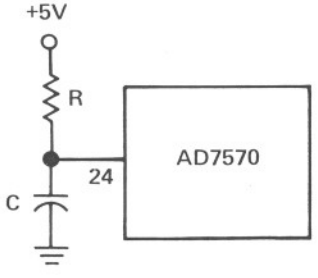


Figure 5. Dynamic Crossplot Accuracy Test

PIN FUNCTION DESCRIPTION

INPUT CONTROLS

1. Convert Start (pin 25 – STRT)
   When the start input goes to Logical "1", the MSB data latch is set to Logic "1" and all other data latches are set to Logic "0". When the start input returns low, the conversion sequence begins. The start command must remain high for at least 500 nanoseconds. If a start command is reinitiated *during* conversion, the conversion sequence starts over.
2. High Byte Enable (pin 20 – HBEN)
   This is a three-state enable for the bit 9 (MSB) and bit 8. When the control is low, the output data lines for bits 9 and 8 are floating. When the control is high, digital data from the latches appears on the data lines.
3. Low Byte Enable (pin 21 – LBEN)
   Same as High Byte Enable pin, but controls bits 0 (LSB) through 7.
4. Busy Enable (pin 27 – BSEN)
   This is an interrogation input which requests the status of the converter, i.e., conversion in process or convert complete. The converter status is addressed by applying a Logic "1" to the Busy Enable. (See Busy under Output Functions.)
5. Short Cycle 8 Bits (pin 26 – $\overline{SC8}$)
   With a Logic "0" input, the conversion stops after 8 bits, reducing the conversion time by 2 clock periods. This control should be exercised for proper operation of the "J" version. When a Logic "1" is applied, a complete 10-bit conversion takes place ("L" version).
6. Clock (pin 24 – CLK)
   With an external RC connected, as shown in the figure below, clock activity begins upon receipt of a Convert-Start command to the A/D and ceases upon completion of conversion. An external clock (CMOS or TTL/DTL levels) can directly drive the clock terminals, if required. Figure 2 shows the internal CLK frequency versus R and C. If V_{CC} is <4.75V, the internal CLK will not operate.



Generating Internal Clock Frequency

7. V_{DD} (pin 1)
   V_{DD} is the positive supply for all analog circuitry plus some digital logic circuits that are not part of the TTL compatible input/output lines (back-gates to the P-channel devices). Nominal supply voltage is +15V.
8. V_{CC} (pin 22)
   V_{CC} is the logic power supply. If +5V is used, all control inputs/outputs (with the exception of comparator terminal) are DTL/TTL compatible. If +15V is applied, control inputs/outputs are CMOS compatible.

OUTPUT FUNCTIONS

1. Busy (pin 28 – $\overline{BUSY}$)
   The Busy line indicates whether conversion is complete or in process. Busy is a three-state output and floats until the Busy-Enable line is addressed with a Logic "1". When addressed, Busy will indicate either a "1" (conversion complete) or a "0" (conversion in process).
2. Serial Output (pin 8 – SRO)
   Provides output data in serial format. Data is available only during conversion. When the A/D is not converting, the Serial Output line "floats." The Serial Sync (see next function) *must* be used, along with the Serial Output terminal to avoid misinterpreting data.
3. Serial Synchronization (pin 9 – SYNC)
   Provides 10 positive edges, which are synchronized to the Serial Output pin. Serial Sync is floating if conversion is not taking place.

Note that all digital inputs/outputs are TTL/DTL compatible when V_{CC} is +5V, and CMOS compatible when V_{CC} is +15V.

PIN NO.	MNEMONIC	FUNCTION
1	V_{DD}	Positive Supply (+15V)
2	V_{REF}	Voltage REFerence (±10V)
3	AIN	Analog INput
4	OUT1	DAC Current OUTput 1
5	OUT2	DAC Current OUTput 2
6	AGND	Analog GrouND
7	COMP	COMParator
8	SRO	SeRial Output
9	SYNC	Serial SYNChronization
10	DB9	Data Bit 9 (MSB)
11	DB8	Data Bit 8
12	DB7	Data Bit 7
13	DB6	Data Bit 6
14	DB5	Data Bit 5
15	DB4	Data Bit 4
16	DB3	Data Bit 3
17	DB2	Data Bit 2
18	DB1	Data Bit 1
19	DB0	Data Bit 0 (LSB)
20	HBEN	High Byte ENable
21	LBEN	Low Byte ENable
22	V_{CC}	Logic Supply (+5V to +15V)
23	DGND	Digital GrouND
24	CLK	CLocK
25	$\overline{STRT}$	STaRT
26	$\overline{SC8}$	Short Cycle 8 Bits
27	$\overline{BSEN}$	BuSy ENable
28	$\overline{BUSY}$	BUSY

Table 1. Function Table

FUNCTIONAL ANALYSIS

BASIC DESCRIPTION

The AD7570 is a monolithic CMOS A/D converter which uses the successive approximations technique to provide up to 10 bits of digital data in a serial and parallel format. Most A/D applications require the addition of only a comparator and a voltage or current reference.

In the successive approximations technique, successive bits, starting with the most significant bit (DB9) are applied to the input of the D/A converter. The DAC output is then compared to the unknown analog input voltage (AIN) using a zero crossing detector (comparator). If the DAC output is greater than AIN, the data latch for the trial bit is reset to zero, and the next smaller data bit is tried. If the DAC output is less than AIN, the trial data bit stays in the "1" state, and the next smaller data bit is tried.

Each successive bit is tried, compared to AIN, and set or reset in this manner until the least significant bit (DB0) decision is made. At this time, the AD7570 output is a valid digital representation of the analog input, and will remain in the data latches until another convert start (STRT) is applied.

TIMING DESCRIPTION

Figure 6 is the AD7570 timing diagram, showing the successive trials and decisions for each data bit. When convert start (STRT) goes HIGH, the MSB(DB9) is set to the Logic "1" state, while DB0 through DB8 are reset to the "0" state.

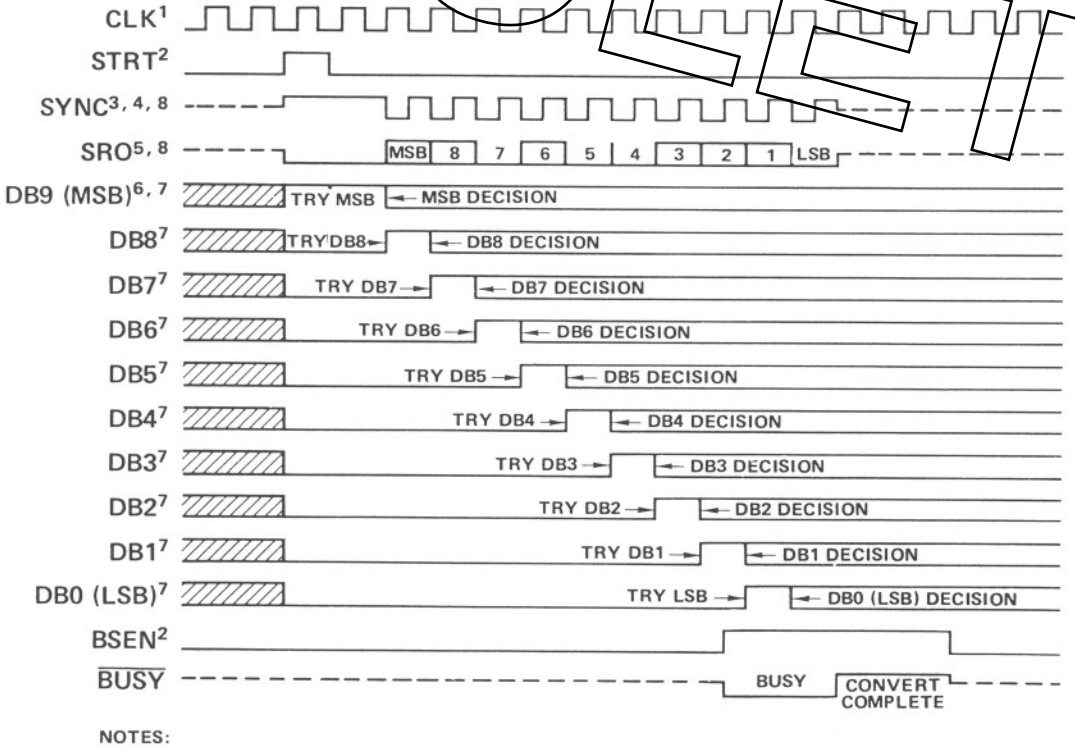
Two clock *pulses* plus 200ns after STRT returns LOW, the MSB decision is made, and DB8 is tried. Each succeeding trial and decision is made at t_{CLK} + 200ns.

Serial NRZ data is available during conversion at the SRO terminal. SYNC provides 10 positive edges which occur in the middle of each serial output bit. SYNC out must be used in conjunction with SRO to avoid misinterpretation of data. Both SYNC and SRO "float" when conversion is not taking place.

8-BIT SHORT CYCLE NOTES

If the AD7570 is short cycled to 8 bits ($\overline{SC8}$ = 0V), the following will occur:

1. The SYNC terminal will provide 8, instead of 10, positive output pulses.
2. DB1 goes "high" coincident with the LSB (DB2 is the LSB when short cycled to 8 bits) decision, and remains high until another STRT is initiated. DB0 remains in the "0" state.
3. $\overline{BUSY}$ goes "high" one clock period after the DB2 (DB2 is the LSB when short cycled) decision is made.



NOTES:
1. INTERNAL CLOCK RUNS ONLY DURING CONVERSION CYCLE (EXTERNAL CLOCK SHOWN).
2. EXTERNALLY INITIATED.
3. SERIAL SYNC LAGS $\overline{CLOCK}$ BY ≈ 200ns.
4. DOTTED LINES INDICATE "FLOATING" STATE.
5. FOR ILLUSTRATIVE PURPOSES, SERIAL OUT SHOWN AS 1101001110.
6. CROSS HATCHING INDICATES "DON'T CARE" STATE.
7. SET AND RESET OF OUTPUT DATA BITS LAGS CLOCK POSITIVE EDGE BY ≈ 200ns.
8. SHOWN FOR $\overline{SC8}$ = 1.

Figure 6. AD7570 Conversion Timing Sequence

DYNAMIC PERFORMANCE

The upper clock frequency limitation (hence the conversion speed limitation) of the AD7570 is due to the output settling characteristics of the current weighting DAC in conjunction with the propagation delay of the comparator, not to speed limitations in the digital logic.

DAC EQUIVALENT CIRCUIT

The D/A converter section of the AD7570 is a precision 10-bit multiplying DAC. The simplified DAC circuit, shown in Figure 7, consists of ten single-pole-double-throw current steering switches and an "inverted" R-2R current weighting network. (For a complete description of the DAC, refer to the AD7520 data sheet.)

The output resistance and capacitance at OUT1 (and OUT2) are code dependent, exhibiting resistive variations from 0.5 "R" to 0.75 "R", and capacitive variations from 40pF to 120pF.

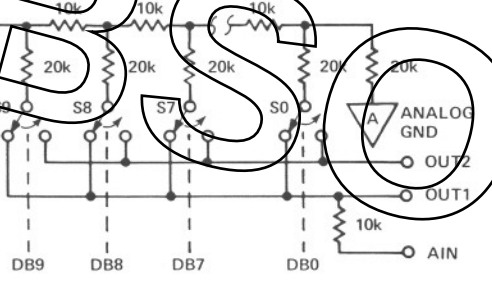


Figure 7. DAC Circuit

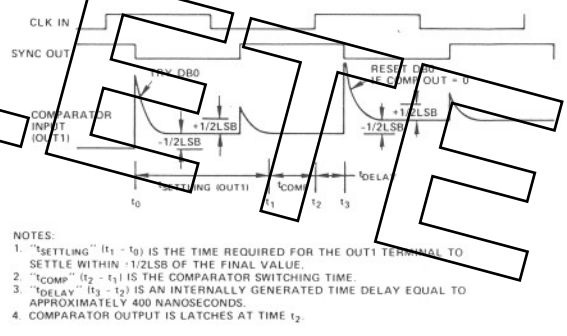
SETTLING TIME ANALYSIS

Due to the changing C_{OUT1} and R_{OUT1}, the time constant on OUT1 falls anywhere between 250 and 900ns, depending on the instantaneous state of the AD7570 digital output code.

Worst case settling requirements occur when a trial bit causes the OUT1 terminal to charge towards a final value which is precisely 1/2 LSB beyond zero crossing. When this occurs, the trial bit must settle and remain within 1/2 LSB of final value, or an incorrect decision will be made by the comparator.

For 10-bit accuracy, the first MSB must settle to within 0.1% of final value; the second MSB to within 0.2%. The LSB settling requirement is only 50% of the LSB value. Figure 8 illustrates the settling time available during a given clock period. The pulse shown on the OUT1 terminal falling midway between t_0 and t_3 is a feedthrough from internal clock mechanisms and is due primarily to bonding wire and header capacitance. Two methods may be used to reduce the OUT1 settling time:

1. Load OUT1 with a 1k resistor. This reduces the time constant by a factor of 10. Further reduction of the 1kΩ load reduces the amount of comparator overdrive, thus increasing the comparator propagation delay, resulting in a reduction of available settling time (t1 - t0 on Figure 8).
2. Use a zero input impedance comparator. Figure 9 illustrates a comparator circuit which has an input impedance of approximately 26Ω. Proper circuit layout will provide 10-bit accuracy for clock frequencies >500kHz.



NOTES:
1. "$t_{SETTLING}$" (t_1 - t_0) IS THE TIME REQUIRED FOR THE OUT1 TERMINAL TO SETTLE WITHIN ±1/2LSB OF THE FINAL VALUE.
2. "t_{COMP}" (t_2 - t_1) IS THE COMPARATOR SWITCHING TIME.
3. "t_{DELAY}" (t_3 - t_2) IS AN INTERNALLY GENERATED TIME DELAY EQUAL TO APPROXIMATELY 400 NANOSECONDS.
4. COMPARATOR OUTPUT IS LATCHES AT TIME t_2.

Figure 8. Expanded Timing Diagram

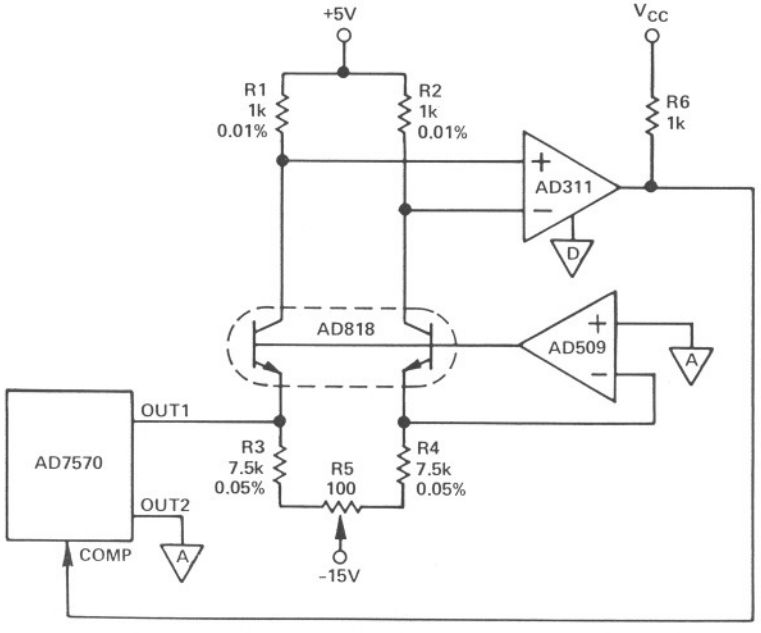


Figure 9. Current Comparator With Low Input Impedance

OPERATION GUIDELINES

UNIPOLAR BINARY OPERATION

Figure 10 shows the circuit connections required for unipolar analog inputs. If *positive* analog inputs are to be quantized, V_{REF} must be *negative*, and the OUT1 (pin 4) terminal of the AD7570 must be connected to the "+" comparator input. For *negative* analog inputs, V_{REF} must be *positive*, and the OUT1 terminal connected to the "–" input of the comparator.

For clarity, the digital control functions have been omitted from the diagram. For proper use of the digital input/output control functions, refer to the pin function description.

The input voltage/output code relationship for unipolar operation is shown in Table 2. Due to the inherent multiplying capability of the internal D/A converter, the AD7570 can accurately quantize full scale ranges of 10V to 1V. It should be noted, however, that for smaller full scale ranges, the resolution and speed limitations of the comparator impose a limitation on the maximum conversion rate.

BIPOLAR (OFFSET BINARY) OPERATION

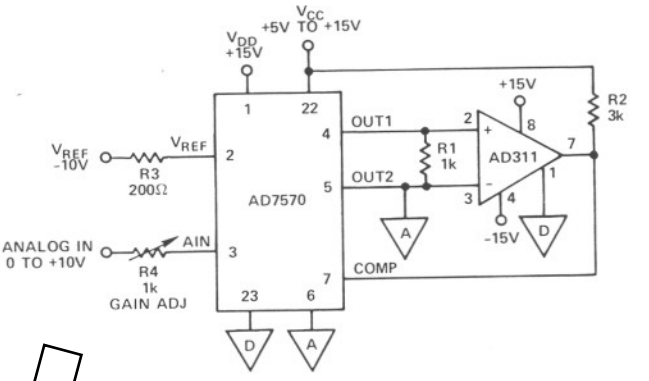
Figure 11 shows the AD7570 configured for offset binary (modified 2's complement) operation. Input voltage/output codes are shown in Table 3.

Amplifier A1, in conjunction with resistors R1, R2, and R3, offsets the bipolar analog input by full scale, and reduces its gain by a factor of 2. The analog signal applied to the AIN terminal is, therefore, a unipolar signal of 0 to +V or 0 to –V, depending on the polarity of V_{REF}.

ADJUSTMENT PROCEDURES UNIPOLAR OPERATION

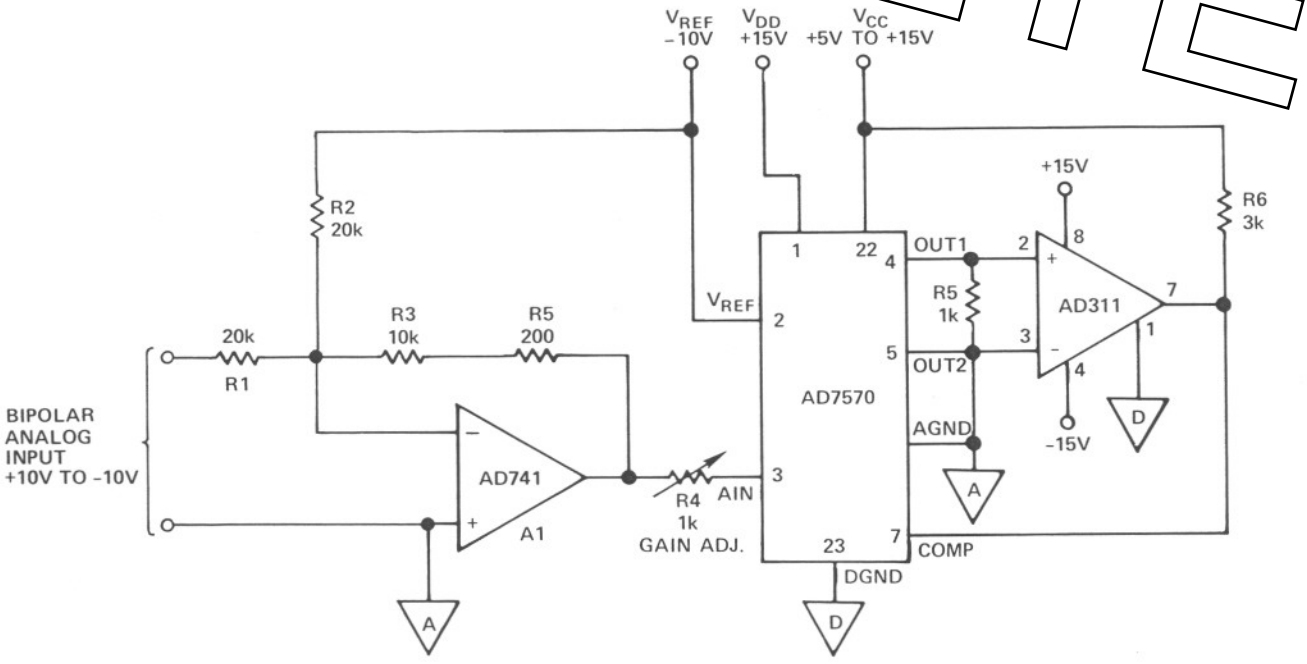
Gain Adjustment

1. Apply continuous start commands to the STRT input of the AD7570.
2. Apply full scale minus 1-1/2LSB to AIN.
3. Observe the SRO terminal as described under zero offset procedure above, and adjust the gain potentiometer (R4) until the LSB flickers between 0 and 1, and all other data bits equal "1". An alternate method is to adjust V_{REF} instead of using R4.



NOTE:
IF POSITIVE V_{REF} IS USED, THE ANALOG INPUT RANGE IS 0 TO $-V_{REF}$, AND THE COMPARATOR'S (–) INPUT SHOULD BE CONNECTED TO OUT1 (PIN 4) OF THE AD7570.

Figure 10. Unipolar Operation



NOTE: IF POSITIVE V_{REF} IS USED, CONNECT MINUS INPUT OF COMPARATOR TO OUT1 (PIN 4) OF THE AD7570.

Figure 11. Bipolar Operation

Table 2. Unipolar Operation

Analog Input (AIN) Notes 1, 2, 3	Digital Output Code MSB LSB
FS – 1LSB	1 1 1 1 1 1 1 1 1 1
FS – 2LSB	1 1 1 1 1 1 1 1 1 0
3/4 FS	1 1 0 0 0 0 0 0 0 0
1/2 FS + 1LSB	1 0 0 0 0 0 0 0 0 1
1/2 FS	1 0 0 0 0 0 0 0 0 0
1/2 FS – 1LSB	0 1 1 1 1 1 1 1 1 1
1/4 FS	0 1 0 0 0 0 0 0 0 0
1LSB	0 0 0 0 0 0 0 0 0 1
0	0 0 0 0 0 0 0 0 0 0

NOTES:
1. Analog inputs shown are nominal center values of code.
2. "FS" is full scale, i.e., $(-V_{REF})$.
3. For 8-bit operation, 1LSB equals $(-V_{REF})(2^{-8})$; for 10-bit operation, 1LSB equals $(-V_{REF})(2^{-10})$.

Table 3. Bipolar Operation

Analog Input (AIN) Notes 1, 2, 3	Digital Output Code MSB LSB
+(FS – 1LSB)	1 1 1 1 1 1 1 1 1 1
+(FS – 2LSB)	1 1 1 1 1 1 1 1 1 0
+(1/2 FS)	1 1 0 0 0 0 0 0 0 0
+(1LSB)	1 0 0 0 0 0 0 0 0 1
0	1 0 0 0 0 0 0 0 0 0
–(1LSB)	0 1 1 1 1 1 1 1 1 1
–(1/2 FS)	0 1 0 0 0 0 0 0 0 0
–(FS – 1LSB)	0 0 0 0 0 0 0 0 0 1
–FS	0 0 0 0 0 0 0 0 0 0

NOTES:
1. Analog inputs shown are nominal center values of code.
2. "FS" is full scale; i.e., (V_{REF}).
3. For 8-bit operation, 1LSB equals $(-V_{REF})(2^{-7})$; for 10-bit operation, 1LSB equals $(-V_{REF})(2^{-9})$.

ADJUSTMENT PROCEDURES BIPOLAR OPERATION

Gain Adjustment

1. Apply continuous start commands to the STRT input of the AD7570.
2. Apply 1-1/2LSB less than positive full scale (FS = V_{REF}) to the bipolar analog input of Figure 11.
3. Trim the gain potentiometer R4 for a flickering LSB, and all other data bits equal to Logic "1". Observe the SRO terminal, as described in zero offset procedure above.

APPLICATION HINTS

1. Unused CMOS digital inputs should be tied to their appropriate logic level and not left floating. Open digital inputs may cause undesired digital activity in the presence of noise.
2. Analog and digital grounds should have separate returns.
3. Load the OUT1 terminal with a 1k resistor to reduce the time constant when operating at clock frequencies >50kHz.
4. For 10-bit operation, the comparator offset should be adjusted to less than 1mV. Each millivolt of comparator offset will cause approximately 0.015% of differential nonlinearity when a 10V reference is used.
5. The comparator input and output should be isolated to prevent oscillations due to stray capacitance. (See layout on the next page).
6. If an external clock is used, the negative transition of STRT should not coincide with the trailing edge of the clock input.

OPERATING PRECAUTIONS

1. Do not allow V_{CC} to exceed V_{DD}. In cases where V_{CC} could exceed V_{DD}, the diode protection scheme in Figure 12 is recommended.
2. Do not apply voltages greater than V_{CC} or lower than ground to any digital *output* from sources which can supply >20mA.
3. Do not apply voltages (from a source which can supply more than 5mA) lower than ground to the OUT1 or OUT2 terminal (see Figure 12).

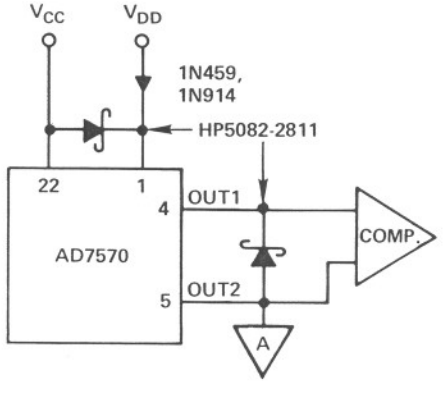
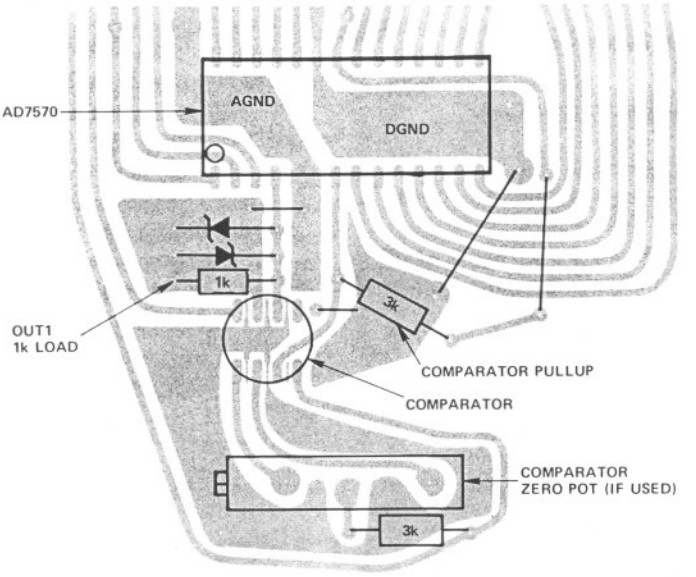


Figure 12. Diode Protection Scheme

OPTIMIZED LAYOUT



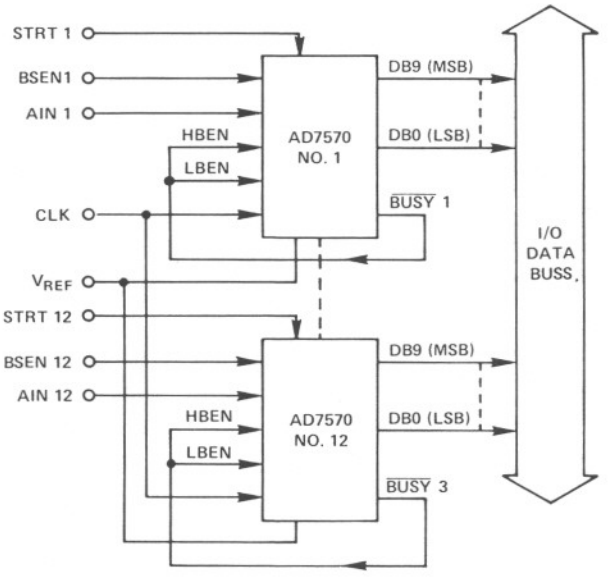
NOTES:
1. ALL PC TRACES ON BOTTOM OF BOARD.
2. LAYOUT SHOWN TERMINATES OUT1 INTO + INPUT OF AD311 TYPE COMPARATOR. V_{REF} = +10V, AIN = 0 TO +10V).

Figure 13. PC Layout (Top View)

BUSING MULTIPLE AD7570 OUTPUTS

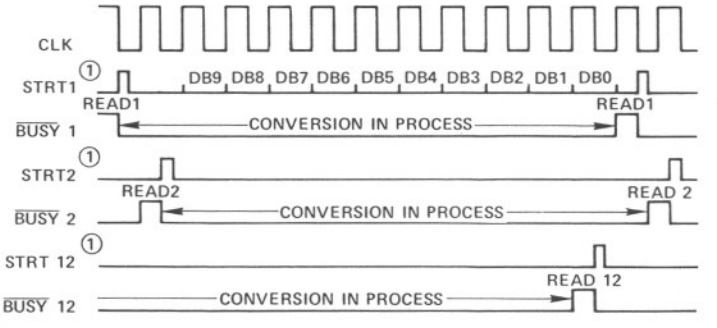
Several AD7570's may be paralleled to a data bus to provide an A/D converter per analog channel, this providing increased system throughput rate. For example, Figure 14 shows such a system for 12 AD7570's in parallel.

The three-state output logic enables of each AD7570 is controlled by its own BUSY (status) outputs. Thus, data is available at the A/D output only after conversion is complete, and until another "convert start" is initiated. The timing diagram of Figure 15 illustrates how the STRT signals of the twelve AD7570's might be staggered to provide a total system throughput twelve times as great as the classic method of data acquisition (an analog multiplexer feeding multichannel analog data to a single A/D converter).



NOTE: BSEN ON EACH AD7570 IS "ENABLED" (LOGIC 1).

Figure 14. Busing Multiple AD7570's



NOTE: STRT SIGNAL 0.5μs PULSE WIDTH, LEADING EDGE SYNCHRONIZED TO CLK TRAILING EDGE.

Figure 15. Timing Diagram

MICROPROCESSOR INTERFACE

Since most 8-bit microprocessors utilize a bidirectional data bus, each input peripheral (such as the AD7570) must be capable of isolating itself from the data bus when other I/O devices, memory, or the CPU takes control of the bus. The AD7570 output data and status (BUSY) lines all utilize three-state logic to provide this requirement.

Figure 16 illustrates a method of interfacing a TTY keyboard and printer to the AD7570, using an 8080 microprocessor as the interface controller.

The program (stored in Read Only Memory) waits for a keystroke on the TTY keyboard. When a keystroke is detected, an A/D conversion is started. When conversion is complete, the 8080 reads in the binary data from the AD7570, converts it to ASCII, and prints out the decimal number (preceded by a carriage return and line feed) on the teletype printer.

More specifically, the main sequence of events would be as follows:

1. When a TTY keystroke is detected by the CPU (via the UAR/T Receiver), a "convert start" (STRT) is applied to the AD7570.
2. BSEN is enabled, placing BUSY (conversion status) on the data bus. When the 8080 detects BUSY = 1, conversion is complete, and BSEN is disabled, causing BUSY to return to its floating state.
3. LBEN is enabled, and the eight least significant data bits (DB0-DB7) are applied to the data bus for subsequent transfer to the 8080. When the data transfer is complete, LBEN is disabled, and DB0-DB7 return to their floating state.
4. HBEN is enabled, and the two most significant AD7570 data bits (DB8 and DB9) are applied to the data bus for subsequent transfer to the 8080. When the data transfer is complete, HBEN is disabled, and DB8 and DB9 return to their floating state.
5. The 8080 (in conjunction with the programmed Read Only Memory) performs a binary to decimal conversion.
6. $\overline{\text{SWE}}$ (Status Word Enable) on the UAR/T transmitter is enabled, applying XBMT (Transmitter Buffer Empty) to the data bus. When a Logic "1" is detected by the 8080, $\overline{\text{SWE}}$ is disabled, and XBMT returns to a floating state.
7. TDS (Transmitter Data Strobe) strobes the converted decimal number into the UAR/T transmitter for subsequent serial clocking into the keyboard.

The interface scheme shown below is only one example of a myriad of possible data acquisition/control systems which could conveniently use the AD7570 to provide digital data to a microprocessor or minicomputer bus.

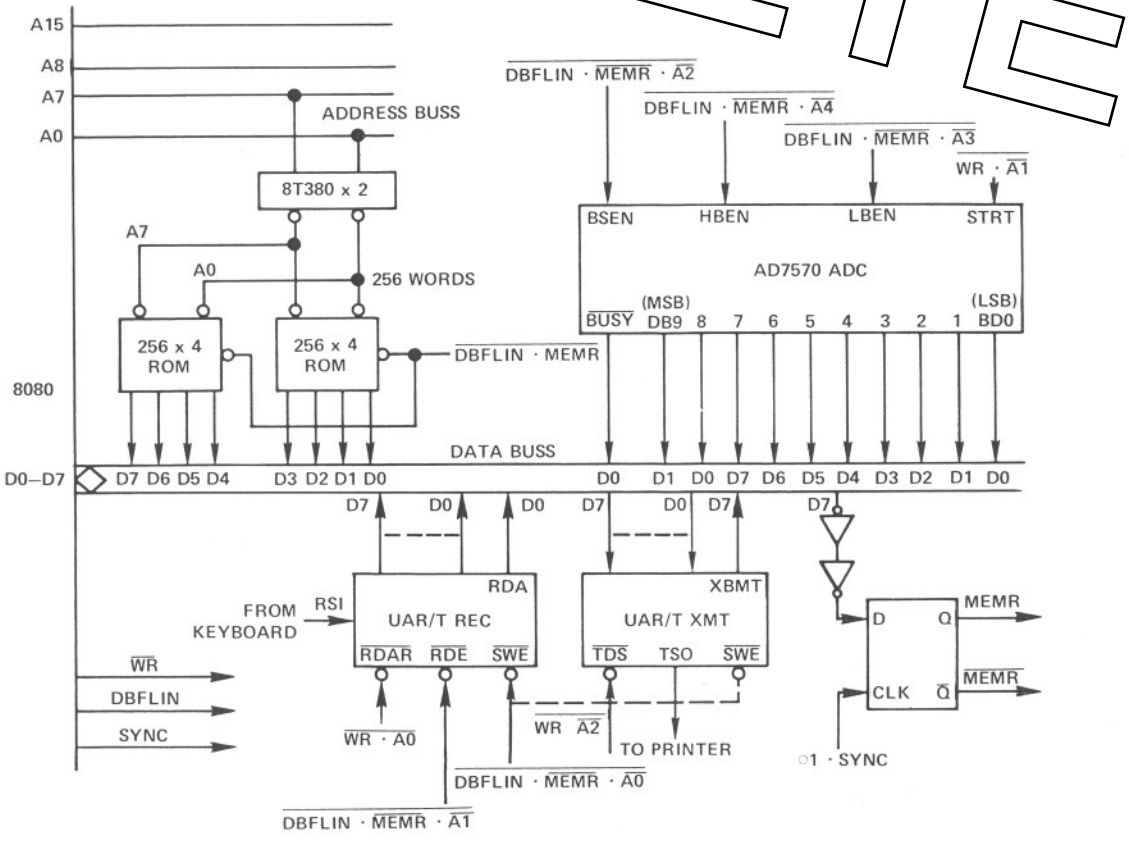


Figure 16. Microprocessor Controlled TTY/ADC Interface

TERMINOLOGY

Resolution
Resolution is the relative value of the LSB, or 2^{-n} for binary devices, for n-bit converters. It may be expressed as 1 part in 2^n, as a percentage, in parts-per-million, or simply by "n bits."

Relative Accuracy
Relative accuracy error is the difference between the nominal and actual ratios to full scale of the analog value corresponding to a given digital input, independently of the full-scale calibration. This error is a function of the linearity of the converter, and is usually specified at less than ±1/2LSB.

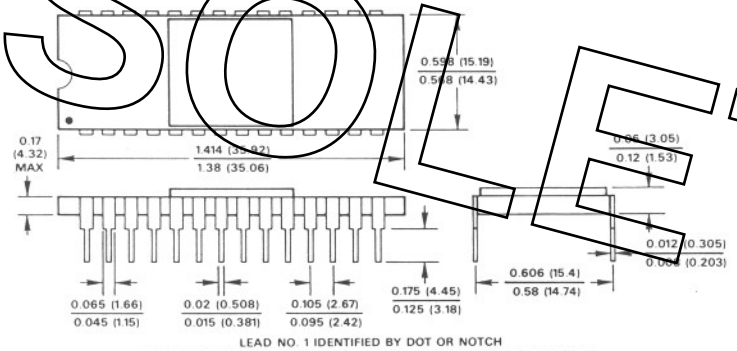
Gain Error
The "gain" of a converter is that analog scale factor setting that establishes the nominal conversion relationship, e.g., 10V full scale. It is adjusted either by setting the feedback resistor of a DAC, the input resistor in a current-comparing ADC, or the reference (voltage or current).

Differential Nonlinearity
In a converter, differential linearity error describes the variation in the analog value of transitions between adjacent pairs of digital numbers, over the full range of the digital input or output. If each transition is equal to its neighbors (i.e., 1LSB), the *differential nonlinearity* is zero. If a transition differs from one of its neighbors by more than 1LSB (e.g., if, at the transition 011. .11 to 100. . .00, the MSB is low by 1.1LSB), a D/A converter can be *non-monotonic*, or an A/D converter using it may miss one or more codes. A specified maximum differential nonlinearity of 1LSB ensures that monotonic behavior exists.

Output Leakage Current
Current which appears at the OUT1 terminal when all digital output (DB0 through DB9) are LOW, or on the OUT2 terminal when all digital outputs are HIGH. The effect of output leakage current will be on the offset of the A/D converter.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH
LEADS ARE GOLD PLATED (50 MICROINCHES MIN) KOVAR OR ALLOY 42

28 Pin Ceramic Dip