ANALOG DEVICES

AN-223
APPLICATION NOTE

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AD7575 Operation with an Offset Signal Ground for Disk Drive Applications

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The AD7575 is a low cost, high speed, 8-bit sampling ADC with a built-in track/hold amplifier. It uses the successive approximation technique to achieve a fast conversion time of 5 μs. The internal track/hold amplifier allows full scale signals up to 50 kHz to be accurately sampled and digitized. Operating from a single +5 V supply, the device is ideal for single supply applications and has an input signal range from 0 V to 2 V_{REF}. The recommended reference voltage is +1.23 V giving an input range of 0 V to +2.46 V.

In many single supply disk drive applications, the signal conditioning circuitry is operated with a pseudo-ground. The pseudo-ground scheme is used to ensure linear operation of the conditioning circuitry over the complete input signal range. The signal swings around the pseudo-ground allowing adequate headroom between the signal extremities and the V_{DD}/0 V levels as illustrated in Figure 1.

In order to accommodate input signals which are referenced to a pseudo-ground, and yet maintain the full dynamic range, it is possible to bias the ADC signal ground (AGND pin) of the AD7575 to a potential above 0 V by an offset voltage, V_{OFFSET}. This results in an ADC input signal span of V_{OFFSET} to V_{OFFSET} +2.46 V. The pseudo-ground is, therefore, located midway between these signal extremes at V_{OFFSET} + V_{REF}. This corresponds to the midscale code in the ADC transfer function.

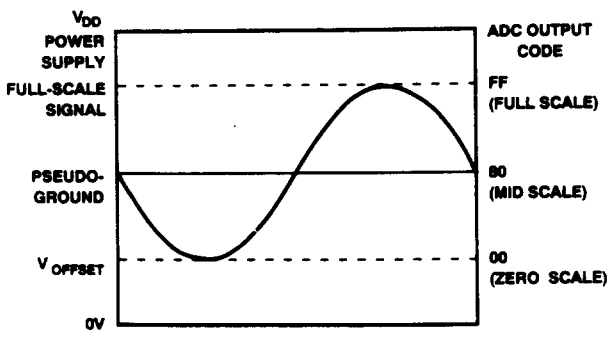

Figure 1. Pseudo-Ground Biasing Arrangement

The recommended biasing scheme for optimum performance from the AD7575 is shown in Figure 2. An AD589 provides the recommended reference voltage of +1.23 V. The AGND pin is biased up above the system ground using a single 5 V operational amplifier such as the TLC271. The amplifier is necessary in order to provide a low impedance signal ground return path. The amplifier must be capable of sinking the analog ground currents which flow in this line. In order to maintain a low dynamic impedance, both the V_{REF} pin and the AGND pin must be decoupled as shown in Figure 2. The optimum decoupling scheme uses 10 μF in parallel with 0.1 μF capacitors between V_{REF} and AGND terminals and a similar arrangement between AGND and DGND. The decoupling is essential in order to remove the ground current transients which occur during the ADC conversion process. Lower values of capacitance will result in degraded performance.

Using the circuit as shown in Figure 1, the performance of the part was evaluated under worst case conditions with V_{DD} = +4.75 V and with AGND bias voltages up to +0.7 V. With a bias voltage of +0.7 V, the input signal range of the ADC is from +0.7 V to +3.16 V or 1.93 V±1.23 V. No degradation in accuracy occurred with this bias voltage. Lower bias voltages may be used required but higher bias voltages may result in performance degradation.

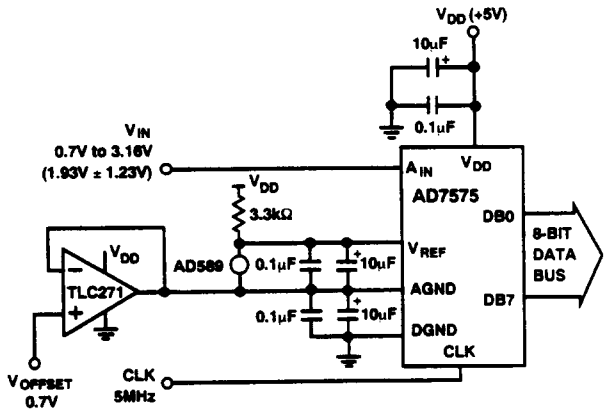

Figure 2. AD7575 AGND Bias Scheme