AD7569/AD7669 Operation with Offset Signal Grounds for Disk Drive Applications

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Single rail power supplies are the normal source of power for the electronics in many disk drive circuits. For a typical application such as head positioning, the sensor and control signals are often referenced to a voltage above ground potential. This is done in order to ensure that both the signal conditioning and the control circuitry is operating within its linear region. With any linear circuitry, such as op amps, there must be sufficient headroom between the signal extremes and the power supplies in order to maintain linear operation over the entire signal range. With single supply linear circuitry, there must be sufficient headroom between the minimum signal level and ground for the same reason. To achieve this, the linear circuitry is often operated with an offset or biased signal ground scheme which creates a pseudo signal ground above the system ground, and thereby provides the necessary headroom.

The sensor signals are normally converted to digital format for processing. When using standard ADCs, the offset signal level can result in a reduced dynamic range as several of the bottom codes are unused. Similarly, for the control signals which are generated using a DAC, a deadband can exist which again reduces the full dynamic range of the controller. This application note discusses how the AD7569/AD7669 analog I/O ports may be configured to operate with offset grounds and thereby maintain the full dynamic range of both the ADC and the DAC.

The AD7569/AD7669 is a complete monolithic 8-bit I/O system. A block diagram for the AD7569 is shown in Figure 1, while the AD7669 is shown in Figure 2. The

AD7569 contains an internal voltage reference, a sample/hold amplifier, an 8-bit ADC, an 8-bit DAC, a buffer amplifier plus all the digital control circuitry. The AD7669 is similar with the addition of an extra 8-bit DAC. Both parts may be operated from a single 5 V power supply with a choice of 0 to 1.25 V or 0 to 2.5 V signal ranges for both the ADC and the DAC. For further information on both parts consult the data sheet.

To accommodate input signals which are not referenced to 0 V but to some offset voltage, V_{OFFSET}, it is necessary to bias the ground of the ADC, $AGND_{ADC}$, with the same voltage offset. This ensures that no unused codes or deadband will exist at the bottom of the ADC code table. Additionally, in order to ensure that the full dynamic range of the ADC is utilized, the maximum input swing should equal the full-scale input swing of the ADC (either 1.25 V or 2.5 V). Similarly the DAC ground, $AGND_{DAC}$ may also be biased up to provide an offset voltage range for the control circuitry. The AD7569/AD7669 has independent ground connections for the ADC, DAC and the digital circuitry. These are designated $AGND_{ADC}$, $AGND_{DAC}$ and DGND. These ground connections are not internally connected together. In most applications these would be externally connected together, but in this application they may be utilized to provide an offset voltage range for the ADC or the DAC, or both. A novel internal voltage reference structure, which derives the reference with respect to V_{DD} instead of the more usual ground, is used in the part. This allows the flexibility to bias up $AGND_{ADC}$ or $AGND_{DAC}$ independently without severely affecting the accuracy of the converters.
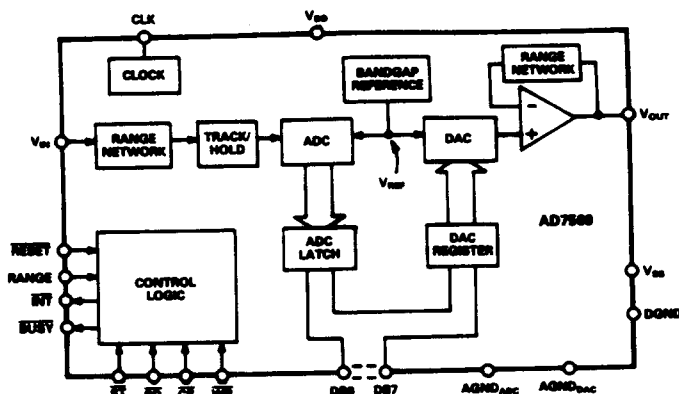
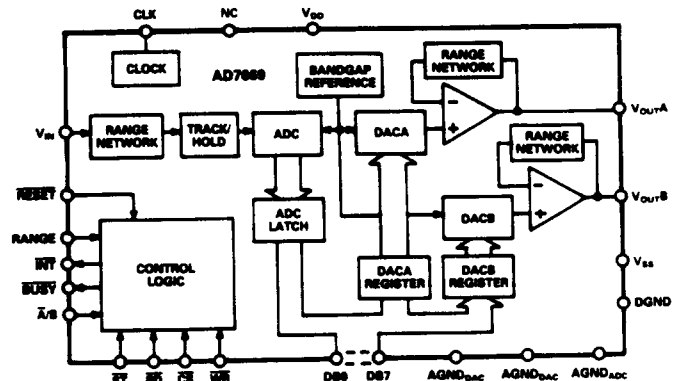

Figure 1. AD7569 Functional Block Diagram

Figure 2. AD7669 Functional Block Diagram

Figure 3 shows a typical disk drive application circuit using the AD7669. The circuit implements a servo control loop using the ADC to monitor the head position while the DAC is used to control the position. Separate ground offset voltages are applied but these could be connected together if required.
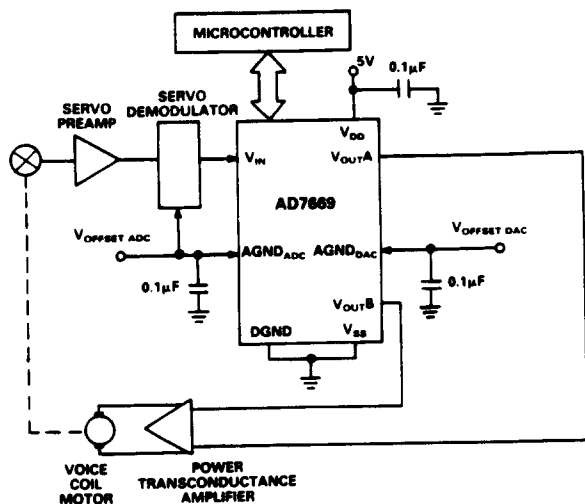

Figure 3. Servo Control Loop

The ADC input voltage range is shifted with respect to the system ground (DGND) by $V_{OFFSET\ ADC}$. This results in an offset transfer function as shown in Figure 4. The first code transition occurs at an input voltage of $V_{OFFSET\ ADC} + 0.5$ LSB.
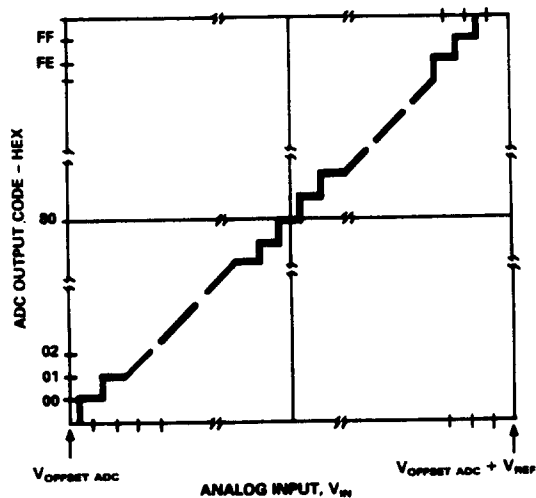

Figure 4. ADC Transfer Function with Offset Ground

Similarly, the $AGND_{DAC}$ may be offset and the transfer function for the DAC is shown in Figure 5. The output voltage may be expressed as

$$V_{OUT} = V_{OFFSET\ DAC} + V_{REF} \cdot D$$

where D is the fractional representation of the digital word. D may be set from 0 to 255/256.
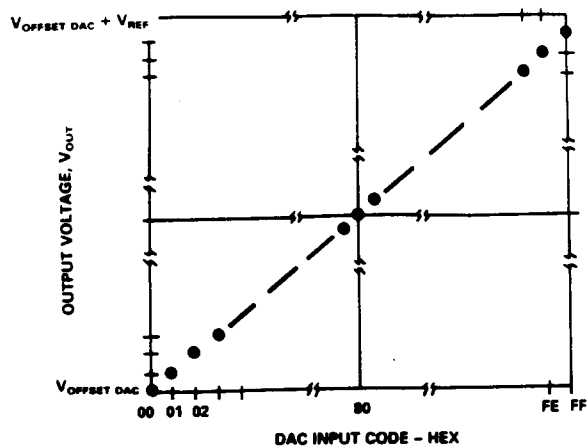

Figure 5. DAC Transfer Function with Offset Ground

For both analog grounds, a low impedance voltage source is required which can sink the currents flowing in the ground lines. With a 0.5 V bias, the $AGND_{ADC}$ current is approximately 4 mA, and the $AGND_{DAC}$ current is approximately 2 mA. In order to maintain a low dynamic impedance, the pseudo grounds should be decoupled to DGND using 0.1 μF capacitors. The capacitors will absorb the current transients which occur during conversion.
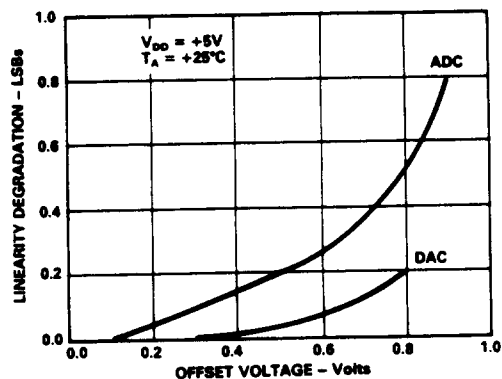

Figure 6. Accuracy vs. Offset Voltage

A plot of linearity error degradation for both the ADC and the DAC is shown in Figure 6. With a ground offset of 0.5 V, the ADC linearity error degradation is 0.2 LSBs while the DAC degrades by less than 0.1 LSB. The DNL error for both the ADC and the DAC remains well below 1 LSB thus ensuring no missed codes for the ADC and monotonic DAC operation.

Larger ground offsets than those shown in Figure 6 may be applied at the expense of accuracy. If significantly larger ground offsets are desired, then another I/O port manufactured by Analog Devices, the AD7769, should be used. This part allows user programmable offsets over a much wider range. Please consult the data sheet for further details on this part.

Information furnished in this application note is based on results taken from three fabrication lots and is believed to be accurate and reliable. However no responsibility is assumed by Analog Devices for its use.