# Channel Switching Using Σ-Δ ADCs

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## INTRODUCTION

This application note refers to the AD7708 and AD7718. Data sheets specify the update rate for Σ-Δ ADCs. The update rate is the rate at which conversions are performed when a single channel is selected and the ADC is continuously converting. The update rate that can be used depends on the application in which the ADC is being used. The peak-to-peak resolution of the device degrades as the update rate is increased. In a multichannel application such as a data acquisition system, conversions from several channels are read, i.e., each channel is selected in turn and a conversion is performed for that channel. In such an application, the rate at which conversions are performed is different compared to a single-channel system. This application note describes the switching procedure used by these parts.

## MULTICHANNEL SYSTEM

Figure 1 shows the AD7708 or AD7718 being used in a data acquisition system. Each channel is connected to a sensor. With its PGA and programmable update rate, the AD7708/AD7718 can be used to convert signals of different amplitudes and at different update rates. The AD7708 and AD7718 can be used with chopping enabled or disabled. Chopping leads to low offset and low offset drift. With chopping disabled, the offset error and offset error drift are a little higher, but a higher conversion rate can be obtained from the device.
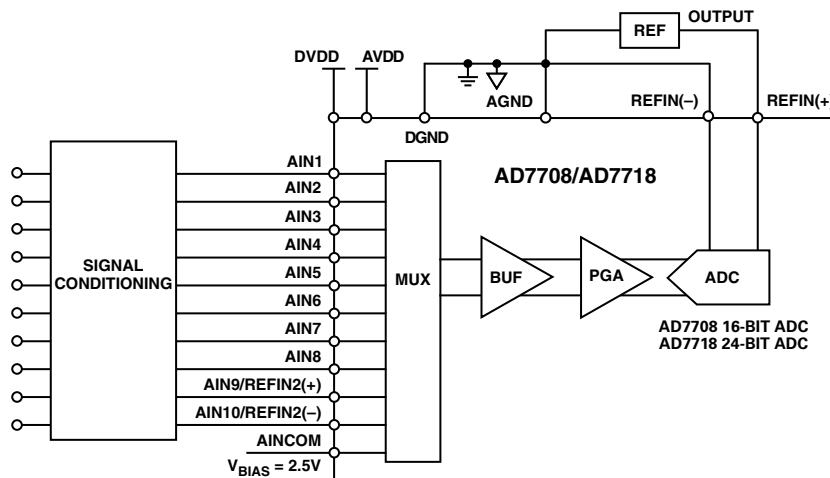


Figure 1. Data Acquisition System Using the AD7708/AD7718

# AN-665

**Chopping Disabled**

When a channel is selected, the first conversion is available after a period $(24 \times SF/f_S)$, where $f_S$ = sampling frequency = 32.768 kHz, and SF is the word loaded into the filter register on-board the device (3 – 255). The second conversion is available after a further $(8 \times SF/f_S)$ seconds. $\overline{RDY}$ will go low each time a conversion is available.

These ADCs use a Sinc filter, which has a settling time of $(24 \times SF/f_S)$ in unchopped mode. Each time a channel is selected, the filter requires this settling time to calculate the first digital word. Subsequent conversions, such as the second conversion, occur at a rate of $(f_S/(8 \times SF))$. Each time that a different channel is selected, the filter must settle as the analog input on the new channel differs from the analog input on the previous channel. After switching channels, $\overline{RDY}$ will stay high until a valid conversion is available.

**Chopping Enabled**

When chopping is used, the conversion rate is reduced for a given SF word. With chopping, the analog inputs are repeatedly switched within the ADC. Consecutive samples are then averaged by 2. This switching and averaging removes the offset error of the ADC. When switching from one channel to another, the settling time required by the Sinc filter to calculate the digital word relevant to the analog input voltage on the selected channel is $(48 \times SF/f_S)$ with chopping enabled. As in unchopped mode, $\overline{RDY}$ remains high until a valid conversion is available. Since $\overline{RDY}$ remains high until a valid conversion is available, the DSP/microcontroller does not have to count $\overline{RDY}$ pulses after switching channels to find the valid conversion. The $\overline{RDY}$ signal can be used as an interrupt to a DSP/microcontroller, the DSP/microcontroller not communicating with the ADC until $\overline{RDY}$ goes low. Subsequent conversions on this channel will occur at a rate of $(24 \times SF/f_S)$.

**ZERO LATENCY**

When using the AD7708 or AD7718, a longer time is required to calculate the first conversion when a channel is selected. Subsequent conversions on this channel occur at a higher rate. With a zero-latency ADC, available from other manufacturers, the complete filter settling time elapses between all conversions. Therefore, zero latency is achieved by reducing the conversion rate of the ADC. Analog Devices' ADCs are designed to operate at the highest speed possible for a given accuracy.

Figure 2 (i) describes the operation of the AD7708/AD7718 when switching between channels in unchopped mode. Using a single channel, conversions are obtained at the high rate (illustrated by the dashed line). When the analog input channel is switched, the ADC requires a longer interval of time to perform a conversion (three times longer in unchopped mode). Figure 2 (ii) shows the zero-latency system. In such a system, the digital filter requires the complete settling time at all times. This results in an ADC with a much slower update rate.

The AD7708 and AD7708 also have a single conversion mode in which the device performs a conversion and then goes into idle mode. In idle mode, the ADC's modulator and filter are held in a reset state. The user can begin a conversion by writing to the MD2, MD1, and MD0 bits in the mode register. When these bits are set appropriately, the modulator and filter are released from the reset state and begin conversion. Because the filter must settle, a conversion is completed after a period $(24 \times SF/f_S)$. The ADC places this valid conversion into the data register, takes $\overline{RDY}$ low, and then returns to idle mode. In this mode, the AD7708/AD7718 operates as a zero-latency ADC because the settling time is required to perform each conversion.

$\overline{RDY}$ goes low only when a valid conversion is available. Therefore, from the DSP/microcontroller's point of view, all modes of conversion use a single conversion cycle in which the extra conversion cycles required to generate a valid digital word after switching channels, or in single conversion mode, are hidden from the microprocessor. The microprocessor does not care about the length of time for which $\overline{RDY}$ is high. It knows that it will read a valid word from the ADC each time $\overline{RDY}$ goes low.
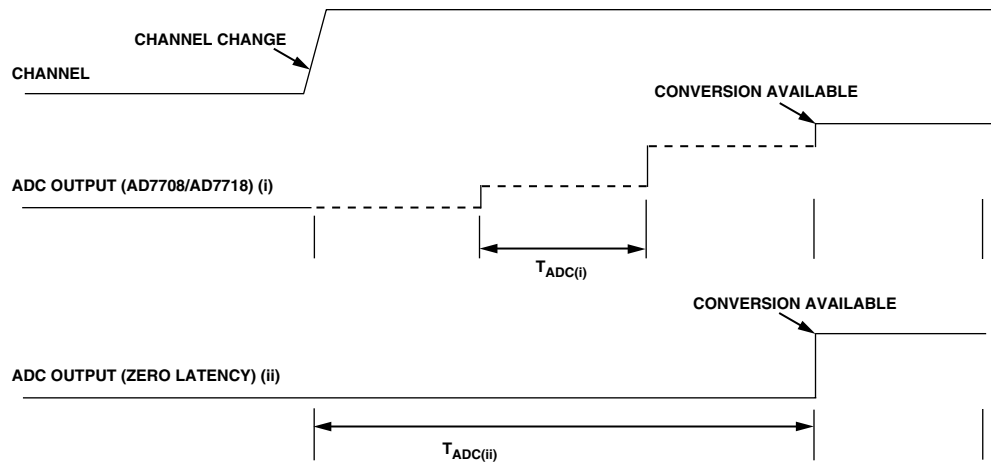
*Figure 2. ADC Conversion Time*

**SUMMARY**

The update rate for the AD7708 and AD7718 is different from the switching speed. Since the ADCs require settling time when switching between channels, the rate at which conversions are available is reduced compared to conversions on a single channel. However, the $\overline{RDY}$ output goes low only when valid conversions are available. Therefore, when switching channels, $\overline{RDY}$ remains high until a valid digital word is available. Zero latency leads to a constant conversion time, irrespective of whether or not a channel change occurs. However, this leads to a reduced update rate. Analog Devices' ADCs are designed so that the optimum update rate is obtained from the device while the $\overline{RDY}$ pin ensures that only valid conversions are available from the device.

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