AD7732/AD7734/AD7738/AD7739 in Low Power Applications
By Tom Meany

INTRODUCTION

This application note refers only to the AD7739, but is also generally applicable to the AD7732, AD7734, and AD7738. The purpose of this application note is to explain how to optimize the use of these parts in power sensitive applications.

Table I. AD7739 Power in Various Modes

$DV_{DD}/$ AV_{DD}	Clock (MHz)	Mode	Buffers	Power (mW) Typ
5/5	6	Normal	On	81.5
3/5	6	Normal	On	71.0
3/5	6	Normal	Off	45.5
3/5	4	Reduce	On	53.0
3/5	4	Reduce	Off	34.0
		Standby		0.5

The AD7739 features can make this ADC competitive with seemingly lower power ADCs from a system perspective. This application note discusses some of these features.

SYSTEM ON A CHIP

When comparing the AD7739, or other members of this family with lower power ADCs, the system on a chip features of the AD7739 must be taken into account. As shown in the block diagram, the AD7739 contains on-chip buffers, a multiplexer, crystal clock oscillator, 2-pin input/output port, high speed digital interface, and calibration logic. When compared as a system, these on-chip features may make the AD7739 competitive with lower power ADCs.

The on-chip buffers in particular are worth noting. Unbuffered high speed Σ-Δ ADCs present a particularly difficult load to any driving circuit. Typically the analog input of an unbuffered Σ-Δ ADC will look like a 4 pF to 40 pF capacitor, which is discharged and then needs to recharge to 16-bit accuracy at the modulator rate. For high speed Σ-Δ ADCs, the modulator rate can be several MHz. The on-chip buffers of the AD7739 are optimized to drive the AD7739 ADC, and all ADC specifications include the buffer performance. From a 5 V supply, the buffers consume about 25 mW. On the AD7738, the multiplexer output is made available off-chip. This means that it is possible to replace the on-chip buf-
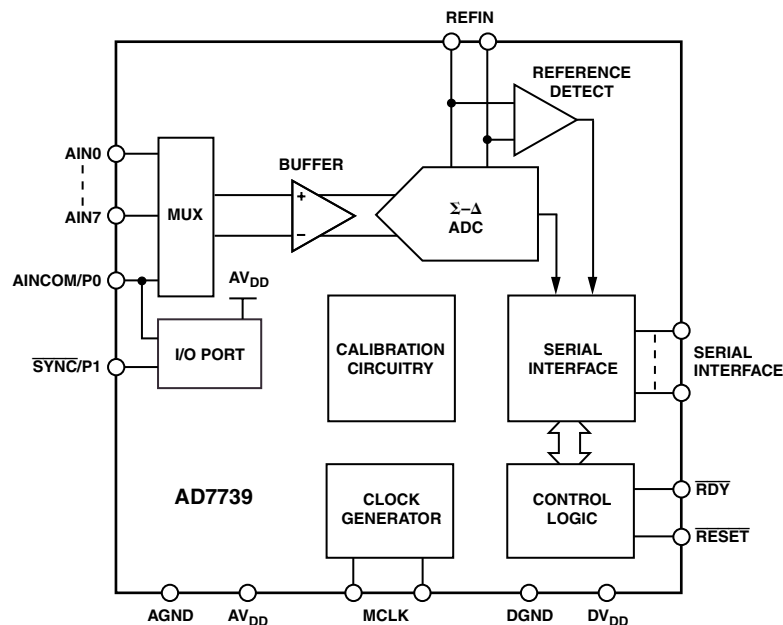

Figure 1. AD7739 Block Diagram

fers with an external buffer. However, we have not found a buffer that is more suitable than the on-chip buffer. A suitable external buffer would require 16-bit settling in 180 ns, run from 5 V supplies with 0.2 V to 4.7 V input and output capability, have noise of 1 µV rms or less, excellent offset and gain drift, INL, PSR and CMR, take up no board space and consume < 30 mW for a pair of buffers.

Both the AD7738 and AD7739 allow the on-chip analog input buffers to be powered down. This may make sense in applications with very low source impedance. In the AD7732 and AD7734, the buffers should not be shut down because they have a high input impedance due to the on-chip resistors.

However, other features such as the Schmitt triggers may reduce system power by allowing slower optocouplers to be used or the I/O port may allow the eliminination of some optocouplers.

When the system power dissipation is greater than planned and the temperature within the box begins to rise, it is worth noting that the AD7739 is fully specified to 105°C as standard.

ADC POWER-DOWN

The members of this family are optimized for channel hopping applications. Each output is fully settled, and an AD7738 can convert with 18 bits rms resolution in 65 µs. For 16-bit peak-to-peak performance, the conversion time is 125 µs. For true 16-bit noise performance and using the on-chip channel sequencer, eight conversions can be completed in 1 ms. If the system requires each channel to convert at a 100 Hz rate, then the AD7738 can sleep for 9 ms, convert for 1 ms, and run with an effective power of about 10 mW or 1 mW/channel.

To enter standby mode, write 011 to the mode bits in the mode register. For minimum power, if using a crystal clock, it is also necessary to tie CLKIN to CLKOUT with an external 10 MΩ resistor and to set the clock disable bit to stop the oscillaor
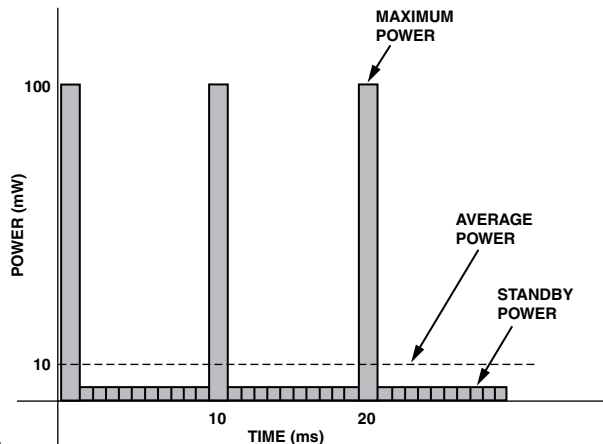

Figure 2. AD7738 Average Power Using Standby Mode

When in power-down, the AD7738 interface is still active. This means that the system controller can read the results of the conversions or configure the ADC registers with the AD7738 in low power mode.
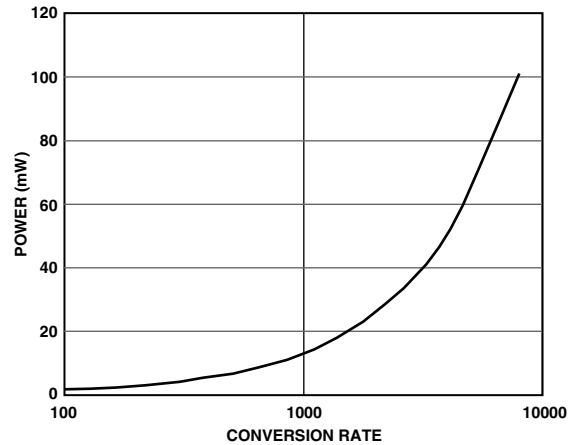

Figure 3. Power vs. Conversion Speed for 16-Bit Fully Settled Conversions Using Standby Mode

CPU POWER-DOWN

As an alernative to powering down the ADC, it may be possible to power down the system controller. This technique is most relevant when using long ADC conversion times, with a large number of channels enabled and a relatively high power system controller.

The members of the AD773x family can be set up to automatically cycle through all enabled channels and then assert their $\overline{RDY}$ pin low to tell the controller that all ADC channels have unread data. Since the AD7738 features per channel 24-bit data registers, all channels can then be read without loss of data. The AD7738 serial interface can operate with a 10 MHz bit rate to allow reading of eight 16-bit values at 2.5 µs/channel or 20 µs for all eight channels. Depending on the processing required, it may be possible to process the data from one channel while reading the data for the next, resulting in a net demand on the system controller of only 20 µs.

As an example, take a situation in which an AD7739 is configured to convert all eight channels in 20 ms. This is a conversion rate of 400 Hz per channel and an AD7739 will give over 21 bits effective resolution (rms bits) at this conversion rate. Every 20 ms the ADC will assert its $\overline{RDY}$ pin to interrupt the controller, which will then power up for 20 µs, and read and process the ADC data before returning to sleep.

REV. 0