

Devices Connected/Referenced

AD7765	24-Bit 156 kSPS, Sigma-Delta ADC
ADR444	Ultralow Noise XFET® Reference with Current Sink and Source (4.096 V)

24-Bit, 4-Channel, High Dynamic Range, 156 kSPS per Channel Simultaneous Sampling Data Acquisition System

CIRCUIT FUNCTION AND BENEFITS

The circuit shown in Figure 1 provides a high dynamic range four channel simultaneous sampling system with high crosstalk isolation, flexible sampling rates, minimal external components, and simple interface connections to a DSP or FPGA. The circuit uses four AD7765 24-bit sigma-delta ADCs in a daisy chain configuration to minimize the number of connections to the digital host. The AD7765's fully integrated differential input/output amplifier, and reference buffer significantly reduce the external component requirement.

Using the ADR444 configured in a simultaneous sampling configuration provides

- Channel-to-channel crosstalk isolation superior to that of solutions that integrate multiple 24-bit ADCs on a single chip.
- 112 dB dynamic range at 156 kSPS.
- Adaptable to greater or smaller channel counts.
- Allows multiple SYNC control (can be phase shifted with respect to each other).
- Dual decimation rates (128 and 256) and flexible sampling clock handles wide range of input bandwidths.

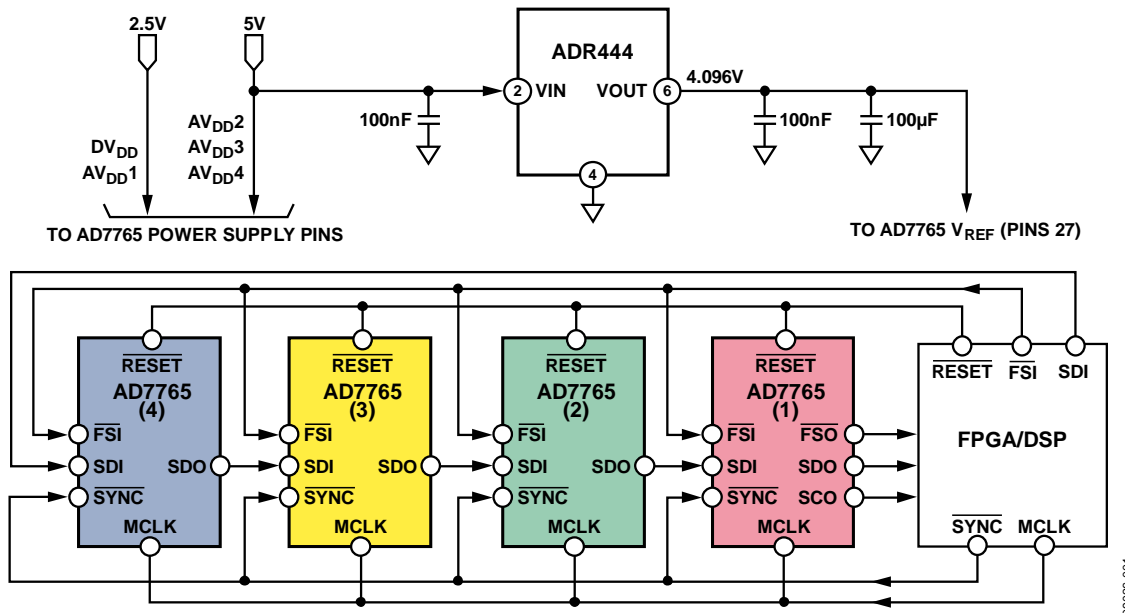


Figure 1. Four AD7765 ADCs in a Daisy-Chained Connection for Simultaneous Sampling (Simplified Schematic: All Connections and Decoupling Not Shown)

Rev. 0

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CIRCUIT DESCRIPTION

Each of the four AD7765 devices is clocked with a common sampling clock (MCLK), synchronization signal ($\overline{\text{SYNC}}$), and reset signal ($\overline{\text{RESET}}$) shown in Figure 1. A common 4.096 V reference supplied from ADR444 using the circuit shown in Figure 5 is applied using a star point configuration to each AD7765 (each ADC has an internal reference buffer).

On power up, apply a $\overline{\text{RESET}}$ pulse to all devices (minimum low time of pulse is $1 \times \text{MCLK}$ period). The $\overline{\text{RESET}}$ rising edge (which takes the ADC out of reset) is applied to each AD7765 synchronous with the MCLK falling edge. Then a $\overline{\text{SYNC}}$ pulse (minimum low time $4 \times \text{MCLK}$ periods) is applied to all AD7765 devices. The $\overline{\text{SYNC}}$ signal acts to gate the AD7765 digital filter (when it is a logic low). On the first MCLK falling edge after $\overline{\text{SYNC}}$ returns to logic high, the AD7765 digital filter starts to process samples internally.

The $\overline{\text{SYNC}}$ function accomplishes two things:

1. Provides a discrete point in time for each AD7765 to begin processing samples.
2. Ensures the data output on the SDO pin of each device is synchronous ($\overline{\text{FSO}}$ falling edge of each ADC is synchronized) as shown in Figure 2.

Once all devices are synchronized all ADCs can be configured. Operating in a daisy chain requires that all ADCs use the same decimation rate (controlled by pin 18), and power mode (controlled by writing to the control register Address 0x0001) settings. This ensures that the data from each device is output simultaneously.

To write to all four devices in the chain, a common $\overline{\text{FSI}}$ (frame sync input) signal is applied to all the AD7765 devices. A write to the AD7765 is comprised of 32 bits (16 address bits, 16 register bits). $\overline{\text{FSI}}$ frames the data to the devices. Writing to all four devices, the SDI input to the chain is loaded with a single data write instruction—i.e., when $\overline{\text{FSI}}$ goes low, 32 bits are written to SDI (serial data input) of AD7765 (4).

The example shown in this note operates in normal power mode in decimate by 128 mode (maximum output data rate of 156 kSPS).

Reading Data from the Daisy Chain

Only one $\overline{\text{FSO}}$ (frame sync output) signal is applied to the digital host as the interrupt for reading data from the chain ($\overline{\text{FSO}}$ (1)). This signal is the frame signal for all four channels. The format of the data read back by the digital host (FPGA or DSP) is shown in Figure 3. Conversion data and status bits from AD7765 (1) are clocked out first ($\overline{\text{FSO}}$ (1) is active low during this time). Data and status bits follow from AD7765 (2), (3), and (4), respectively. Note that $\overline{\text{FSO}}$ (1) will be logic high when the data results from remaining converters in the chain are being clocked out.

The next transition of $\overline{\text{FSO}}$ (1) from logic high to logic low signals that the next set of samples from all four channels are ready to be read back. The digital host is required to begin reading back on the $\overline{\text{FSO}}$ (1) falling edge, and read back 4×32 bits, i.e., 128 bits from the SDO (1) serial output. Data output on SDO (serial data output) is synchronous with the SCO (serial clock output).

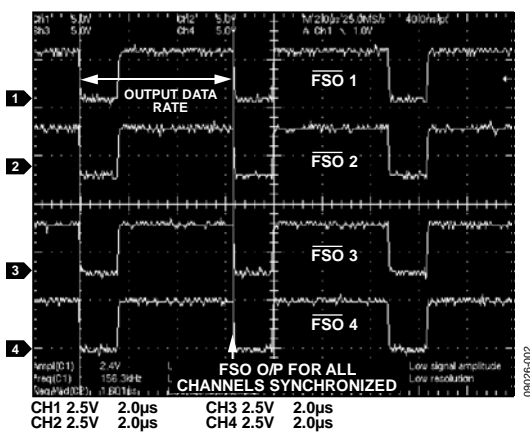


Figure 2. Scope Photo of $\overline{\text{FSO}}$ for Each of the Four AD7765 Channels, Simultaneous Sampling with an Output Data Rate of 156 kSPS

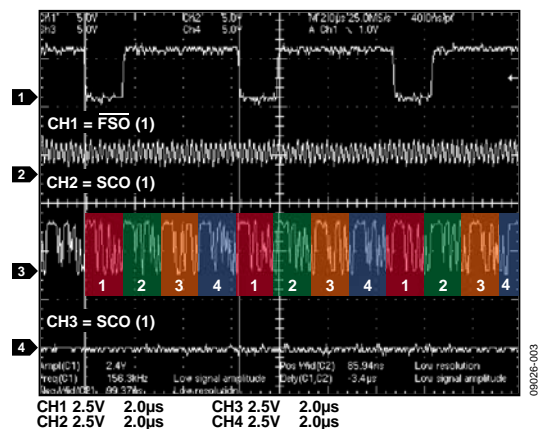


Figure 3. Daisy Chain: Reading Data. Digital Interface from AD7765 (1) to the FPGA. Data from Each Channel is Color Coded and Numbered. Output Data Rate Is 156 kSPS (Decimate by 128)

Performance

The AD7765 daisy chain circuit allows the user to simultaneously sample up to four channels at 156 kSPS. The speed of the output data rate can be changed by either reducing the MCLK frequency or changing the decimation rate of the AD7765. It is advised that the ADCs be re-synchronized following a change in the decimation rate. Figure 4 show the FFT from the output of AD7765 (3) running at the maximum sampling rate of 156 kSPS operating from an MCLK frequency of 40 MHz. A -0.5 dBFS input is applied to the AD7765 differential amplifier inputs with a 1 kHz input frequency.

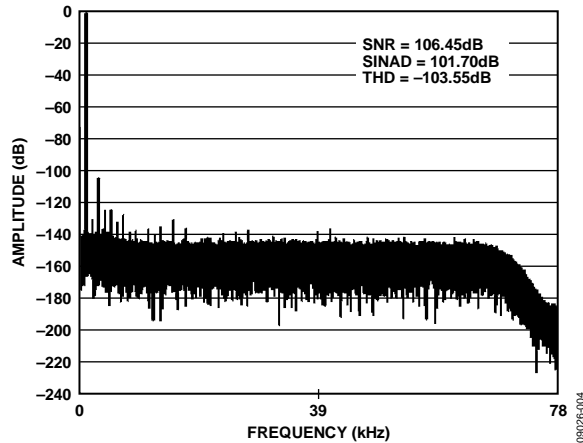


Figure 4. FFT Output for 1 kHz Input Signal with Sampling Rate of 156 kSPS, 40 MHz MCLK, 100 μF Reference Star Point Capacitor. 131,072 Samples.

Figure 5 shows the FFT output of AD7765 (3) running at a sampling rate of 97.65 kSPS operating from an MCLK frequency of 25 MHz with a 1 kHz (-0.5 dBFS) input. Table 1 shows the performance of the AD7765 at 40 MHz, 30 MHz, 25 MHz, and 20 MHz for Normal Power.

The signal source was an Audio Precision SYS2522 analog output, balanced GND, 7.699 V p-p output, 40 Ω output impedance, high accuracy mode. The analog input was applied directly to the AD7765 integrated differential amplifier. The FFT sample size was 131,072.

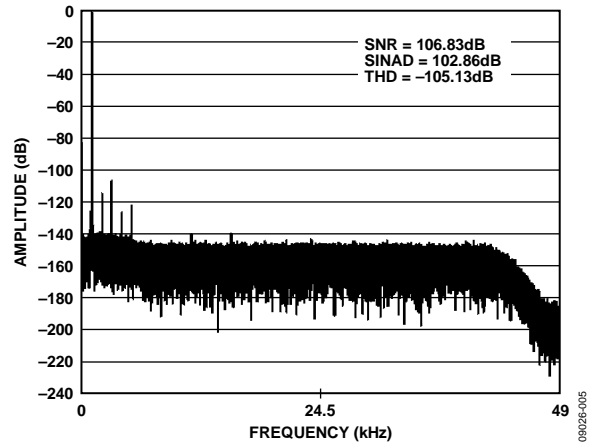


Figure 5. FFT Output for 1 kHz Input Signal with Sampling Rate of 97.65 kSPS, 25 MHz MCLK 100 μF Reference Star Point Capacitor. 131,072 Samples.

Crosstalk

One of the main performance benefits of implementing multi-channel simultaneous sampling with discrete ADCs rather than integrated components is the crosstalk performance. Table 2 shows the crosstalk on adjacent AD7765 channels when a -0.5 dB, 1 kHz input is applied to AD7765 (2).

Table 2. Crosstalk Performance

ADC Channel	AD7765 (1)	AD7765 (2)	AD7765 (3)	AD7765 (4)
Crosstalk (dB)	-125dB	N/A	-125dB	-130dB
Input Voltage	Pins 1 and 3 Shorted to GND	-0.5 dBFS 1 kHz input	Pins 1 and 3 Shorted to GND	Pins 1 and 3 Shorted to GND

Table 1. Performance versus Reference Star Point Capacitor. AD7765 Decimate by128, Normal Power Mode, -0.5 dBFS, 1 kHz Input

MCLK (MHz)	20 MHz		25 MHz		30 MHz		40 MHz	
-3 dB PASS-BAND ANALOG INPUT BW	31.25 kHz		39.0625 kHz		46.3875 kHz		62.5 kHz	
STAR POINT CAPACITOR	10μF	100μF	10μF	100μF	10μF	100μF	10μF	100μF
SNR (dBFS)	106.16	107.40	106.29	106.83	106.27	106.96	105.53	106.45
SINAD (dBFS)	102.92	103.26	102.40	102.86	102.39	102.16	101.19	101.70
THD (dB)	-105.74	-105.41	-104.75	-105.13	-104.73	-103.97	-103.26	-103.55

Reference Configuration

The ADR444 is a 4.096 V reference supply to each of the AD7765 devices in this circuit. One of the benefits of the AD7765 is that it has an on-board reference buffer, which isolates the user from the internal reference sampling circuitry. This means that no external buffer is required for the case where multiple devices share the same reference. The star point configuration shown in Figure 6 allows the reference voltage to be applied from parallel traces to each ADC from a single point. This is the best practice for minimizing any potential interactions between the ADCs. The reference voltage is serially tapped from a common reference trace to each device. The on-chip reference buffer also isolates the internal dynamic switched capacitor loads from the star point.

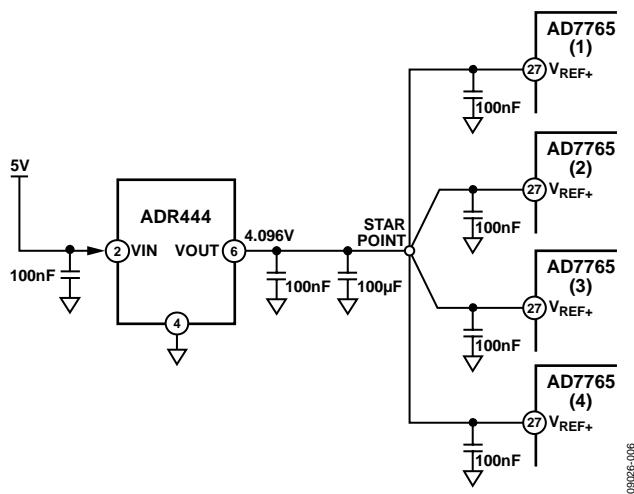


Figure 6. Reference Voltage Configuration Test Conditions

COMMON VARIATIONS

The circuit described is a scalable design in that it easily allows the user to adapt to new operating or application conditions.

If only two or three ADC channels are required, the last ADC in the chain can be eliminated, and the SDI for the chain simply routed to Device (3).

There is flexibility in setting the sampling rates of the individual devices to handle different bandwidths. For example, the user can split the chain up into two sets of two channels each by routing a separate SYNC signal to each channel, or by simply using the decimation rate pin to change the effective sampling rate. In such an implementation, there is also a pin-for-pin replacement part, the AD7764, which allows the user to sample at up to 312 kSPS with a two-channel daisy chain.

LAYOUT

Details on the layout of the PC board for AD7765 are described in the data sheet, with emphasis on the decoupling of supplies and the reference on the right hand side of the device. The Gerber files for the AD7765 evaluation board is available at www.analog.com by navigating to the Evaluation Board section on the AD7765 product page.

LEARN MORE

- [MT-031 Tutorial, Grounding Data Converters and Solving the Mystery of "AGND" and "DGND", Analog Devices.](#)
- [MT-022 Tutorial, ADC Architectures III: Sigma-Delta ADC Basics, Analog Devices.](#)
- [MT-023 Tutorial, ADC Architectures IV: Sigma-Delta ADC Advanced Concepts and Applications, Analog Devices.](#)
- [MT-074 Tutorial, Differential Drivers for Precision ADCs, Analog Devices.](#)
- [MT-075 Tutorial, Differential Drivers for High Speed ADCs Overview, Analog Devices.](#)
- [MT-101 Tutorial, Decoupling Techniques, Analog Devices.](#)

Data Sheets and Evaluation Boards

- [AD7765 Data Sheet](#)
- [AD7765 Evaluation Board](#)
- [ADR444 Data Sheet](#)

REVISION HISTORY

3/11—Revision 0: Initial Version

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