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APPLICATION NOTE

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Coherent Sampling for Power Quality Measurements Using the AD7779 24-Bit Simultaneous Sampling Sigma-Delta ADC

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INTRODUCTION

With the evolution of smart grids, utility companies are requiring additional visibility and more automation for power grids. Increased automation within the grid infrastructure increases the grid efficiency by using dynamic load adjustment to meet the demand. This increased visibility and automation requires an increase in the monitoring capabilities of the nodes on the grid. Consumers of transmission and distribution (T&D) products require cost effective products with multiple functions to meet the smart grid requirements. These functions include protection, measurement, and quality monitoring. T&D device manufacturers are developing integrated hardware/platform solutions to meet these requirements. The consolidation of functionality into a single hardware/platform solution requires an analog-to-digital converter (ADC) with the following characteristics:

- An 8-/4-channel simultaneous sampling 24-bit ADC
- A high dynamic range (114 dB at 8 kSPS)
- A fast settling ADC (low group delay)
- Fine adjustment of the ADC output data rate (ODR) to facilitate coherent sampling to within 0.01 Hz of the line frequency

The AD7779 is a 24-bit simultaneous sampling Σ-Δ ADC that meets all of these requirements. This application note presents ways to achieve coherent sampling with the line frequency using the AD7779 and compares them against alternative techniques.

COHERENT SAMPLING SPECIFICATIONS

To achieve the required accuracy on the harmonic data and metering parameters in power metering and power quality devices, ensure coherency between the ADC sampling rate and the power line frequency.

The power line frequency can vary 50 Hz ± 15% or 60 Hz ± 15%. In countries where the grid is well established and controlled, the rate of change of the power line frequency is low. In countries where the grid is under development, the power line frequency varies significantly. Power quality standard IEC 61000-4-30 specifies a frequency tracking resolution vs. power quality product classification. Class A devices must track 0.01 Hz changes in the line frequency, Class S devices must track 0.05 Hz changes in the line frequency, and the manufacturer determines the tracking specification for Class B devices. Class B devices may be removed from future editions of the IEC 61000-4-30 standard.

The method for measuring voltage harmonics used by the IEC 61000-4-30 standard is defined in the IEC 61000-4-7: a discrete Fourier transform (DFT) is performed digitally over a group of samples using a rectangular window. The DFT windowing techniques are not recommended because the DFT window profile (Hamming, Blackman, or so on) changes the magnitude of the harmonics; if each manufacturer uses a different fast Fourier transform (FFT) windowing technique, the harmonic analysis results differ from one product supplier to another. Therefore, the IEC 61000-4-30 Class A power quality devices cannot use the DFT windowing techniques to achieve coherent sampling.

EXISTING SOLUTIONS TO ACHIEVING COHERENT SAMPLING

Customers currently use one of the following options to maintain coherency with the line frequency:

- Use a phase-locked loop (PLL) to adjust the ADC clock dynamically.
- Sample the ADC and perform the DFT using a Goertzel algorithm.
- Oversample the ADC by at least 4 times, interpolate the waveform samples, and perform the DFT using a regular fast Fourier transform (FFT) algorithm.

The PLL is implemented in either analog or digital domains. It provides an output signal with a frequency equal to the fundamental frequency of the input signal. The signal dynamically adjusts the ADC clock and achieves the coherency of the ADC sampling with the fundamental frequency of the line. The problem with the PLL is its response time; that is, the time from the moment the line frequency changes to the moment the PLL output settles.

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REVISION HISTORY

2/16—Initial Version: Revision 0

Figure 1 shows a block diagram of a protective relay and measurement system composed of the AD7779 and a digital signal processor (DSP) that calculates the voltage harmonics and then uses them in the protection algorithms. The Goertzel DFT algorithm practically adjusts the Fourier transform coefficients' function of the number of waveform samples acquired during an integer number of line cycles. These coefficients are sine and cosine; therefore, the DSP must have increased bandwidth to accommodate this load.

As an alternative to the Goertzel algorithm, use the interpolation approach. Set the AD7779 to an output rate of 32 kSPS, 4 times larger than the 8 kSPS normally used. The DSP interpolates the waveform samples to maintain the same number of samples over the line cycle independent of the line frequency. The interpolation can be linear or of a higher degree, with the latter yielding more accurate results. The DSP must have increased bandwidth to accommodate this additional computational load. Note that the interpolation introduces spurious harmonics into the measurement band.

Each existing solution has disadvantages such as increased power consumption (due to the increased DSP calculation bandwidth requirement) and additional cost. The sample rate converter (SRC) of the AD7779 allows users to achieve a Class A power quality device by having sufficient resolution in the AD7779 ODR to track 0.01 Hz changes in the power line frequency. The SRC eliminates the need for the interpolation block shown in Figure 1.

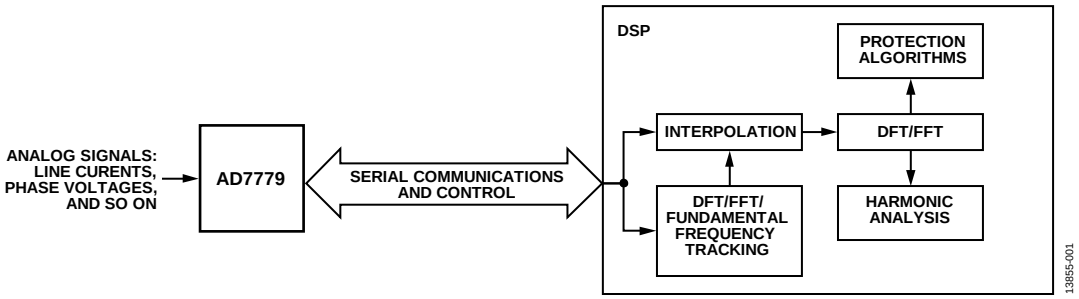

Figure 1. Block Diagram of a Protective Relay and Measurement System

SAMPLE RATE

SAMPLE RATE CONVERTER (SRC)

The Σ-Δ ADCs include a low-pass sinc filter to remove the noise from the modulator efficiently. The sinc filter also reduces the output data rate by some integer value relative to the modulator clock rate, a process called decimation. Usually the decimation is restricted to a set number of integer values. The sinc filter on the AD7779 is implemented with a synchronous sample rate converter (SRC) to allow decimation by a non-integer value. The user can vary this value over time while still using the efficient and proven sinc filter architecture.

For the SRC to be available, the AD7779 must be in the SPI control mode. During the power-up procedure, select this mode by tying the FORMAT0 pin and the FORMAT1 pin directly to IOVDD, the input/output digital LDO supply.

The AD7779 is intended specifically for applications that monitor ac voltages and currents in mains electrical power line networks. Two of the main characteristics measured in these applications are the transmission line frequency and the power. Determine these by performing an FFT on the outputs generated by an ADC.

The AD7779 can maintain coherent sampling over the line frequency by allowing a user to program specific output data rates. The user programs a decimation factor (N) for the sinc filter with the SPI interface. The formula for the output data rate (ODR) is

$$ODR = \frac{MCLK}{M \times N} = \frac{f_{MOD}}{N} \quad (1)$$

where:
MCLK is the AD7779 clock frequency.
M is equal to 4 when the AD7779 device is set to high resolution (HR) mode, and 8 when the AD7779 device is set to low power (LP) mode.
$f_{MOD} = MCLK/M$, which is the sampling clock of the modulator.

The procedure for calculating the decimation factor, N, follows:

1. Connect the FORMAT0 pin and the FORMAT1 pin to IOVDD to put the AD7779 in the SPI control mode.
2. Select the sinc filter, the decimation rate, the power mode, the PGA gain, and the internal/external voltage reference by writing to the relevant memory map registers using the SPI interface. Note that the AD7779 has a sinc3 filter only.
3. Select the output data rate (ODR) of the ADCs in between the minimum and maximum rates detailed in Table 1.
4. Calculate the sampling clock of the modulator by f_{MOD} = MCLK/M.
5. Calculate the decimation factor by N = f_{MOD}/ODR.

Table 1. Minimum and Maximum Output Data Rates (ODRs)

Mode	Minimum ODR (kHz)	Maximum ODR (kHz)
HR	0.500000001	16
LP	0.125000001	8

For example, for the AD7779, elect to use the sinc3 filter with the device set to LP mode.

Sample the voltage 64 times over one line period to use the ADC output samples into a 64-point DFT. If the line frequency is exactly 50.00 Hz, the output data rate is then ODR = 50.00 × 64 = 3.200 kHz. The sampling clock of the modulator is

$$f_{MOD} = \frac{MCLK}{M} = \frac{4096}{8} = 512 \text{ kHz}.$$

The decimation factor N is then

$$N = \frac{f_{MOD}}{ODR} = \frac{512}{3.2} = 160.$$

If the line frequency becomes 50.01 Hz, still sample it 64 times. The output data rate is then ODR = 50.01 × 64 = 3.20064 kHz.

The decimation factor N is then

$$N = \frac{f_{MOD}}{ODR} = \frac{512}{3.20064} = 159.968006.$$

Use the AD7770/AD7771/AD7779 Filter Model to calculate the decimation factor and the sinc filter response in any condition.

PROGRAMMING THE DECIMATION FACTOR N INTO THE SAMPLE RATE CONVERTER

Program the decimation factor N to the memory map before loading it into the SRC. The decimation factor is composed of an integer and a fractional number. There are four memory map registers used to program the decimation factor.

Two registers are used to program the integer, allowing a range of programmable values from the minimum specified value (see Table 2) to 4095.

- Register 0x60, the SRC_N_MSB bits, Bits[3:0]
- Register 0x61, the SRC_N_LSB bits, Bits[7:0]

Two registers are used to program the fractional number, also called the interpolation factor, allowing a 16-bit decimal representation of the fractional number to be programmed.

- Register 0x62, the SRC_IF_MSB bits, Bits[7:0]
- Register 0x63, the SRC_IF_LSB bits, Bits[7:0]

Table 2 details the maximum and minimum values for the decimation factor N based on the filter type.

Table 2. Maximum and Minimum Decimation Factor N Values

Filter Type	Minimum N	Maximum N
Sinc3 (HR Mode)	128	4095
Sinc3 (LP Mode)	64	4095

In the example from the Sample Rate Converter (SRC) section, N = 159.968006. The integer is 159 and the fractional number is 0.968006. SRC_N_MSB = 0x00 and SRC_N_LSB = 0x9F.

To calculate the value of the SRC_IF_MSB and SRC_IF_LSB registers,

1. Multiply the fractional number by 2^{16}: $0.968006 \times 2^{16} = 63{,}439.24$.
2. Take the integer and convert it to hexadecimal format: 63,439 = 0xF7CF.
3. Write 0xF7 into the SRC_IF_MSB register and 0xCF into the SRC_IF_LSB register.

The AD7770/AD7771/AD7779 Filter Model calculates the register values for every calculated decimation factor N for the SRC_N_MSB, SRC_N_LSB, SRC_IF_MSB, and SRC_IF_LSB registers.

LOADING THE DECIMATION FACTOR N INTO THE SAMPLE RATE CONVERTER

The SRC_N_MSB, SRC_N_LSB, SRC_IF_MSB, and SRC_IF_LSB registers only store the decimation factor. They must be loaded to the DSP via an SRC load operation. The decimation factor can be loaded by software or by hardware, depending on Bit 7 (SRC_LOAD_SOURCE) in the SRC_UPDATE register (Register 0x64):

- Bit 0 = SRC_LOAD_UPDATE
- Bit 7 = SRC_LOAD_SOURCE

If Bit 7, SRC_LOAD_SOURCE, has a default value of 0, perform the load by setting SRC_LOAD_UPDATE bit to 1. Wait at least two MCLK periods and then clear the SRC_LOAD_UPDATE bit to 0. The bit must be cleared to 0 before any attempt to execute a new load.

If Bit 7, SRC_LOAD_SOURCE, is set to 1, the ODR is controlled in hardware. To execute the load,

1. Connect the MODE0/GPIO0 pin to the MODE1/GPIO1 pin.
2. Set the MODE2/GPIO2 pin high for two MCLK periods in LP mode and for one MCLK period in HR mode. Then set the MODE2/GPIO2 pin low.

If multiple AD7779 devices must be loaded with the same synchronized SRC load signal, connect the MODE1/GPIO1 pin of one device to the MODE0/GPIO0 pins of the other devices. Note this synchronization method requires the use of a common MCLK (see Figure 2).

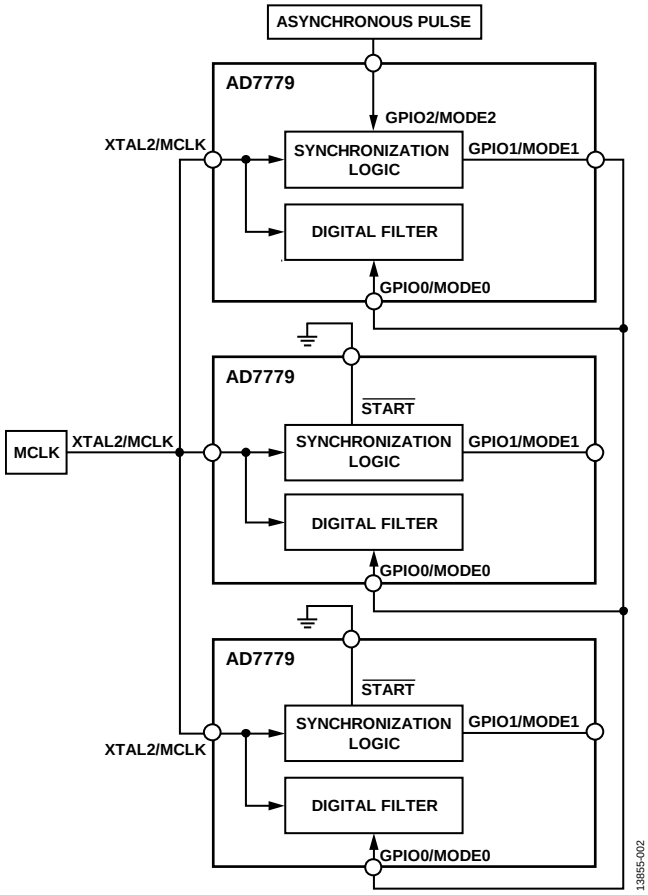

Figure 2. Synchronization of Multiple AD7779 Devices

LATENCY IN TRANSITIONING TO THE NEW ODR

After the SRC has been loaded with the new decimation factor, there is a latency in transitioning to the new ODR. The latency arises because the SRC enters a transition sequence: it finishes calculating the filter outputs at the previous ODR and then starts calculating outputs at the new ODR. The ODR is determined by monitoring the period of the signal at the $\overline{\text{DRDY}}$ pin (Pin 30). The $\overline{\text{DRDY}}$ pin stays high for at least one DCLK pulse to indicate the latest conversion has completed and the data is about to be provided at the DOUT pin.

There is a latency from when the decimation factor is loaded to when the new ODR is seen at the $\overline{\text{DRDY}}$ pin. The new ODR is seen after three or four $\overline{\text{DRDY}}$ pulses (see Figure 3). The exact latency is not fixed because it depends on when the SRC is loaded relative to the $\overline{\text{DRDY}}$ pulses.

During the transition sequence, do not load a new decimation factor into the SRC. Any attempt is ignored.

FREQUENCY

The $\overline{\text{DRDY}}$ pin can be used to measure the ODR of the AD7779. When the decimation factor is an integer, the period of the $\overline{\text{DRDY}}$ pin is always constant and equal to 1/ODR

If, for example, N = 160, ODR = f_{MOD}/N = 512/160 = 3.2 kHz and the period between $\overline{\text{DRDY}}$ pulses is 1/3200 = 312.5 µs. If N = 159, ODR = 512/159 = 3.220126 kHz and the period between $\overline{\text{DRDY}}$ pulses is 1/3220.126 = 310.547 µs.

If the decimation factor N is a non-integer number, the period of the $\overline{\text{DRDY}}$ oscillates between the periods determined by the integers obtained rounding up or down the decimation factor. The average of the periods is equal to the expected ODR. The periods, however, are always calculated at the ODR programmed to the AD7779.

For example, if N = 159.968006, the $\overline{\text{DRDY}}$ period oscillates between the period determined by N = 159 (310.547 µs) and N = 160 (312.5 µs) in such a way to average N/f_{MOD} = 159.968006/512000 = 312.438 µs.

To verify that the ODR period is the expected one, measure the time between the number of $\overline{\text{DRDY}}$ pulses indicated by the following expressions. They provide a good approximation of the time it takes to obtain the expected ODR.

When IF is ≤0.5,

((1/*IF*) + 1) pulses

When IF is >0.5,

((1/(1 − *IF*)) + 1) pulses

where *IF* is the fractional number of N.

Round up the result to the nearest integer whenever the number of $\overline{\text{DRDY}}$ pulses is not an exact integer.

For example, if N = 159.968006, IF = 0.968006. The number of $\overline{\text{DRDY}}$ pulses that must be counted to calculate the expected ODR period is the following:

1/(1 − 0.968006) + 1 = 32.35 ≅ 33 $\overline{\text{DRDY}}$ pulses

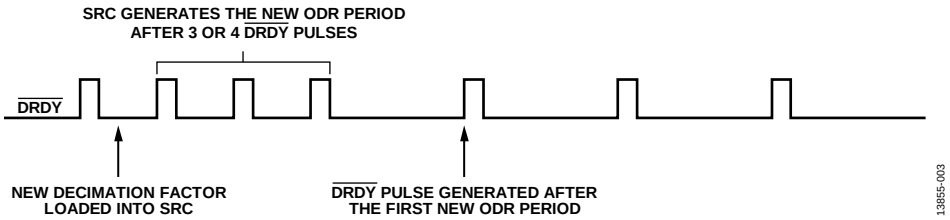

Figure 3. New Output Data Rate Latency

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