AN-1405
APPLICATION NOTE

One Technology Way • P.O. Box 9106 • Norwood, MA 02062-9106, U.S.A. • Tel: 781.329.4700 • Fax: 781.461.3113 • www.analog.com

Diagnostic Features on the AD7770, AD7771, and AD7779

by Lluis Beltran Gil and Miguel Usach

INTRODUCTION

The AD7770/AD7771/AD7779 are 8-channel, simultaneous sampling, Σ-Δ analog-to-digital converters (ADCs). Each channel is comprised of a dedicated programmable gain amplifier (PGA) stage (offering gains of 1, 2, 4, and 8), a full Σ-Δ ADC, and a low latency sinc3 digital filter.

Within the different blocks of the AD7770/AD7771/AD7779, numerous diagnostics and monitoring functions are implemented in both the analog and digital domain, such as the reference block, the modulator or the serial interface, among others (see Figure 1).

The AD7770/AD7771/AD7779 also include a 12-bit successive approximation register (SAR) ADC that can be powered independently. The SAR ADC can be used for diagnostic and monitoring purposes without having to decommission one of the Σ-Δ ADC channels dedicated to system measurement functions with the use of an external multiplexer and signal conditioning. Internal nodes and external supplies can also be monitored by selecting them through the internal diagnostics multiplexer connected to the SAR ADC.

The AD7770/AD7771/AD7779 can be configured using either the serial peripheral interface (SPI) control mode or the pin control mode. In pin control mode, the device is configured in a predefined state at power-up based on the voltage levels applied to the MODE0 to MODE3 pins and the FORMAT0 and FORMAT1 pins. For more information, see the AD7770/AD7771/AD7779 data sheets.

It is not possible to access many of the diagnostic and monitoring features implemented on the device in pin control mode. SPI control mode, unlike pin control mode, allows access to the full set of diagnostic and monitoring functions implemented. Therefore, it is recommended to use the device in SPI control mode for diagnostic and monitoring purposes.

This application note gives an overview of these features, the errors that are detected by the AD7770/AD7771/AD7779, and the different options available to diagnose and overcome these errors.

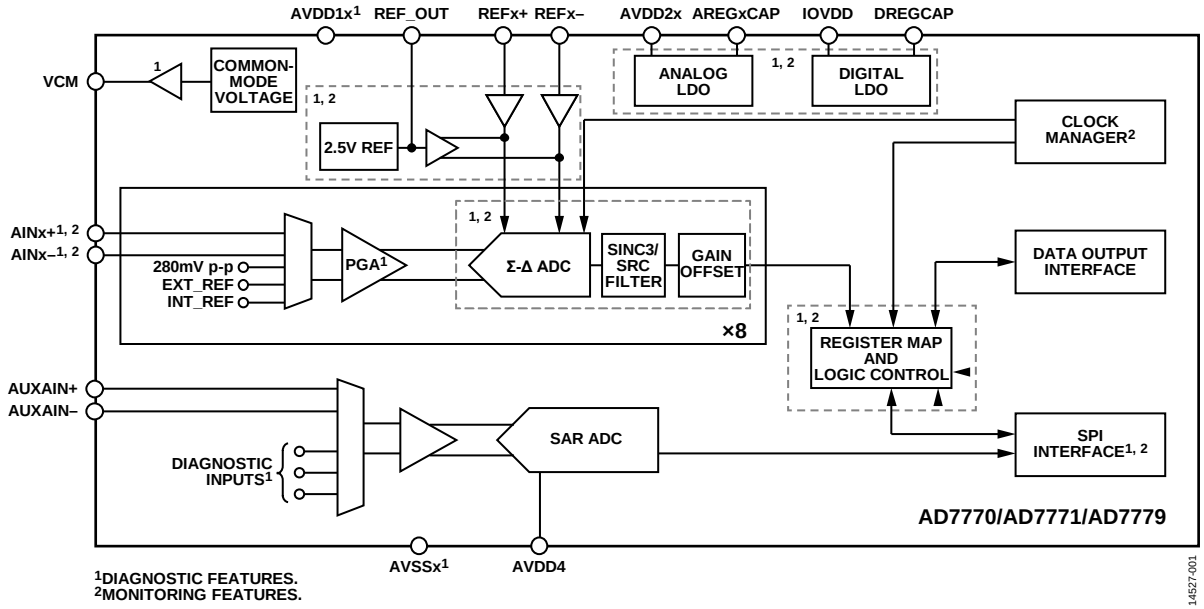

Figure 1. AD7770/AD7771/AD7779 Block Diagram (Only One out of Eight Channel Signal Chains is Shown)

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6/2017—Rev. 0 to Rev. A

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4/2017—Revision 0: Initial Version

DIAGNOSTIC AND MONITORING FEATURES

The AD7770/AD7771/AD7779 provide a comprehensive list of error checkers along the signal chain, reference, common-mode, digital, and supply blocks, to guarantee the correct functionality of the device. When an error checker triggers,

- The ALERT pin sets.
- The alert bit on the Σ-Δ ADC header is set.
- The CHIP_ERROR bit within the status registers is set (see Table 2).
- The corresponding flag within the memory map is set.

The ALERT pin, Pin 18 when using pin control mode or Pin 16 when using SPI control mode, is typically high only while the error is present and is reset when the error disappears, except for the SPI errors, where the ALERT pin is not reset until the following SPI transaction.

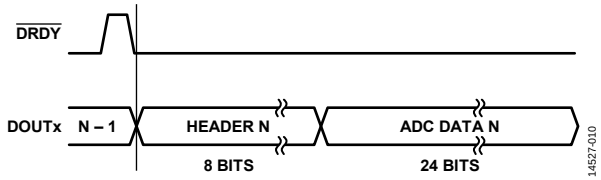

Figure 2. ADC Output 8-Bit Header Plus 24-Bit Conversion Data

The Σ-Δ data header precedes every data frame and contains an alert bit. The alert bit is the most significant bit (MSB), which offers similar functionality to that of the ALERT pin, and alerts the user when an error is present. Additionally, the Σ-Δ cyclic redundancy check (CRC) header, shown in Figure 3, which is active by default, can be switched to an error header (in SPI control mode, only) through the DOUT_HEADER_FORMAT bit, Register 0x014, Bit 5. If the error header is selected, the four least significant bits (LSBs) in the header provide additional information for major errors, for example, when a reset is detected, a modulator or digital filter is saturated, or an analog input is over or under its range, shown in Figure 3.

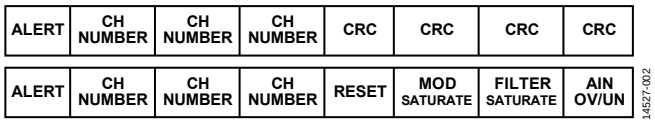

Figure 3. CRC and Error Headers

When an error triggers in any of the monitored blocks, the corresponding flag within the memory map sets; consequently, in pin control mode, the error source cannot be checked, because it is not possible to access the memory map, as opposed to SPI control mode.

These error bits within the memory map are sticky, meaning they reset only when the error register is read back and the source of error disappears.

To simplify the search of the error source, the memory map includes three registers: STATUS_REG_1, STATUS_REG_2, and STATUS_REG_3. These registers point to the specific register that contains the source of error shown in Table 2.

For instance, if the ERR_LOC_CH4 bit, located on STATUS_REG_1 (see Table 2), is set, the bit indicates that a flag has triggered in the CH4_ERR_REG register, Register 0x050, according to Table 1.

Bit 5 of all three status registers (the CHIP_ERROR bit) indicates if any error bit is set. This bit clears when the error is no longer present and when the register is read back. However, Bits[4:0] are not cleared until the register they are pointing to is read and reset.

Table 1. Register Error Source

Bit Name	Register Source
ERR_LOC_GEN2	GEN_ERR_REG_2
ERR_LOC_GEN1	GEN_ERR_REG_1
ERR_LOC_CH7	CH7_ERR_REG
ERR_LOC_CH6	CH6_ERR_REG
ERR_LOC_CH5	CH5_ERR_REG
ERR_LOC_CH4	CH4_ERR_REG
ERR_LOC_CH3	CH3_ERR_REG
ERR_LOC_CH2	CH2_ERR_REG
ERR_LOC_CH1	CH1_ERR_REG
ERR_LOC_CH0	CH0_ERR_REG
ERR_LOC_SAT_CH6_7	CH6_7_SAT_ERR
ERR_LOC_SAT_CH4_5	CH4_5_SAT_ERR
ERR_LOC_SAT_CH2_3	CH2_3_SAT_ERR
ERR_LOC_SAT_CH0_1	CH0_1_SAT_ERR

Table 2. AD7770/AD7771/AD7779 Status Registers

Reg.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x05D	STATUS_REG_1	Reserved		CHIP_ERROR	ERR_LOC_CH4	ERR_LOC_CH3	ERR_LOC_CH2	ERR_LOC_CH1	ERR_LOC_CH0
0x05E	STATUS_REG_2	Reserved		CHIP_ERROR	ERR_LOC_GEN2	ERR_LOC_GEN1	ERR_LOC_CH7	ERR_LOC_CH6	ERR_LOC_CH5
0x05F	STATUS_REG_3	Reserved		CHIP_ERROR	INIT_COMPLETE	ERR_LOC_SAT_CH6_7	ERR_LOC_SAT_CH4_5	ERR_LOC_SAT_CH2_3	ERR_LOC_SAT_CH0_1

MAIN SIGNAL CHAIN

Along the signal chain, the AD7770/AD7771/AD7779 include error checkers that monitor the output, the filter output, the modulator, and the analog input pins. The PGA gain can also be diagnosed.

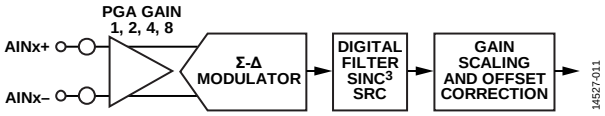

Figure 4. Signal Chain per Channel

OUTPUT SATURATION

Each channel has associated offset and gain adjustment registers within the memory map (from Register 0x01C to Register 0x04B) to calibrate the devices as explained in the AD7770/AD7771/AD7779 data sheets. An error in setting the gain and offset configuration can cause the output to clip at either positive or negative full scale. For instance, if the gain and offset registers in Channel 6 are not programmed properly, the CH6_ERR_OUTPUT_SAT bit on the corresponding CH6_7_SAT_ERR register asserts, shown in Table 3.

When the error triggers, it can be double checked by reading the last data converted to verify if the output actually has clipped at positive or negative full scale (+FS or −FS). When verified, a potential cause for the clipping is if the offset or gain register has not been programmed properly, especially if either the filter or modulator saturation checker are not triggered before. However, if those calibration registers are not overwritten, this error checker can also indicate the filter is close to saturation, causing the default gain scaling to bring the output beyond +FS or −FS.

Another potential cause to trigger this error checker is if the analog inputs are beyond +FS or −FS, which can be diagnosed by using the SAR ADC, explained in the SAR ADC section, or if the PGA does not scale the analog input properly, which can be diagnosed as explained in the PGA Gain section.

FILTER SATURATION

The filter saturation triggers if the filter output is out of bounds, which represents an output code approximately 20% higher than positive or negative full scale.

When any of the eight on-chip digital filters generate a saturation error, the corresponding CHx_ERR_FILTER_SAT bit, located on the corresponding CHx_SAT_ERR register (Register 0x054 to Register 0x057), is asserted. For instance, when the Channel 6 filter saturates, Bit 1 on the CH6_7_SAT_ERR register asserts, shown in Table 3.

Filter saturation can be verified by reading the Σ-Δ conversion. When verified, it is recommended to change the Σ-Δ reference to the AVDD pin through the ADC_MUX_CONFIG register (Register 0x015, Bits[7:6]), allowing a wider input range to check if the input voltage was higher than expected, indicating an error in the ADC front end.

If the filter output is out of bounds, it consequently causes the output saturation to trigger. Therefore, checking if the output saturation has triggered indicates if the modulator saturation checker works properly.

MODULATOR SATURATION

If any of the 8 Σ-Δ modulators outputs 20 consecutive 1s or 0s, the saturation detector asserts the corresponding CHx_ERR_MOD_SAT bit of the corresponding CHx_SAT_ERR register. For instance, Bit 2 in the CH6_7_SAT_ERR register sets if Channel 6 outputs 20 consecutive 1s or 0s, shown in Table 3. This bit clears only when reading the corresponding register of the CHx_ERR_MOD_SAT bit if the error corrected itself, for example, when the modulator outputs different values than all 0s or all 1s again.

When the modulator saturates, it indicates that it is out of bounds, and a pulse in the $\overline{\text{RESET}}$ pin is required to reset the modulator.

If the modulator is out of bounds, it causes the filter saturation to trigger. Therefore, checking if the filter saturation is triggered indicates if the modulator saturation checker works properly.

All three saturation detectors, namely the modulator, filter, and output saturation detectors, are enabled by default and can be disabled through the CHX_ERR_REG_EN register, Register 0x058[7:5], shown in Table 3.

Table 3. CH6_7_SAT_ERR and CHx_ERR_REG_EN

Reg.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x057	CH6_7_SAT_ERR	Reserved		CH7_ERR_MOD_SAT	CH7_ERR_FILTER_SAT	CH7_ERR_OUTPUT_SAT	CH6_ERR_MOD_SAT	CH6_ERR_FILTER_SAT	CH6_ERR_OUTPUT_SAT
0x058	CHX_ERR_REG_EN	OUTPUT_SAT_TEST_EN	FILTER_SAT_TEST_EN	MOD_SAT_TEST_EN	AINM_UV_TEST_EN	AINM_OV_TEST_EN	AINP_UV_TEST_EN	AINP_OV_TEST_EN	REF_DET_TEST_EN

PGA GAIN

The user can diagnose whether the PGA gain is correct. The internal diagnostics multiplexer connected to the input of the Σ-Δ converter has the option to connect a 280 mV signal through the ADC_MUX_CONFIG (Register 0x015[5:2]). Consequently, each gain stage (1, 2, 4, and 8) can be verified individually by checking if the Σ-Δ data converted corresponds to the 280 mV signal, gained by the stage programmed through the configuration register of the channel, Register 0x000 to Register 0x007, Bits[7:6].

OVERVOLTAGE/UNDERVOLTAGE EVENTS

Every analog input on the AD7770/AD7771/AD7779 includes a comparator circuit, which triggers the CHx_ERR_AINx_OV bit on the corresponding CHx_ERR_REG register (Register 0x04C to Register 0x053) in the event that the absolute input voltage has exceeded the AVDD1x voltage level in either the AINx+ or AINx− pins, as the AINx+ or AINx− pins can be separately checked. This bit clears when the input voltage returns to a level lower than AVDD1x and the register is read back. Operating the ADC outside the data sheet limits degrades its linearity. For instance, if the Channel 6 positive analog input (AIN6+) goes beyond the AVDD1B voltage, the CH6_ERR_AINP_OV bit (Register 0x052, Bit 1) asserts.

In the same way, by means of a second comparator, if the input voltage is lower than AVSSx, the corresponding CHx_ERR_AINx_UV bit asserts and does not clear until the voltage level raises higher than AVSSx and the register is read back. Figure 5 shows both comparators implemented in every analog input (in both AINx+ and AINx−) that monitor and trigger overvoltage or undervoltage events. If the error is present for a long period of time, it can degrade the device and affect its reliability. Due to the comparator threshold tolerance, the trigger level is in the ±30 mV range around the supply rails, that is, at AVDDx ±30 mV for the overvoltage events and AVSSx ±30 mV for the undervoltage events.

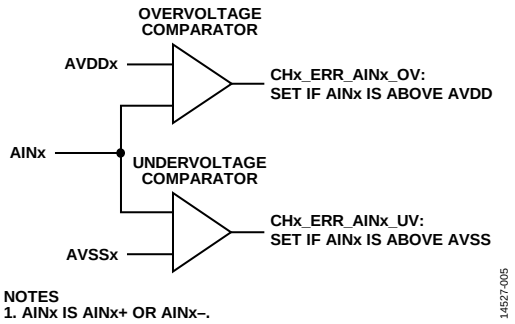

Figure 5. Overvoltage and Undervoltage Comparator in Every Analog Input

When these errors trigger, they can be diagnosed using the SAR converter, connecting the analog input that triggered to the AUXAIN+/AUXAIN− pair of inputs. For more information, refer to the SAR ADC section.

REFERENCE BLOCK

REFERENCE DETECTION

The AD7770/AD7771/AD7779 voltage reference level is monitored by an on-chip comparator, shown in Figure 6. This comparator triggers when the voltage reference on any of the Σ-Δ channels drops below 0.7 V for a few microseconds, setting the corresponding CHx_ERR_REF_DET bit of the channels affected, located on Bit 0 of the error register of the channel (CHx_ERR_REG, Register 0x04C to Register 0x053). This error flag indicates that the reference voltage applied is no longer a valid reference for conversions. When this happens, the error can indicate a failure on the internal reference buffers or a failure in the reference.

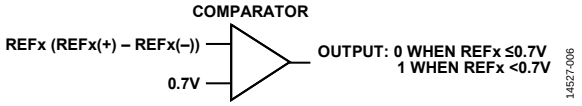

Figure 6. Reference Detect Circuitry

If the reference detection triggers, the reference is diagnosed by using the SAR ADC to select the REF+ or REF− signal on the input multiplexer of the SAR, as explained in the SAR ADC section. Alternatively, the reference can be selected on the ADC input multiplexer to measure the reference voltage through any of the Σ-Δ ADC (refer to the Sigma-Delta ADC Multiplexer section). To do so, the reference selected must be AVDD1A/AVSS1A, so the input range is wider and can accommodate the 2.5 V reference without saturating the modulator (see Table 5).

When the reference is verified, select a different operation mode on the reference buffer (the BUFFER_CONFIG_1 and BUFFER_CONFIG_2 registers, Register 0x019 and Register 0x01A) and/or select a different voltage reference (ADC_MUX_CONFIG register, Register 0x015, Bits[7:6]) from any of the three sources available as summarized in Table 4 and Table 5, respectively.

The reference detect error checker is disabled by default, but it can be enabled through the REF_DET_TEST_EN bit on the CHX_ERR_REG_EN register, Register 0x058, Bit 0.

COMMON MODE

The common-mode output (typical at (AVDD1 + AVSSx) ÷ 2), like the PGA, has no built in monitoring features and therefore no error checker triggers if the output does not work properly. However, its operation can be diagnosed by connecting the SAR input multiplexer to the VCM pin voltage. Refer to the SAR ADC section for more information.

Table 4. Reference Buffer Operation Modes, BUFFER_CONFIG_1 (Register 0x019) and BUFFER_CONFIG_2 (Register 0x01A)

Reference Buffer Operation Mode	REFx+	REFx−
Enabled	BUFFER_CONFIG_1, Bit 4 = 1; BUFFER_CONFIG_2, Bit 7 = 0	BUFFER_CONFIG_1, Bit 3 = 1; BUFFER_CONFIG_2, Bit 6 = 0
Precharged	BUFFER_CONFIG_1, Bit 4 = 1; BUFFER_CONFIG_2, Bit 7 = 1	BUFFER_CONFIG_1, Bit 3 = 1; BUFFER_CONFIG_2, Bit 6 = 1
Disabled	BUFFER_CONFIG_1, Bit 4 = 0	BUFFER_CONFIG_1, Bit 3 = 0

Table 5. Σ-Δ References

ADC_MUX_CONFIG, Bits[7:6]	Channel 0 to Channel 3	Channel 4 to Channel 7
00	REF1+/REF1−	REF2+/REF2−
01	Internal reference	Internal reference
10	AVDD1A/AVSS1A	AVDD1B/AVSS1B
11	REF1−/REF1+	REF2−/REF2+

DIGITAL CORE

ROM AND MEMMAP CRC

During power-up, a fuse verification takes place. To avoid an error in the fuses caused by regrowth, the AD7770/AD7771/AD7779 include an error correction coding (ECC) block that can correct up to two fuses per fuse bank. In total, there are four fuse banks.

The registers and fuses incorporate a CRC block that is calculated on all on-chip registers, including write/read registers, configuration registers, and test registers, storing the result. Every few microseconds, the CRC is recalculated and compared to the stored value. If the CRC values stored and the CRC values calculated do not match, the memory map (MEMMAP) is corrupted. Every time the memory map is accessed, the CRC is recalculated and stored.

The CRC is calculated and compared to the value read from the fuse block itself with the following expression:

$$x^{16} + x^{14} + x^{13} + x^{12} + x^{10} + x^{8} + x^{6} + x^{4} + x^{3} + x^{1} + x^{0}$$

When an error is found during ROM verification or the MEMMAP is corrupted, the ROM_CRC_ERR bit or the MEMMAP_CRC_ERR bit is asserted, respectively. These bits are located within the GEN_ERR_REG_1 register, Register 0x059. If an error occurs, reset the device.

These checkers, enabled by default, are disabled by clearing the MEMMAP_CRC_TEST_EN bit and/or the ROM_CRC_TEST_EN bit in the GEN_ERR_REG_1_EN register, Register 0x05A, Bits[5:4].

MCLK SWITCH ERROR

The AD7770/AD7771/AD7779 integrate an internal oscillator clock that initializes the devices at power-up. After power-up, the AD7770/AD7771/AD7779 pass the clocking control to the external oscillator. If an error occurs in the handover, the EXT_MCLK_SWITCH_ERR bit (GEN_ERR_REG_2, Register 0x05B, Bit 4) is asserted, indicating the handover did not take place properly, and the device operates using the internal oscillator. In this case, the AD7770/AD7771/AD7779 can be accessed, and registers can be read from or written to, but the Σ-Δ does not generate any conversion result. By checking the conversion result, it can be diagnosed whether the handover took place properly or not.

This error assumes a minimum clock of 265 kHz. When the external clock is between 132 kHz and 265 kHz, depending on the internal synchronization between the internal oscillator and the external clock, the error may not trigger. Therefore, if the external clock is lower than 265 kHz, disable the checker by setting the CLK_QUAL_DIS bit, (GENERAL_USER_CONFIG_3, Register 0x013, Bit 0). Setting this bit also clears the error. If the external clock is higher than 265 kHz and the error triggers, reset the device.

INTERFACE INTEGRITY

The integrity of the AD7770/AD7771/AD7779 digital data transfers is important to prevent any miscommunication between the ADC and the system, or vice versa, causing the incorrect information to be transferred and processed.

SPI TRANSMISSION ERRORS

When using the AD7770/AD7771/AD7779 in SPI mode, the SPI interface reads from the memory map registers and writes to any configuration register, in addition to reading the ADC data. Different error checkers are implemented to detect errors in the data that is transmitted. These errors are not recovered automatically, and the flag and the ALERT pin is set until the register is read back and a new SPI frame is issued.

INVALID READ/WRITE

When the master is trying to read an invalid register address, or write to an invalid register address or a read only register, the SPI_INVALID_READ_ERR bit or the SPI_INVALID_WRITE_ERR bit is asserted, which can be found on the GEN_ERR_REG_1 register (Register 0x059), and the read/write operation is ignored.

SCLK COUNTER

Any SPI transaction is a multiple of eight clocks. The AD7770/AD7771/AD7779 include an internal counter that triggers a flag, the SPI_CLK_COUNT_ERR bit located in the GEN_ERR_REG_1 register (Register 0x059), if the number of clocks counted while the $\overline{CS}$ pin is low does not equal to a multiple of eight. It asserts when the $\overline{CS}$ pin returns to high. If a write operation is being performed and the SCLK clock line contains an incorrect number of SCLK pulses, the value is not written to the addressed register and the write operation is aborted.

To verify whether the transaction took place correctly, it is recommended to read the register that attempted to write when the error triggered.

CRC CHECKSUM ERROR

If the SPI CRC is enabled (Register 0x05A, Bit 0, the SPI_CRC_TEST_EN bit), eight CRC bits are appended to any SPI transaction, shown in Figure 7.

If the CRC calculated by the AD7770/AD7771/AD7779 does not match the CRC transmitted by the master, the CRC error triggers, setting the SPI_CRC_ERR bit (Register 0x059, Bit 0), the ALERT pin, and the ALERT bit in the Σ-Δ header until the register is read back. The received message is then ignored.

The SPI CRC only affects write/read register map commands and SAR output conversions.

To calculate the CRC for a write operation, the R/$\overline{W}$ bit, seven address bits, and data bits are used.

The AD7770/AD7771/AD7779 append eight CRC bits to every data transmitted. If the previous command is a write register command, the SDO pin shifts out the same data that has been previously received.

If the command is a readback register command, the AD7770/AD7771/AD7779 use the R/$\overline{W}$ bit of the received readback command, including the 7-bit address, and the readback data from the addressed register to calculate the CRC.

If the SPI interface reads back the SAR conversion results, the CRC is calculated using the b0000 header and the 12 bits of SAR conversion data.

To read back the SAR results from the SPI interface, set the SAR_DIAG_MODE_EN bit, located on the GENERAL_USER_CONFIG_2 register (Register 0x012, Bit 5).

The CRC checksum is calculated by the following polynomial expression:

$$x^8 + x^2 + x + 1$$

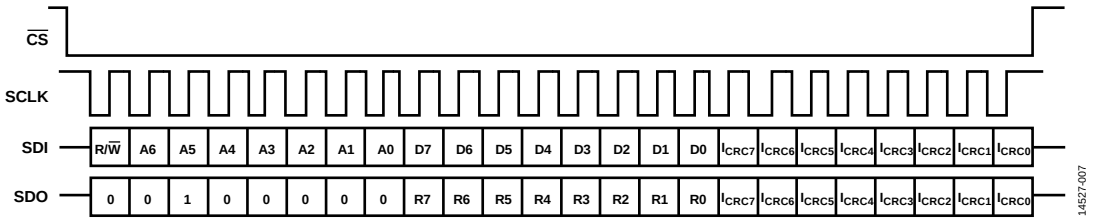

Figure 7. SPI with CRC

SIGMA-DELTA CONVERSION

The Σ-Δ conversion can be read back through the data output interface or the SPI interface.

In pin control mode, select the interface through the FORMAT0 and FORMAT1 pins. When in SPI control mode, the SPI_SLAVE_MODE_EN bit (Register 0x013, Bit 4) must be set to clock out the ADC data through the SPI interface instead of the DOUT interface, which is selected by default.

The readback data format from the Σ-Δ contains 32 bits per channel, 8 header bits, and 24 data bits as shown in Figure 2. By default, the eight header bits of the Σ-Δ contain an alert bit that offers the same information as the ALERT pin, the channel source of the data, and the four CRC bits, as shown in Figure 3.

The CRC is calculated using the data from two pairing, for example, Channel 0 and Channel 1, Channel 2 and Channel 3, Channel 4 and Channel 5, or Channel 6 and Channel 7. In total, 56 bits are used, for example, for the second channel pairing, Channel 2 and Channel 3, where:

56 Bits = Alert Bit + 3 ADC Channel Bits (010) +
24 Data Bits (Channel 2) + Alert Bit +
3 ADC Channel Bits (011) + 24 Data Bits (Channel 3)

The first pairing channel contains the CRC MSB and the second paring contains the CRC LSB.

If the received data does not match the CRC appended, ignore the ADC data.

When any of the interface errors are triggered, the ALERT pin asserts and remains asserted until the error register is read, that is, until a new SPI transaction is performed successfully. By default, the SPI error checkers are disabled but can be enabled through the GEN_ERR_REG_1_EN register, Register 0x05A.

SUPPLIES

When the AD7770/AD7771/AD7779 initialize while the devices are in operation, further monitoring is performed to check the voltage levels and determine if any reset occurs.

INTERNAL LOW DROPOUT REGULATORS (LDOs) STATUS

The AD7770/AD7771/AD7779 have two on-chip LDOs for the analog block (ALDO1 and ALDO2) and one for the digital core (DLDO). Internal comparators monitor each LDO output voltage level, and an error flag generates when the voltage surpasses a predefined threshold level.

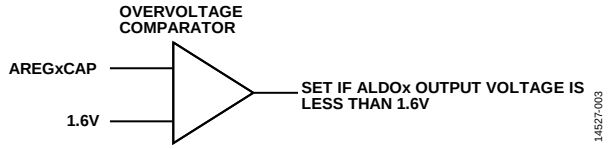

Figure 8. Analog LDO Monitor

If the voltage in any of the three LDOs drops for a few microseconds below its threshold, the corresponding bit is asserted, specifically: ALDO1_PSM_ERR, ALDO2_PSM_ERR, or DLDO_PSM_ERR, located on the GEN_ERR_REG_2 register, Register 0x05B, Bits[2:0].

These internal LDOs can be individually overdriven, if required, by setting Bits[2:0] in the BUFFER_CONFIG_2 register, Register 0x01A, and an external supply can be applied directly to the AREG1CAP, AREG2CAP, or DREGCAP pins. In this case, the external output voltage is sensed.

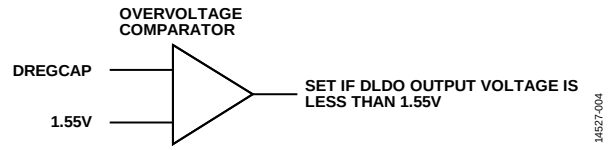

Figure 9. Digital LDO Monitor

All three checkers are individually enabled/disabled through the GEN_ERR_REG_2_EN, Register 0x05C, Bits[3:2].

When any of the three error checkers trigger, they can be verified by using the on-chip SAR ADC and connecting the multiplexer on the SAR input to the corresponding LDO, as explained in the SAR ADC section.

The levels of the internal monitors can be manually triggered to check if the detector works correctly by appropriately setting the LDO_PSM_TRIP_TEST_EN bits, Register 0x05C, Bits[1:0]. These bits increase the comparator window threshold above the LDO outputs, forcing the comparator to trigger.

RESETS AND POWER-UP

The AD7770/AD7771/AD7779 registers can be reset to their default values in any of the following cases:

- In power-up, when the LDO reaches a minimum level and triggers the power-on reset (POR) circuit.
- Introducing a pulse on the $\overline{\text{RESET}}$ input pin. This is recommended just after powering up the device, to guarantee a correct initialization.
- Writing to the SOFT_RESET bits in the GENERAL_USER_CONFIG_1 register (Register 0x011, Bits[1:0]) in the corresponding sequence, for example, writing first to SOFT_RESET = 11, followed by SOFT_RESET = 10.
- Clocking in 64 consecutive 1s through the SDI pin.

In any of the previous cases, the AD7770/AD7771/AD7779 reset and consequently, the RESET_DETECTED bit (GEN_ERR_REG_2, Register 0x05B, Bit 5) is active.

The AD7770/AD7771/AD7779 remain in reset until all the LDO outputs are at the correct levels. The assertion of the RESET_DETECTED bit indicates a reset occurred, by either software or hardware. For instance, the RESET_DETECTED bit detects a glitch on the $\overline{\text{RESET}}$ pin.

When the RESET_DETECTED bit is asserted, it is cleared by reading the GEN_ERR_REG_2 register, Register 0x05B in SPI control mode or toggling the $\overline{\text{SYNC\_IN}}$ pin in both SPI and pin control modes.

SAR ADC

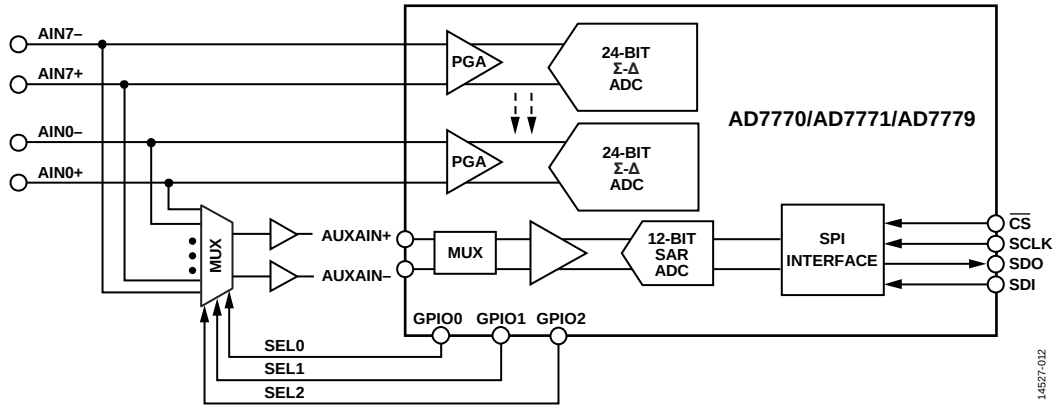

Figure 10. SAR ADC for Diagnostic Purposes

The SAR ADC on the AD7770/AD7771/AD7779 is used for many of the diagnostic functions explained previously, both on-chip and at a system level. Because it is controlled and powered independently from the main ADC channels, that is, from AVDD4 and AVSS4 pins, it can be preferable to use the SAR for this function because there is no disruption to the main ADC conversions. Use of the SAR for diagnostic purposes reduces the risk of common cause failures that occur when using another Σ-Δ ADC channel for diagnostic purposes, because the SAR uses SPI pins rather than the data output interface to clock out the ADC data. Using an external multiplexer, shown in Figure 10, through which select lines may be controlled by the AD7770/AD7771/AD7779 general-purpose input/output (GPIO) pins and some signal conditioning, can enable the SAR ADC to diagnose a signal channel without decommissioning any other Σ-Δ ADC dedicated to system measurement functions.

When the SAR ADC is enabled through the SAR_DIAG_MODE_EN bit (Register 0x012, Bit 5), all data shifted out from the SDO pin line come from the SAR ADC; therefore, the Σ-Δ ADC can simultaneously use the DOUT interface without disruption.

DIAGNOSTICS MULTIPLEXER

A multiplexer precedes the SAR ADC, shown in Figure 11, allowing the selection between a pair of external pins (AUXAIN+/AUXAIN–) and various on-chip supplies, signals, LDO output voltages, references, and the temperature of the die.

Table 6 states all the possible nodes that can be connected to the SAR ADC through the multiplexer, some of which have been mentioned previously in this application note, for monitoring purposes. This multiplexer is controlled over the GLOBAL_MUX_CONFIG register, Register 0x016, Bits[7:3]. Depending on the configuration of these bits, the SAR ADC input connects at different signals, as described in Table 6. When one of the previous errors triggers, if the corresponding signal is available to be connected to the SAR input, the SAR ADC can monitor the voltage level so it can be used for diagnostics purposes.

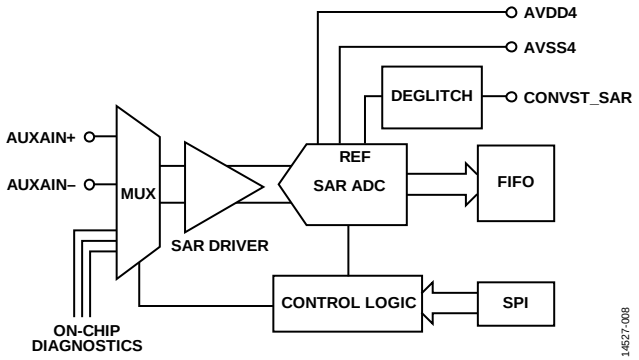

Figure 11. SAR ADC Signal Chain Including the Multiplexer, Driver Amplifier, ADC, and Logic Circuitry

Table 6. SAR Multiplexer Inputs

GLOBAL_MUX_CTRL	SAR AIN+[1]	SAR AIN−[1]	Attenuation ÷ 6
00000	AUXAIN+	AUXAIN−	No
00001	DV_{BE}	AVSSx	No
00010	REF1+	REF1−	No
00011	REF2+	REF2−	No
00100	REF_OUT	AVSSx	No
00101	VCM	AVSSx	No
00110	AREG1CAP	AVSSx	Yes
00111	AREG2CAP	AVSSx	Yes
01000	DREGCAP	DGND	Yes
01001	AVDD1A	AVSSx	Yes
01010	AVDD1B	AVSSx	Yes
01011	AVDD2A	AVSSx	Yes
01100	AVDD2B	AVSSx	Yes
01101	IOVDD	DGND	Yes
01110	AVDD4	AVSSx	No
01111	DGND	AVSSx	Yes
10000	DGND	AVSSx	Yes
10001	DGND	AVSSx	Yes
10010	AVDD4	AVSSx	Yes
10011	REF1+	AVSSx	No
10100	REF2+	AVSSx	No
10101	AVSSx	AVDD4	Yes

[1] AVSSx stands for the AVSS1 through AVSS4 pins.

SIGMA-DELTA ADC MULTIPLEXER

Every Σ-Δ ADC can also be used for diagnostic purposes, provided there is a multiplexer on the signal path before the PGA (see Figure 1), which allows the input from the converter to be connected to a zero scale, positive full scale, negative full scale, or a fixed 280 mV differential signal to verify the correct operation of the channel, shown in Figure 12.

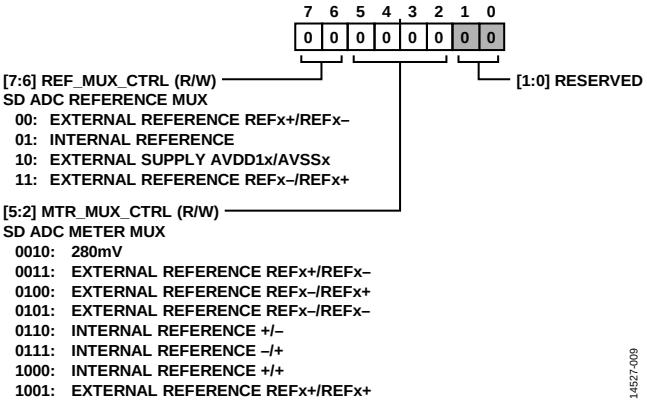

Figure 12. ADC_MUX_CONFIG Register that Allows Selecting the Reference and the Input to the ADCs

The diagnostic multiplexer is enabled through the CHx_RX bit on the CHx_CONFIG register of the channel of interest. Then, the multiplexer can be controlled through the MTR_MUX_CTRL bits on the ADC_MUX_CONFIG register, Register 0x015, Bits[5:2]. Therefore, this internal multiplexer can also be used for diagnostic purposes, as mentioned in the PGA Gain section and in the Reference Detection section.

The AD7770/AD7771/AD7779 have features that enable the user to monitor the internal blocks, diagnose when alerts happen, and verify if errors are present. The device can also apply different methods to correct these errors. All of these features make the AD7770/AD7771/AD7779 ideal solutions for applications that require diagnostics for functional safety.

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