Key Sheet
AD7790

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Highlights of the AD7790—Low Power, 16-Bit, Buffered Sigma-Delta ADC

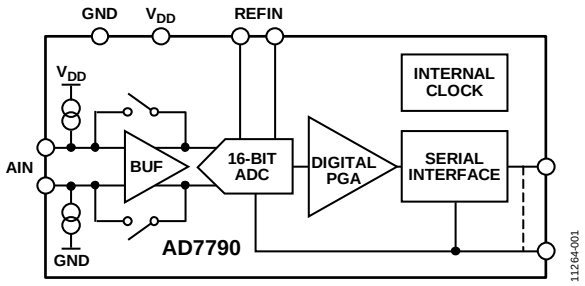

Figure 1. Functional Block Diagram

GENERAL DESCRIPTION

This key sheet[1] provides users with an overview of the AD7790. Key attributes of the part include the following:

- Designed for the measurement of wide dynamic range, low frequency signals, such as those in pressure transducers, weigh scales, and temperature measurement applications.
- Low power, flexible, high performance, low noise, 16-bit sigma-delta (Σ-Δ) ADC suitable for converting low input bandwidth analog signals with a fully flexible output data rate (ODR) between 9.5 SPS and 120 SPS.
- Single fully differential analog channel with ultralow power consumption.
- With an ODR of 9.5 SPS, the AD7790 boasts an rms noise of 1.1 μV.
- User friendly, with the part being fully configurable over a 4-wire serial interface.
- Available in a 10-lead MSOP package, allowing a reduced board size.

FEATURES AND BENEFITS

The AD7790 offers the following features and benefits:

- Simultaneous 50 Hz and 60 Hz rejection at 16.6 SPS ODR
- Optional internal rail-to-rail input buffer
- Three MCLK divide options, allowing further reduction in power dissipation
- Ultralow noise performance across the ODR range
- Fully compatible with SPI, QSPI™, MICROWIRE®, and DSP
- SPI configuration control
- 3-wire serial digital interface (Schmitt trigger on SCLK)

[1] This document provides users with an overview of the AD7790; it is not a notice of performance or intent. Refer to the AD7790 data sheet for performance and more specific information about this product.

Rev. 0

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KEY CHARACTERISTICS

FUNDAMENTAL SPECIFICATIONS

Table 1.

Parameter	Min	Typ	Max	Unit
ADC Type		Σ- Δ ADC		
Number of Input Channels		One fully differential input channel		
Resolution	16		16	Bits
Output Data Rate (ODR)	9.5		120	SPS
Differential Input Voltage Range	−REFIN/gain		+REFIN/gain	V
Power Supply Voltage				
V_{DD} with Respect to GND	2.5		5.25	V
Power Supply Current				
With V_{DD} = 3.6 V, Buffer Off		65	75	μA
With V_{DD} = 5.25 V, Buffer On		145	160	μA
Offset Error		±3		μV
Offset Error Drift vs. Temperature		±10		nV/°C
Full-Scale Error		±10		μV
Gain Drift vs. Temperature		±0.5		ppm/°C
Integral Nonlinearity (INL)	−15	±3.5	+15	ppm of FSR
Power Supply Rejection	90			dB
Operating Temperature Range	−40		+105	°C

NOISE

Table 2. Output Data Rates and RMS Noise

Output Data Rate (SPS)	f_{3dB} (Hz)	RMS Noise (μV)	Rejection
120	28	40	25 dB @ 60 Hz
100	24	25	25 dB @ 50 Hz
33.3	8	3.36	
20	4.7	1.6	80 dB @ 60 Hz
16.6	4	1.5	65 dB @ 50 Hz and 60 Hz (default setting)[1]
16.7	4	1.5	80 dB @ 50 Hz
13.3	3.2	1.2	
9.5	2.3	1.1	62 dB @ 50 Hz and 60 Hz

[1] Simultaneous 50 Hz and 60 Hz rejection is optimized when the ODR equals 16.6 SPS because notches are placed at both 50 Hz and 60 Hz with this update rate.

OPERATING THE AD7790

DATA INTERFACE

The data interface for the AD7790 is

- Performed using a 4- or 3-wire SPI
- Compatible with SPI, QSPI, MICROWIRE, and DSP
- Allows a user to both write to and read from the AD7790 on the same data bus
- Indicates when transferred data is available by bringing the DOUT/$\overline{RDY}$ signal and the $\overline{RDY}$ bit in the status register low

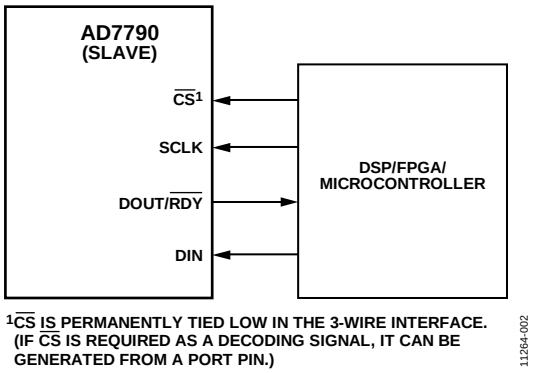

Figure 2. AD7790 Data Interface, 4-Wire SPI

Table 3. 4-Wire Serial Interface Pin Functions

Pin	Function
$\overline{CS}$[1]	Selects the ADC (also applicable in systems with multiple devices on the serial bus).
	Provides a frame synchronization signal.[2]
SCLK	Determines when data transfers (either on DIN or DOUT/$\overline{RDY}$) occur.
DOUT/$\overline{RDY}$	Accesses data from the on-chip registers.
	Indicates when the transferred data is available.
DIN	Transfers data into the on-chip registers.

[1] $\overline{CS}$ is permanently tied low in the 3-wire interface. (If $\overline{CS}$ is required as a decoding signal, it can be generated from a port pin.)

[2] Useful for DSP interfaces. The first bit (MSB) is effectively clocked out by $\overline{CS}$ because $\overline{CS}$ typically occurs after the falling edge of SCLK in DSPs. The SCLK can continue to run between data transfers, provided the timing numbers are obeyed.

DATA MODES

There are three data modes available: continuous conversion mode, continuous read mode, and single conversion mode.

Continuous Conversion Mode (Default)

Continuous conversion is the default power-up mode. In this mode, the AD7790 converts continuously, and the $\overline{RDY}$ bit in the status register goes low each time a conversion is complete. If $\overline{CS}$ is low, the DOUT/$\overline{RDY}$ line also goes low when a conversion is complete. To read a conversion, the user writes to the communications register, indicating that the next operation is a read of the data register. When the data-word has been read from the data register, DOUT/$\overline{RDY}$ goes high. The user can read this register additional times, if required.

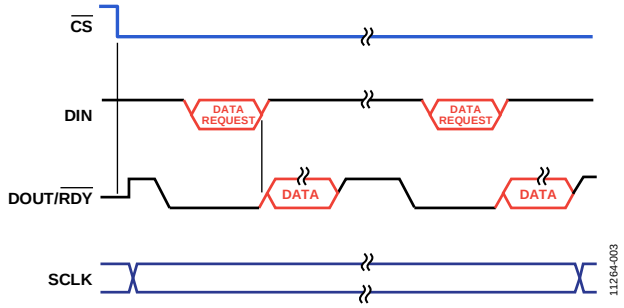

Figure 3. Continuous Conversion Mode

Continuous Read Mode

Rather than write to the communications register each time a conversion is complete to access the data, the AD7790 can be configured so that the conversions are automatically placed on the DOUT/$\overline{RDY}$ line. By writing 001111XX (where XX represent don't cares) to the communications register, the user need only apply the appropriate number of SCLK cycles to the ADC, and the conversion word is automatically placed on the DOUT/$\overline{RDY}$ line when a conversion is complete.

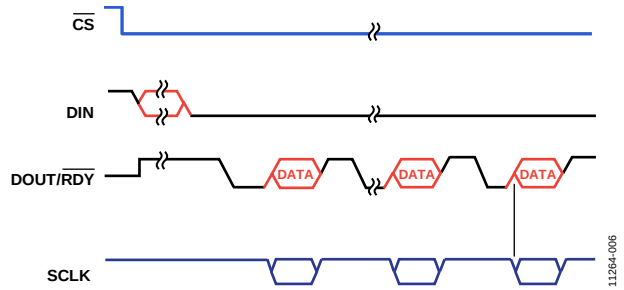

Figure 4. Continuous Read Mode

In continuous read mode, the serial interface is dedicated to reads of the data register. If any other register needs to be accessed, continuous read mode must be disabled. In addition, every time a conversion is available, the serial interface is reset in this mode. Therefore, it is essential that the conversion be read before the next conversion is available.

While in the continuous read mode, the ADC monitors activity on the DIN line so that it can receive the instruction to exit the continuous read mode. Additionally, a reset occurs if 32 consecutive 1s are seen on DIN. Therefore, DIN should be held low in continuous read mode until an instruction is to be written to the device.

Single Conversion Mode

In single conversion mode, the AD7790 performs a single conversion and is placed in standby mode after the conversion is complete. DOUT/$\overline{RDY}$ goes low to indicate the completion of a conversion. When the data-word has been read from the data register, DOUT/$\overline{RDY}$ goes high. The data register can be read several times, if required, even when DOUT/$\overline{RDY}$ has gone high.

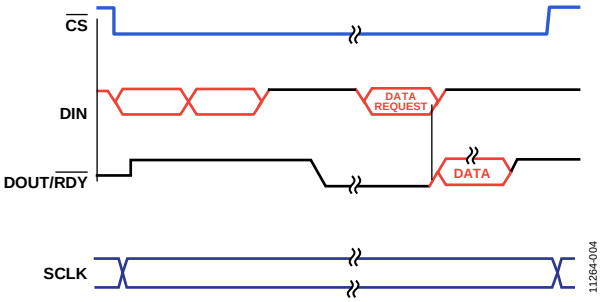

Figure 5. Single Conversion Mode

TYPICAL APPLICATION DIAGRAM

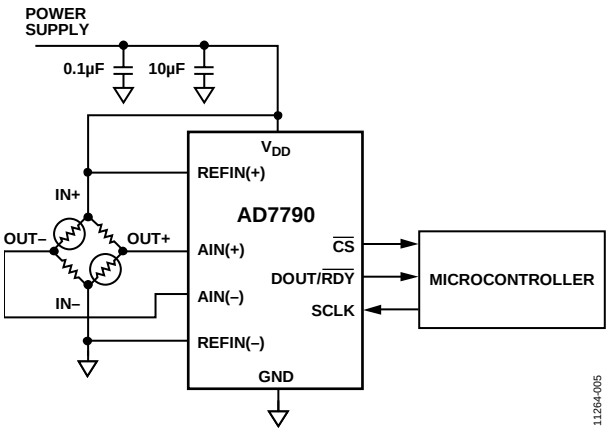

Figure 6. Typical Application Diagram

FREQUENTLY ASKED QUESTIONS

What is the optional internal rail-to-rail buffer?
The AD7790 has one differential analog input channel that is

- Connected to the on-chip buffer amplifier when the device is operated in buffered mode
- Connected directly to the modulator when the device is operated in unbuffered mode

In buffered mode, the input channel feeds into a high impedance input stage of the buffer amplifier. Therefore, the input can tolerate significant source impedances and is tailored for direct connection to external resistive-type sensors, such as strain gauges or resistance temperature detectors (RTDs).

What is 50 Hz and 60 Hz rejection?
The mains power supply generates interference at 50 Hz or 60 Hz, with the frequency varying from one country to another. The AD7790 has the ability to simultaneously reject 50 Hz and 60 Hz signals at an ODR of 16.6 SPS.

What MCLK divide options are available?
The AD7790 has a current consumption of 160 μA maximum when operated with the buffer enabled and with a 5 V power supply. The power can be reduced further by setting the CDIV1 and CDIV0 bits in the filter register appropriately.

By setting these bits, the internal clock is divided by 2, 4, or 8 before being applied to the modulator and filter, resulting in a reduction of the output data rate and a reduction in the digital current.

How do I interface with the part?
The part can be configured by using a 4-wire SPI interface; this interface is also used as the data interface. The SPI interface allows the user to read the status of the part and to change the setup.

Are there any ESD protection schemes that should be considered for the AD7790?
This converter is manufactured on a standard CMOS process; therefore, all standard practices and protection schemes that apply to other CMOS devices also apply to this device. There are ESD protection diodes on all the inputs that protect the device from possible ESD damage due to handling and production. To determine the appropriate ESD precautions, refer to the AD7790 data sheet for information about the absolute maximum ratings.

Is an antialiasing filter required?
The analog input is sampled at 64 kHz. The digital filter does not provide any rejection at this frequency or at frequencies that are multiples of 64 kHz; an external antialiasing filter is required to provide rejection at these frequencies, with a simple RC filter being sufficient. Typical values for the filter are

- 1 kΩ resistor in series with each analog input
- 0.1 μF capacitor between the analog input pins
- 0.01 μF capacitor from each input pin to ground

These typical values can be used only when the buffer is enabled. When the buffer is disabled, smaller RC values are required because larger values can cause gain errors.

Can filtering be added to the reference pins?
The reference input to the AD7790 is not buffered. Therefore, the filtering must be limited on the reference pins because large RC values can cause gain errors. Suitable capacitor values are

- 2200 pF capacitor between the reference pins
- 220 pF capacitor from each pin to ground

With these capacitor values, there can be some resistance in parallel with the reference pins. However, it must be limited to less than 100 Ω.

LEARN MORE AND START DESIGNING

To learn more about the AD7790 and compatible products or to sample and buy the AD7790 device, click on the links provided or contact an Analog Devices, Inc., sales representative.

COMPATIBLE DEVICES

Table 4. Recommended Compatible Devices[1]

Linear Regulators	Precision References	ADC Driver Amplifiers	Circuits from the Lab™	Evaluation Board
ADP3303 family ADP3330 family	ADR380 family ADR361 family	N/A (the AD7790 includes an on-board internal buffer)	CN-0271, *K-Type Thermocouple Measurement System with Integrated Cold Junction Compensation*	AD7791 evaluation board is recommended for AD7790 evaluation

[1] Information about additional companion products are provided on the AD7790 product page.

PACKAGE DIAGRAM

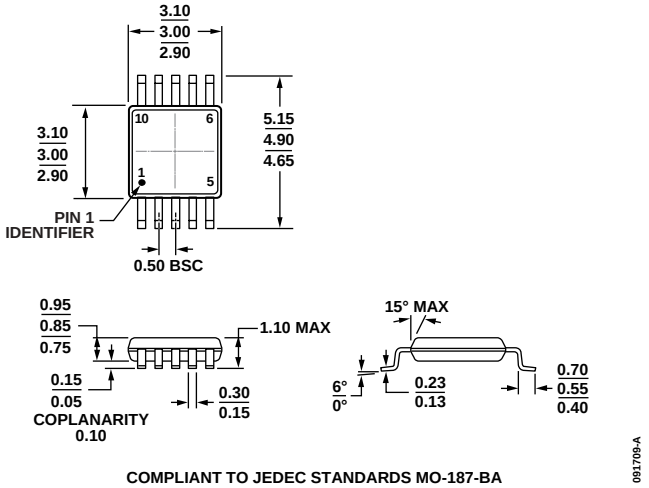

Figure 7. 10-Lead Mini Small Outline Package [MSOP]
(RM-10)
Dimensions shown in millimeters

GETTING STARTED

AD7790 DATA SHEET

SAMPLE AND BUY THE AD7790

UG11264-0-1/13(0)

ANALOG DEVICES

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