ANALOG DEVICES

AN-592
APPLICATION NOTE

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Recommendations for the Use of the $\overline{\text{CONVST}}$ Input of the AD7822/AD7825/AD7829 and the AD7827

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INTRODUCTION

The AD7822/AD7825/AD7829 are high speed 1-, 4-, and 8-channel parallel 8-bit ADCs, and the AD7827 is a high speed, single-channel, serial 8-bit ADC. They are all half flash ADCs with similar functionality of the $\overline{\text{CONVST}}$ input. This Application Note describes some considerations that are worth noting with the $\overline{\text{CONVST}}$ input and recommendations for avoiding any application issues.

FUNCTION OF THE $\overline{\text{CONVST}}$ INPUT

The $\overline{\text{CONVST}}$ signal is an input to the devices. It is used to power up the devices, initiate conversions, and place the devices into the Power-Down Mode.

A falling edge on $\overline{\text{CONVST}}$ places the track-and-hold into hold mode and thus initiates an 8-bit analog-to-digital conversion. The track-and-hold goes back into track 120 ns after the start of the conversion. The state of the $\overline{\text{CONVST}}$ signal is checked at the end of a conversion, and if it is logic low, the devices will power down. If in power-down, a rising edge on $\overline{\text{CONVST}}$ will power up the devices.

$\overline{\text{CONVST}}$ INPUT TROUBLESHOOTING

When V_{DD} is first applied, the devices are in a low current mode of operation. These devices therefore need to be powered up before conversions can be initiated. This is done by applying a rising edge to the $\overline{\text{CONVST}}$ pin. It is important that V_{DD} is stable before this rising edge is applied. If $\overline{\text{CONVST}}$ rises before V_{DD} has settled, or if it goes above V_{DD} while it is rising, the devices will attempt to power up but will fail to do so properly. Subsequently, when $\overline{\text{CONVST}}$ then goes low either by bringing it low to initiate a conversion or by the falling edge of a glitch on the line, the devices will fail to convert correctly. This is due to conversions being initiated with the devices not being powered up properly. This can cause the devices to lock up and will result in no end of conversion (EOC) signal being returned by the particular device, meaning it has failed to convert correctly. If this occurs, the recovery method is to perform a power cycle while ensuring $\overline{\text{CONVST}}$ does not rise before V_{DD}.

RECOMMENDATIONS

Ideally, to avoid any issues, $\overline{\text{CONVST}}$ should either be maintained low until V_{DD} has settled or remain at a lower voltage than V_{DD} while it is rising. It should also never be floating once V_{DD} is applied. If this cannot be guaranteed, then it is recommended that the $\overline{\text{CONVST}}$ input be forced to track the V_{DD} voltage but never rise above it. This is achieved by connecting a 10 kΩ pull-up resistor and a Schottky diode in parallel, between $\overline{\text{CONVST}}$ and V_{DD}. By doing this, $\overline{\text{CONVST}}$ will never rise before V_{DD} nor glitch when V_{DD} is rising. Figure 1 shows a typical connection diagram for the AD7827 (the $\overline{\text{CONVST}}$ connection in this diagram also applies to the AD7822/AD7825/AD7829 parallel devices).

It is important to also note that $\overline{\text{CONVST}}$ (or any other inputs to the devices) should never be applied before V_{DD} because by doing so the maximum ratings of the particular device will be exceeded resulting in possible permanent damage. See the Absolute Maximum Ratings of the particular data sheet for more detailed information.

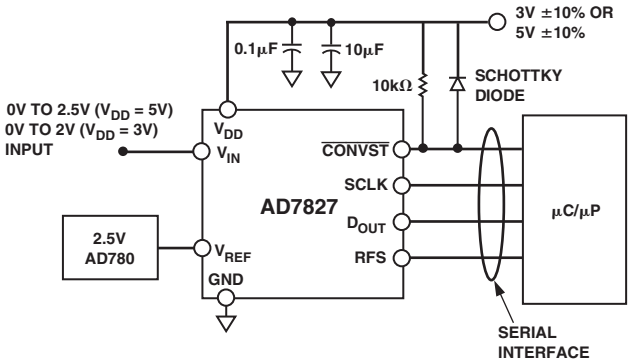

Figure 1. Typical Connection Diagram of the AD7827

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