ANALOG DEVICES

AN-229
APPLICATION NOTE

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Evaluation Board for the AD7885 16-Bit A/D Converter

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INTRODUCTION

This application note describes the evaluation board for the AD7885 16-bit A/D converter. This is a 16-bit monolithic analog-to-digital converter with internal sample-and-hold and a conversion time of 5.3 μs. The throughput rate is 166 kSPS. It uses a 2-pass flash architecture to achieve this speed and throughput. It has both ac and dc specifications. Integral Linearity Error is ±0.006% FSR, and the Signal to (Noise + Distortion) Ratio is 84 dB. Its fast 8-bit byte output interface is compatible with both microcontrollers (8051, 68HC11, etc.) and general purpose processors (MC6800 Series, MC68008, 8088, Z80, etc.). Full information on the converter is in the AD7884/AD7885 data sheet from Analog Devices. This should be consulted in conjunction with the application note when using the evaluation board.

The board operates from +15 and −15 volt power supplies. On-board components include the reference and op amp circuitry necessary for the analog front-end and output latches for interfacing to a 16-bit processor bus.

A full circuit diagram for the AD7885 board is shown in Figure 3.

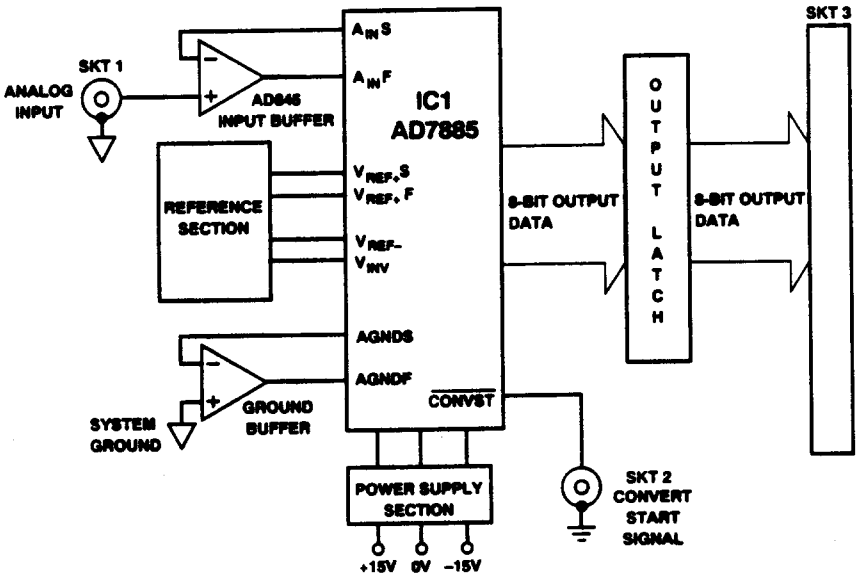

Figure 1. Evaluation Board Block Diagram

LINK OPTIONS

The evaluation board has a number of link options available and these are summarized in Table I below.

Table I. Link Options

Link No.	Function
LK1–LK4	Links 1–4 enable the user to select either the ±3 volt input range or the ±5 volt input range.
LK5	This allows $\overline{RD}$ to be tied permanently low.
LK6	This allows $\overline{CS}$ to be tied permanently low.

POWER SUPPLIES, GROUNDING AND DECOUPLING

The board is powered from a ±15 V supply. These supplies drive two 5 V regulators (IC7 and IC8) which produce the ±5 V required for the AD7885. The AD7885 has one AV_{DD} pin and one V_{DD} pin. These are driven from the same +5 V supply. The AV_{DD} pin is decoupled to signal ground with a 10 μF tantalum and a 0.1 μF ceramic capacitor. The V_{DD} pin is decoupled with a 0.1 μF capacitor only. The same decoupling arrangement is used for the negative supply pins. AV_{SS} is decoupled to signal ground with 10 μF and 0.1 μF while V_{SS} is decoupled with 0.1 μF.

The ±15 V supplies also drive the analog front-end circuitry which includes the AD586 reference and the op amps A1–A4. These are decoupled to signal ground with 10 μF tantalum and 0.1 μF ceramic disc capacitors. Power for the digital section of the board (IC9, IC10 and C11) should be applied at Pin 23 of SKT 3. The digital supply is routed separately from the analog section and they are not joined anywhere on the board.

The evaluation board uses extensive ground planing to minimize any high frequency noise interference. The ground planing for the analog section is kept separate from that for the digital section, and they are joined only at Pin 21 (DGND) of the AD7885.

ANALOG INPUT SECTION

The analog input to the board is applied to the miniature BNC connector SKT 1, labelled A_{IN}. The input then goes to the link, LK8, and from there on to the input buffer, IC3. LK8 allows the user to divert the input to signal conditioning circuitry, which may be built on the grid section of the board. With LK8 inserted, A_{IN} goes directly to IC3, an AD845. This is a very fast JFET amplifier which combines very low input offset voltage and offset drift with fast settling and high slew rate. Consult the AD845 data sheet for full details.

The AD845 drives the AD7885 inputs through a series of links. These links allow the user to configure the ADC for either a ±3 volt input or a ±5 volt input. Table II shows the necessary link settings for each range.

Table II. LK1–LK4 Settings

Input Range	LK1	LK2	LK3	LK4
±3 Volts	AB	AB	AB	AB
±5 Volts	BC	BC	BC	BC

AGND BUFFER

IC2 is the force, sense amplifier for AGND. The AGNDS pin should be at zero potential. The board uses the OP-07 for IC2. The output of IC2 is decoupled with a 47 μF solid tantalum capacitor to AGND to deal with the fast current transients on the AGNDS pin. The stability of this arrangement is marginal, and the circuit shown in Figure 2 is used to improve phase margin. A feedback capacitor (C_F) of 47 μF should be used. This circuit compensates for the load capacitor by adding a low frequency zero and ensures an adequate phase margin.

MULTIPLEXER APPLICATIONS

When the AD7885 is used in multiplexer applications, it is possible for the analog input to see a full-scale step input. In these applications, it is better to use a very fast amplifier as the AGND buffer. Suitable op amps are the AD845 or AD847. With these, there is no need for the 47 μF capacitor to AGND at the output, and the step response time allows a throughput of 150 kHz to be achieved. Thus, if the user wishes to multiplex several channels into the AD7885, C3 and C26 should be removed, R4 and R5 should be shorted out and the OP-07 (IC2) should be replaced with either the AD845 and AD847.

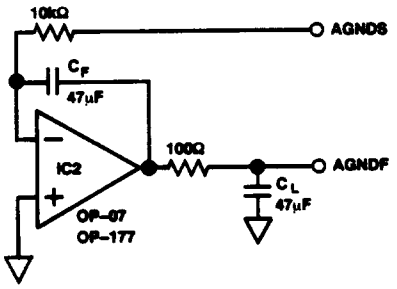

Figure 2. Compensation Circuit for AGND Buffer

REFERENCE SECTION

The required +3 V reference is derived from the AD586. The +5 V output is divided down to +3 V by R1 and R2 before being buffered by IC6. IC4 is a unity gain inverter which provides the −3 V negative reference. The gain setting resistors are on-chip and are factory-trimmed to ensure precise tracking of V_{REF+}. Figure 3 shows IC4 and IC6 as AD845s. The very high slew rate of these amplifiers have the ability to respond to the rapidly changing reference input impedance and input currents and hold the V_{REF+} and V_{REF-} inputs at the required dc input levels.

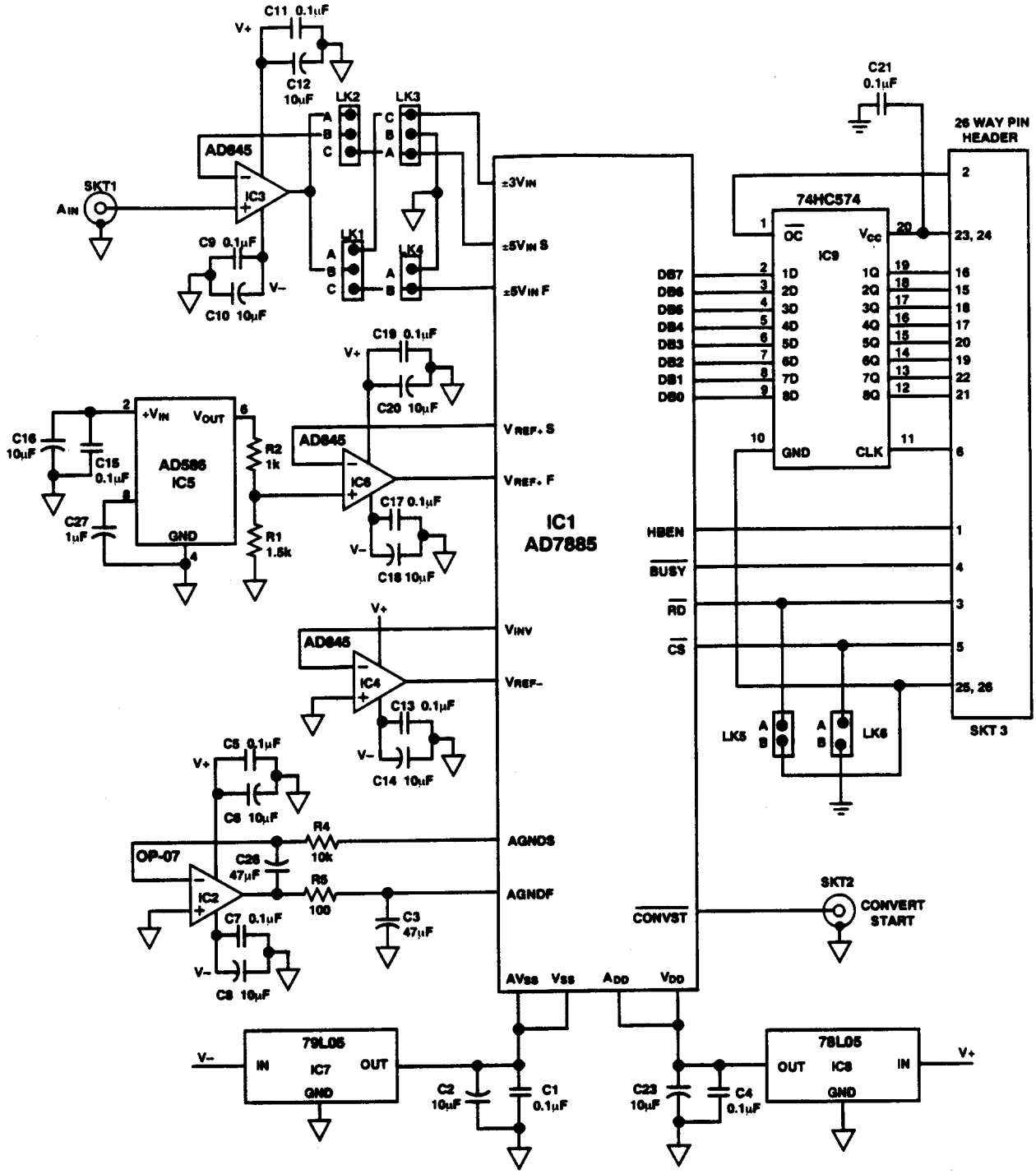

Figure 3. AD7885 Evaluation Board Circuit Diagram

EVALUATION BOARD INTERFACING

The board has an 8-bit byte interface. The 8-bit port is available at SKT 3. The pinout for SKT 3 is given in Figure 4.

onversion is initiated by applying a $\overline{\text{CONVST}}$ signal at SKT 2. $\overline{\text{BUSY}}$ is low during conversion and goes high to indicate the end of conversion. When the $\overline{\text{BUSY}}$ line goes high, it is possible to read the conversion result by bringing $\overline{\text{CS}}$ and $\overline{\text{RD}}$ low. In the two-byte read operation, the HBEN input determines whether the most significant or least significant byte is read. When HBEN is high, then the 8 MSBs are put on the bus; when HBEN is low, then the 8 LSBs are put on the bus.

It is also possible to tie $\overline{\text{CS}}$ and $\overline{\text{RD}}$ permanently low through links LK5 and LK6. This means that the data bus drivers are permanently turned on. Each new conversion result is automatically put on the bus at the end of conversion. The state of HBEN determines whether the least significant byte or the most significant byte is on the bus. The AD7885 design guarantees that the data is valid on the $\overline{\text{BUSY}}$ rising edge.

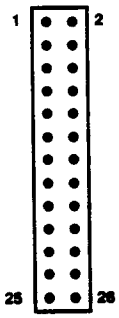

Figure 4. Pin Configuration for SKT3

BOARD LAYOUT AND COMPONENT OVERLAY

Figures 5, 6 and 7 show the evaluation board layout and component overlay. These may be used to study the grounding and decoupling techniques for the various components. There are separate analog and digital ground planes which are joined only at Pin 21 (DGND) of the AD7885.

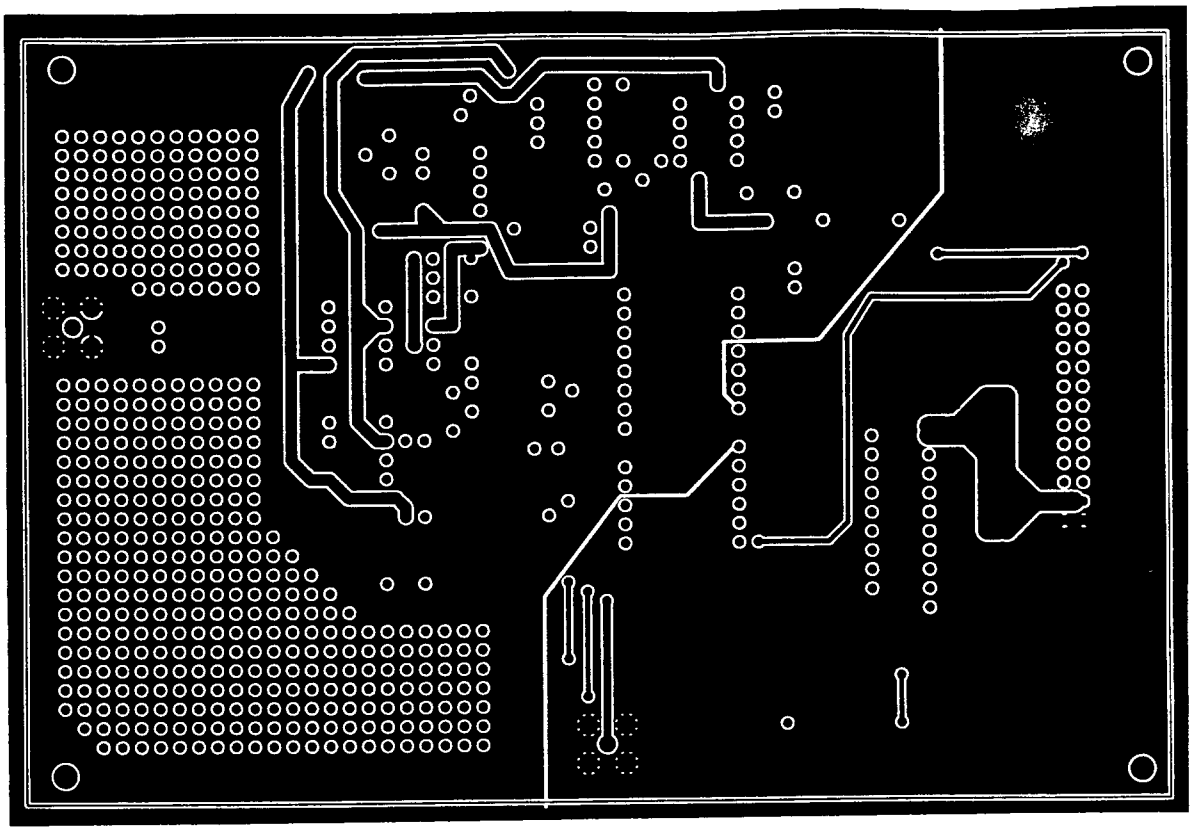

Figure 5. AD7885 Evaluation Board Component Side Layout

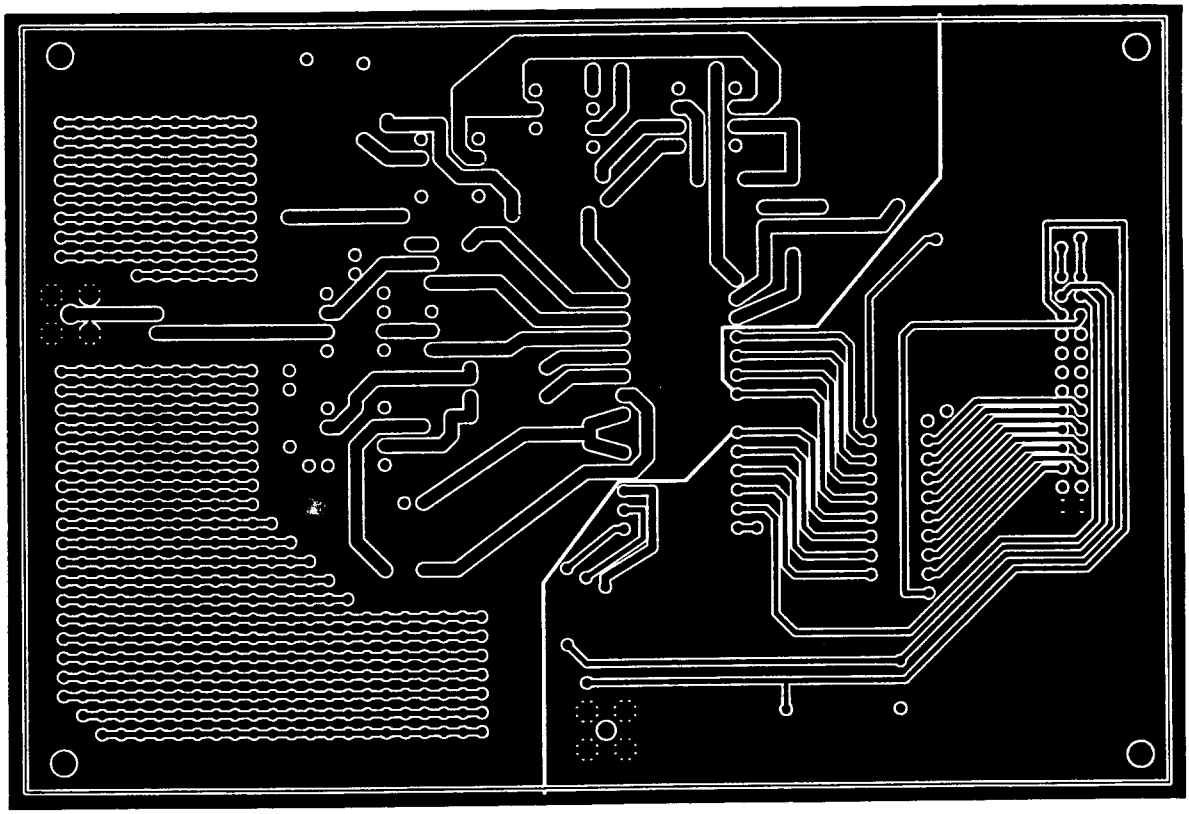

Figure 6. AD7885 Evaluation Board Solder Side Layout

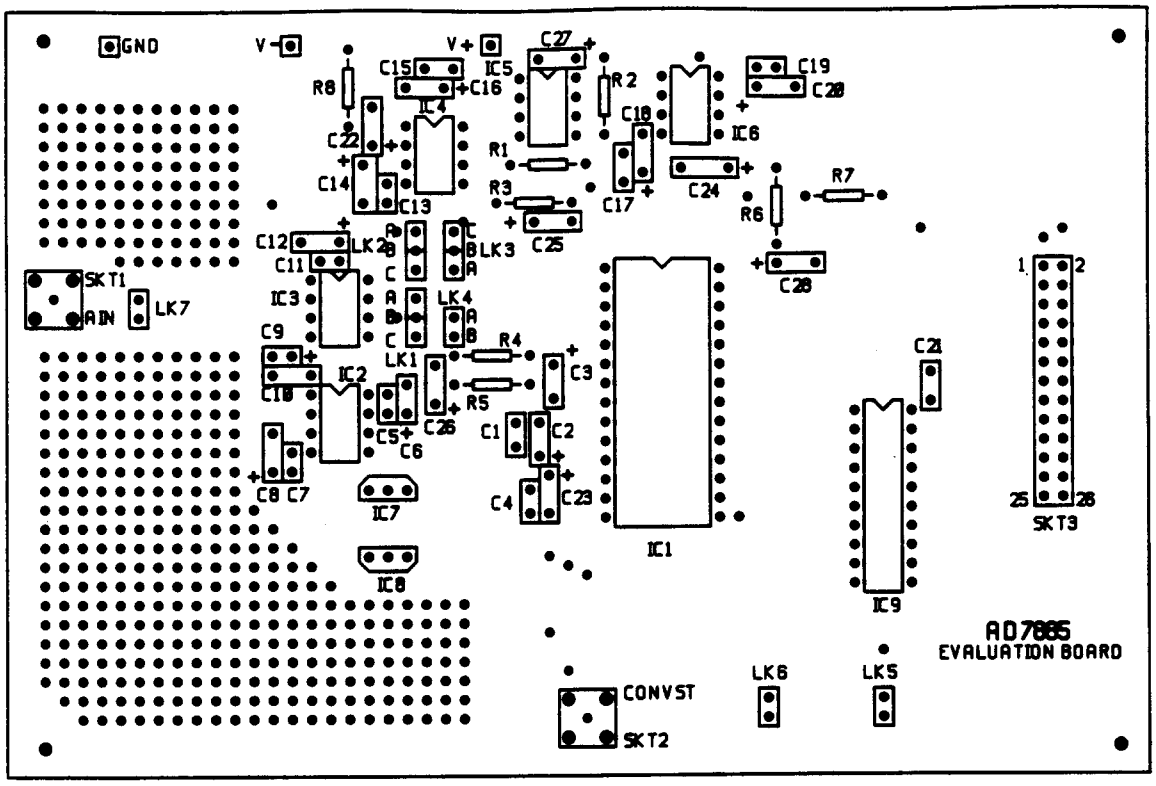

Figure 7. AD7885 Evaluation Board Component Overlay