

FEATURES

Fast throughput rate: 1 MSPS

Specified for AV_{DD} of 2.7 V to 5.25 V

Low power

6 mW maximum at 1 MSPS with 3 V supplies

13.5 mW maximum at 1 MSPS with 5 V supplies

4 single-ended inputs with sequencer

Wide input bandwidth: 70 dB SNR at 50 kHz input frequency

Flexible power/serial clock speed management

No pipeline delays

High speed serial interface: SPI/QSPI™/MICROWIRE™/DSP compatible

Shutdown mode: 0.5 μ A maximum

16-lead TSSOP package

Qualified for automotive applications

Known good die (KGD): these die are fully guaranteed to data sheet specifications.

GENERAL DESCRIPTION

The **AD7924-KGD** is a 12-bit, high speed, low power, 4-channel successive approximation ADCs. The parts operate from a single 2.7 V to 5.25 V power supply and feature throughput rates up to 1 MSPS. The part contains a low noise, wide bandwidth track-and-hold amplifier that can handle input frequencies in excess of 8 MHz.

The conversion process and data acquisition are controlled using \overline{CS} and the serial clock signal, allowing the device to easily interface with microprocessors or DSPs. The input signal is sampled on the falling edge of \overline{CS} and conversion is initiated at this point. There are no pipeline delays associated with the part.

The **AD7924-KGD** uses advanced design techniques to achieve very low power dissipation at maximum throughput rates. At maximum throughput rates, the **AD7924-KGD** consumes 2 mA maximum with 3 V supplies; with 5 V supplies, the current consumption is 2.7 mA maximum.

Through the configuration of the control register, the analog input range for the part can be selected as 0 V to REF_{IN} or 0 V to $2 \times REF_{IN}$, with either straight binary or twos complement output coding. The **AD7924-KGD** features four single-ended analog inputs with a channel sequencer to allow a preprogrammed selection of channels to be converted sequentially.

The conversion time for the **AD7924-KGD** is determined by the SCLK frequency, which is also used as the master clock to control the conversion.

Additional application and technical information can be found in the **AD7924** data sheet.

Rev. A

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FUNCTIONAL BLOCK DIAGRAM

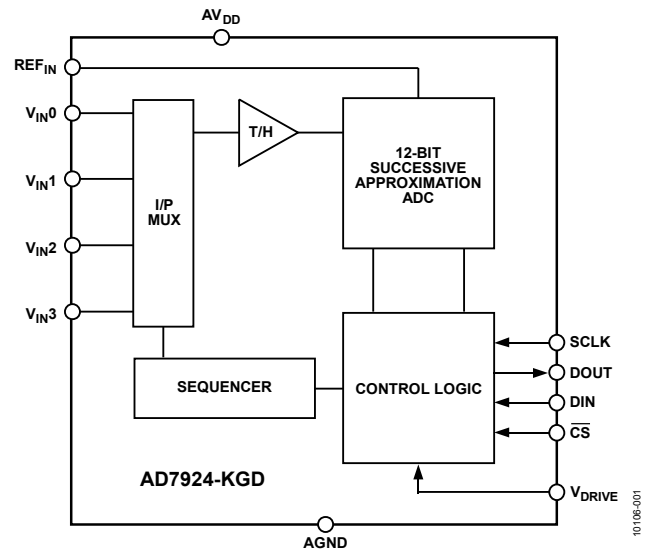


Figure 1.

PRODUCT HIGHLIGHTS

1. **High Throughput with Low Power Consumption.**
The **AD7924-KGD** offers throughput rates up to 1 MSPS. At the maximum throughput rate with 3 V supplies, the **AD7924-KGD** dissipates only 6 mW of power maximum.
2. **Four Single-Ended Inputs with Channel Sequencer.**
A consecutive sequence of channels can be selected, through which the ADC will cycle and convert on.
3. **Single-Supply Operation with V_{DRIVE} Function.**
The **AD7924-KGD** operates from a single 2.7 V to 5.25 V supply. The V_{DRIVE} function allows the serial interface to connect directly to 3 V or 5 V processor systems, independent of V_{DD} .
4. **Flexible Power/Serial Clock Speed Management.**
The conversion rate is determined by the serial clock, allowing the conversion time to be reduced by increasing the serial clock speed. The part also features two shutdown modes to maximize power efficiency at lower throughput rates. Current consumption is 0.5 μ A maximum when in full shutdown.
5. **No Pipeline Delay.**
The part features a standard successive approximation ADC with accurate control of the sampling instant via the \overline{CS} input and once-off conversion control.

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REVISION HISTORY

11/14—Rev. 0 to Rev. A

| | |
|---|---|
| Change to Bond Pad Composition Value, Table 5 | 8 |
|---|---|

10/11—Revision 0: Initial Version

SPECIFICATIONS

$V_{DD} = V_{DRIVE} = 2.7\text{ V}$ to 5.25 V , $REF_{IN} = 2.5\text{ V}$, $f_{SCLK} = 20\text{ MHz}$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Temperature range is -40°C to $+85^{\circ}\text{C}$.

Table 1.

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|--|------------------------|-----|------------------------|---------------|---|
| DYNAMIC PERFORMANCE | | | | | |
| Signal-to-(Noise + Distortion), SINAD | 70 | | | dB | $f_{IN} = 50\text{ kHz}$ sine wave, $f_{SCLK} = 20\text{ MHz}$ @ 5 V |
| | 69 | | | dB | @ 3 V, typically 69.5 dB |
| Signal-to-Noise Ratio, SNR | 70 | | | dB | |
| Total Harmonic Distortion, THD | | | -77 | dB | @ 5 V, typically -84 dB |
| | | | -73 | dB | @ 3 V, typically -77 dB |
| Peak Harmonic or Spurious Noise, SFDR | | | -78 | dB | @ 5 V, typically -86 dB |
| Intermodulation Distortion, IMD | | | | | $f_a = 40.1\text{ kHz}$, $f_b = 41.5\text{ kHz}$ |
| Second-Order Terms | | -90 | | dB | |
| Third-Order Terms | | -90 | | dB | |
| Aperture Delay | | 10 | | ns | |
| Aperture Jitter | | 50 | | ps | |
| Channel-to-Channel Isolation | | -85 | | dB | $f_{IN} = 400\text{ kHz}$ |
| Full Power Bandwidth | | 8.2 | | MHz | @ 3 dB |
| | | 1.6 | | MHz | @ 0.1 dB |
| DC ACCURACY | | | | | |
| Resolution | 12 | | | Bits | |
| Integral Nonlinearity, INL | | | ± 1 | LSB | |
| Differential Nonlinearity, DNL | | | $-0.9/+1.5$ | LSB | Guaranteed no missed codes to 12 bits |
| 0 V to REF_{IN} Input Range | | | | | Straight binary output coding |
| Offset Error | | | ± 8 | LSB | Typically ± 0.5 LSB |
| Offset Error Match | | | ± 0.5 | LSB | |
| Gain Error | | | ± 1.5 | LSB | |
| Gain Error Match | | | ± 0.5 | LSB | |
| 0 V to $2 \times REF_{IN}$ Input Range | | | | | $-REF_{IN}$ to $+REF_{IN}$ biased about REF_{IN} with twos complement output coding |
| Positive Gain Error | | | ± 1.5 | LSB | |
| Positive Gain Error Match | | | ± 0.5 | LSB | |
| Zero Code Error | | | ± 8 | LSB | Typically ± 0.8 LSB |
| Zero Code Error Match | | | ± 0.5 | LSB | |
| Negative Gain Error | | | ± 1 | LSB | |
| Negative Gain Error Match | | | ± 0.5 | LSB | |
| ANALOG INPUT | | | | | |
| Input Voltage Range | 0 | | REF_{IN} | V | RANGE bit set to 1 |
| | 0 | | $2 \times REF_{IN}$ | V | RANGE bit set to 0, $V_{DD}/V_{DRIVE} = 4.75\text{ V}$ to 5.25 V |
| DC Leakage Current | | | ± 1 | μA | |
| Input Capacitance | | 20 | | pF | |
| REFERENCE INPUT | | | | | |
| REF_{IN} Input Voltage | | 2.5 | | V | $\pm 1\%$ specified performance |
| DC Leakage Current | | | ± 1 | μA | |
| REF_{IN} Input Impedance | | 36 | | k Ω | $f_{SAMPLE} = 1\text{ MSPS}$ |
| LOGIC INPUTS | | | | | |
| Input High Voltage, V_{INH} | $0.7 \times V_{DRIVE}$ | | | V | |
| Input Low Voltage, V_{INL} | | | $0.3 \times V_{DRIVE}$ | V | |
| Input Current, I_{IN} | | | ± 1 | μA | Typically 10 nA, $V_{IN} = 0\text{ V}$ or V_{DRIVE} |
| Input Capacitance, C_{IN}^1 | | | 10 | pF | |

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|--|--|-----|---------|---------|--|
| LOGIC OUTPUTS | | | | | |
| Output High Voltage, V_{OH} | $V_{DRIVE} - 0.2$ | | | V | $I_{SOURCE} = 200 \mu A$, $AV_{DD} = 2.7 V$ to $5.25 V$ |
| Output Low Voltage, V_{OL} | | | 0.4 | V | $I_{SINK} = 200 \mu A$ |
| Floating-State Leakage Current | | | ± 1 | μA | |
| Floating-State Output Capacitance ¹ | | | 10 | pF | |
| Output Coding | Straight (natural) binary Twos complement | | | | CODING bit set to 1 CODING bit set to 0 |
| CONVERSION RATE | | | | | |
| Conversion Time | | | 800 | ns | 16 SCLK cycles with SCLK at 20 MHz |
| Track-and-Hold Acquisition Time | | | 300 | ns | Sine wave input |
| | | | 300 | ns | Full-scale step input |
| Throughput Rate | | | 1 | MSPS | |
| POWER REQUIREMENTS | | | | | |
| V_{DD} | 2.7 | | 5.25 | V | |
| V_{DRIVE} | 2.7 | | 5.25 | V | |
| I_{DD} | | | | | Digital inputs = 0 V or V_{DRIVE} |
| Normal Mode (Static) | | 600 | | μA | $AV_{DD} = 2.7 V$ to $5.25 V$, SCLK on or off |
| Normal Mode (Operational) | | | 2.7 | mA | $AV_{DD} = 4.75 V$ to $5.25 V$, $f_{SCLK} = 20 MHz$ |
| | | | 2 | mA | $AV_{DD} = 2.7 V$ to $3.6 V$, $f_{SCLK} = 20 MHz$ |
| Auto Shutdown Mode | | 960 | | μA | $f_{SAMPLE} = 250 kSPS$ |
| | | | 0.5 | μA | Static |
| Full Shutdown Mode | | | 0.5 | μA | SCLK on or off (20 nA typ) |
| Power Dissipation | | | | | |
| Normal Mode (Operational) | | | 13.5 | mW | $AV_{DD} = 5 V$, $f_{SCLK} = 20 MHz$ |
| | | | 6 | mW | $AV_{DD} = 3 V$, $f_{SCLK} = 20 MHz$ |
| Auto Shutdown Mode (Static) | | | 2.5 | μW | $AV_{DD} = 5 V$ |
| | | | 1.5 | μW | $AV_{DD} = 3 V$ |
| Full Shutdown Mode | | | 2.5 | μW | $AV_{DD} = 5 V$ |
| | | | 1.5 | μW | $AV_{DD} = 3 V$ |

¹ Sample tested at 25°C to ensure compliance.

TIMING SPECIFICATIONS

$AV_{DD} = 2.7\text{ V to }5.25\text{ V}$, $V_{DRIVE} \leq AV_{DD}$, $REF_{IN} = 2.5\text{ V}$, $T_A = T_{MIN}\text{ to }T_{MAX}$, unless otherwise noted.

Table 2.

| Parameter ¹ | Limit at T_{MIN}, T_{MAX} | | | Description |
|------------------------|-----------------------------|------------------------|-------------------|---|
| | $AV_{DD} = 3\text{ V}$ | $AV_{DD} = 5\text{ V}$ | Unit | |
| f_{SCLK}^2 | 10 | 10 | kHz min | Minimum quiet time required between the \overline{CS} rising edge and the start of the next conversion \overline{CS} to SCLK setup time Delay from \overline{CS} until DOUT three-state disabled Data access time after SCLK falling edge SCLK low pulse width SCLK high pulse width SCLK to DOUT valid hold time SCLK falling edge to DOUT high impedance DIN setup time prior to SCLK falling edge DIN hold time after SCLK falling edge 16th SCLK falling edge to \overline{CS} high Power-up time from full shutdown/auto shutdown modes |
| | 20 | 20 | MHz max | |
| $t_{CONVERT}$ | $16 \times t_{SCLK}$ | $16 \times t_{SCLK}$ | | |
| t_{QUIET} | 50 | 50 | ns min | |
| t_2 | 10 | 10 | ns min | |
| t_3^3 | 35 | 30 | ns max | |
| t_4^3 | 40 | 40 | ns max | |
| t_5 | $0.4 \times t_{SCLK}$ | $0.4 \times t_{SCLK}$ | ns min | |
| t_6 | $0.4 \times t_{SCLK}$ | $0.4 \times t_{SCLK}$ | ns min | |
| t_7 | 10 | 10 | ns min | |
| t_8^4 | 15/45 | 15/35 | ns min/ns max | |
| t_9 | 10 | 10 | ns min | |
| t_{10} | 5 | 5 | ns min | |
| t_{11} | 20 | 20 | ns min | |
| t_{12} | 1 | 1 | μs max | |

¹ Sample tested at 25°C to ensure compliance. All input signals are specified with $t_r = t_f = 5\text{ ns}$ (10% to 90% of AV_{DD}) and timed from a voltage level of 1.6 V (see Figure 2). The 3 V operating range spans from 2.7 V to 3.6 V. The 5 V operating range spans from 4.75 V to 5.25 V.

² Mark/space ratio for the SCLK input is 40/60 to 60/40.

³ Measured with the load circuit of Figure 2 and defined as the time required for the output to cross 0.4 V or $0.7 \times V_{DRIVE}$.

⁴ t_8 is derived from the measured time taken by the data outputs to change 0.5 V when loaded with the circuit of Figure 2. The measured number is then extrapolated back to remove the effects of charging or discharging the 50 pF capacitor. This means that the time, t_8 , quoted in the timing characteristics is the true bus relinquish time of the part and is independent of the bus loading.

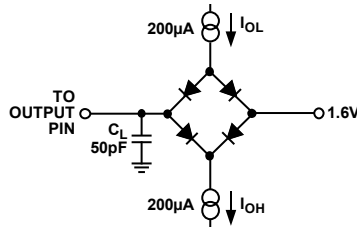


Figure 2. Load Circuit for Digital Output Timing Specifications

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 3.

| Parameter | Rating |
|---|---|
| AV_{DD} to AGND | $-0.3\text{ V to }+7\text{ V}$ |
| V_{DRIVE} to AGND | $-0.3\text{ V to }AV_{DD} + 0.3\text{ V}$ |
| Analog Input Voltage to AGND | $-0.3\text{ V to }AV_{DD} + 0.3\text{ V}$ |
| Digital Input Voltage to AGND | $-0.3\text{ V to }+7\text{ V}$ |
| Digital Output Voltage to AGND | $-0.3\text{ V to }AV_{DD} + 0.3\text{ V}$ |
| REF_{IN} to AGND | $-0.3\text{ V to }AV_{DD} + 0.3\text{ V}$ |
| Input Current to Any Pin Except Supplies ¹ | $\pm 10\text{ mA}$ |
| Operating Temperature Range | $-40^\circ\text{C to }+85^\circ\text{C}$ |
| Storage Temperature Range | $-65^\circ\text{C to }+150^\circ\text{C}$ |
| Junction Temperature | 150°C |
| Lead Temperature, Soldering | |
| Vapor Phase (60 secs) | 215°C |
| Infrared (15 secs) | 220°C |
| ESD | 1.5 kV |

¹Transient currents of up to 100 mA do not cause SCR latch-up.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

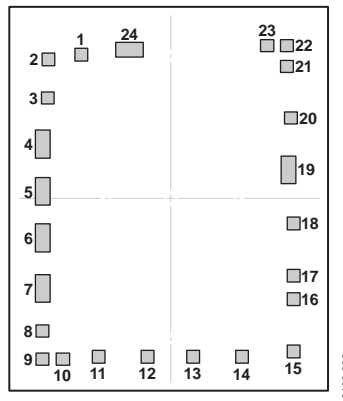
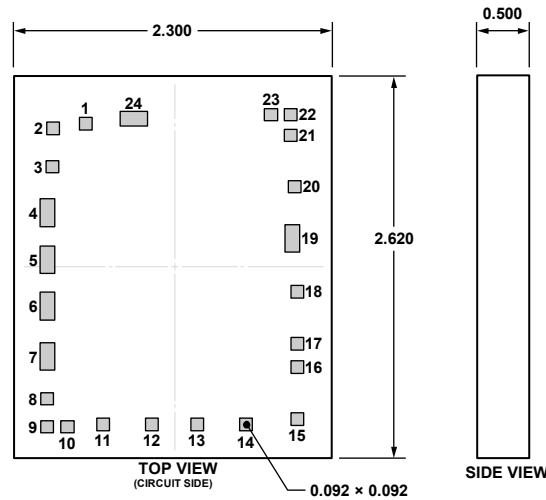


Figure 3. Pad Configuration

Table 4. Pad Function Descriptions

| Pad No. | X-Axis (μm) | Y-Axis (μm) | Mnemonic | Pad Type | Description |
|---------|-------------|-------------|------------------------|----------|---|
| 1 | -580.3 | +965.95 | SCLK | Single | Serial Clock |
| 2 | -815.4 | +932.75 | DIN | Single | Data In, Logic Input. |
| 3 | -815.4 | +677.6 | $\overline{\text{CS}}$ | Single | Chip Select. |
| 4A | -850.85 | +416 | AGND | Double | Analog Ground. |
| 4B | -850.85 | +316 | AGND | Double | Analog Ground. |
| 5 | -854.15 | +50.35 | AVDD | Double | Analog Power Supply Input. |
| 6 | -854.4 | -258.7 | AVDD | Double | Analog Power Supply Input. |
| 7A | -850.45 | -546 | VREF | Double | Reference Input. |
| 7B | -850.45 | -646 | VREF | Double | Reference Input. |
| 8 | -854.2 | -877.9 | NC | Single | No Connect. Do not connect to this pin. |
| 9 | -854.2 | -1070.1 | AGND | Single | Analog Ground. |
| 10 | -712.45 | -1070.1 | AGND | Single | Analog Ground. |
| 11 | -458.95 | -1054.1 | NC | Single | No Connect. Do not connect to this pin. |
| 12 | -108.95 | -1054.1 | NC | Single | No Connect. Do not connect to this pin. |
| 13 | +200.85 | -1054.1 | NC | Single | No Connect. Do not connect to this pin. |
| 14 | +550.85 | -1054.1 | NC | Single | No Connect. Do not connect to this pin. |
| 15 | +916.2 | -1021.15 | VIN3 | Single | Analog Input 0. |
| 16 | +916.2 | -671.15 | VIN2 | Single | Analog Input 1. |
| 17 | +916.2 | -510.75 | VIN1 | Single | Analog Input 2. |
| 18 | +916.2 | -160.75 | VIN0 | Single | Analog Input 3. |
| 19A | 880.85 | 144 | AGND | Double | Analog Ground. |
| 19B | 880.85 | 244 | AGND | Double | Analog Ground. |
| 20 | 896.05 | 537.15 | DOUT | Single | Data Output. |
| 21 | 865.35 | 885.8 | VDRIVE | Single | Logic Power Supply Input. |
| 22 | 865.35 | 1025.8 | VDRIVE | Single | Logic Power Supply Input. |
| 23 | 725.35 | 1025.8 | NC | Single | No Connect. Do not connect to this pin. |
| 24A | -191 | +997.4 | AGND | Double | Analog Ground. |
| 24B | -291 | +997.4 | AGND | Double | Analog Ground. |

OUTLINE DIMENSIONS



09-12-2011-A

Figure 4. 24-Pad Bare Die [CHIP]
(C-24-1)
Dimensions shown in millimeters

DIE SPECIFICATIONS AND ASSEMBLY RECOMMENDATIONS

Table 5. Die Specifications

| Parameter | Value | Unit |
|----------------------|---------------------|----------------|
| Chip Size | 2180 (x) × 2450 (y) | μm |
| Scribe Line Width | 120 (x) × 170 (y) | μm |
| Die Size | 2300 (x) × 2620 (y) | μm |
| Thickness | 500 | μm |
| Backside | Silicon | Not applicable |
| Passivation | Nitride | Not applicable |
| Bond Pads (Minimum) | 92 × 92 | μm |
| Bond Pad Composition | 99.5% Al, 0.5% Cu | % |
| ESD | 1.5 | kV |

Table 6. Assembly Recommendations

| Assembly Component | Recommendation |
|--------------------|-----------------------------|
| Die Attach | No special recommendations |
| Bonding Method | Gold ball or aluminum wedge |
| Bonding Sequence | 9 and 10 |

ORDERING GUIDE

| Model | Temperature Range | Package Description | Package Option |
|---------------|-------------------|------------------------|----------------|
| AD7924-KGD-DF | −40°C to +85°C | 24-Pad Bare Die [CHIP] | C-24-1 |