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APPLICATION NOTE

Careful Design Tames High Speed Op Amps

by Joe Buxton

Operational amplifiers continuously push the limits of speed and bandwidth. Today's high-speed IC op amps reach gain-bandwidth products in the hundreds-of-megahertz range—numbers unheard of just a few years ago. With such performance, designers must be extremely careful in preserving the op amp's stability without sacrificing bandwidth. Circuits and layouts previously used when designing with lower-frequency devices must be rethought in detail. Otherwise, circuit stability and ac performance can be impaired significantly.

Many factors cause instability in high-speed op amps. These include capacitive loading, inadequate power supply bypassing, input capacitance, and lead-lag compensation. Designers have dealt with both capacitive loading and supply bypass problems for some time. But at high frequencies, their effects are more critical and potentially harmful. Moreover, input capacitance and lead-lag compensation are usually ignored for lower-frequency circuits. Now their consideration is vital.

Driving a capacitive load is one of the most troublesome and difficult problems to overcome because it can easily cause circuit oscillation. When combined with an amplifier's output resistance (R_0), a capacitive load (C_L) creates a pole in the feedback loop that increases the closed-loop phase shift *(Fig. 1)*. Depending on its frequency, the phase shift can reduce phase margin, potentially causing the circuit to become unstable. This phase shift is easily calculated from the pole frequency (f_c):

$$f_c = 1/(2\pi R_0 C_L)$$

Additional phase shift $= \text{TAN}^{-1}(f_U/f_c)$

where f_u is the open-loop unity-gain frequency (the op amp's unity-gain bandwidth).

To verify these equations, compare the open-loop gain and phase responses of a 10-MHz, unity-gain-stable op amp, such as the OP-42 with and without a capacitive load *(Fig. 1, again)*. The network analyzer plots indicate the no-capacitive-load condition *(Fig. 1a)*. They also show a loading of 450 pF *(Fig. 1b)*. The 450-pF capacitive load combined with the OP-42's 45-Ω output impedance introduces a
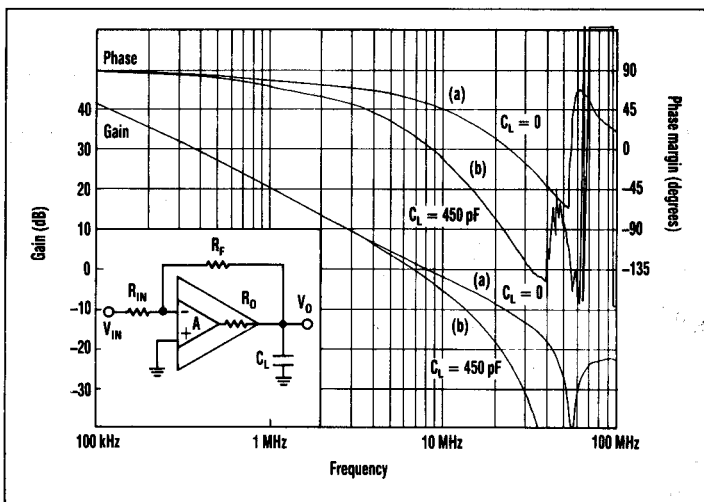
1. A CAPACITIVE LOAD (C_L) combines with an op amp's output impedance (R_0) to alter the gain and phase response, and thus the phase margin. The upper curves (a) are for an unloaded device, the lower curves (b) are for the same op amp driving a 450-pF load.

pole at $f_c = 8$ MHz. This results in an additional 45° of phase shift. Consequently, what used to be a stable circuit with 50° of phase margin degrades to a phase-margin of only 5°—potentially causing instability.

CLASSY CLASSICS

The classical way to maintain stability is to compensate for load capacitance by adding a resistor (R_X) in series with the amplifier's output impedance and a shunt capacitor (C_F) in the feedback path *(Fig. 2, left)*.[1] The basic technique requires adding the proper shunt capacitance and series resistance so that the external feedback network adds a net 0° of phase shift to the loop. Amplifier stability depends on the phase shift of the signal that's fed back to the op amp's inverting input. The signal's phase shift must be less than 180° when the loop gain is greater than or equal to 1. If the feedback network contributes 0° of phase shift, the signal is only phase shifted by the op amp. Assuming the op amp has enough phase margin for the particular gain used, stability is ensured.

Now that the stability goal of the feedback network is established, how is it achieved? Redrawing the

external feedback network helps clarify the analysis *(Fig. 2, right)*. Each capacitor contributes a pole and a zero to the feedback network. Intuitively, if the pole and zero contribution of one capacitor cancels the zero and pole contribution of the other capacitor, there will be 0° of phase shift. With this in mind, just derive the pole and zero locations for each capacitor, then set them equal to each other and solve for R_X and C_F. While it is straightforward in concept, the actual derivation is extremely involved and time consuming. But it can be approximated by taking an intuitive approach.

Because capacitive reactance changes with frequency, it can be assumed that a capacitor is an open circuit at 0 Hz and a short circuit at infinite Hz. To simplify network analysis, this principle is applied to one capacitor at a time. For the first case, assume that C_F is a short circuit, resulting in both a pole and a zero location as a function of C_L *(Fig. 3a)*. Next assume that C_L is an open circuit, again providing a pole and a zero location, but as a function of C_F *(Fig. 3b)*. Now there are two poles and two zeros. By equating the poles to the zeros, the necessary value for

R_X and C_F can be found with the following two equations:

$$R_X = R_0 R_{IN}/R_F$$

$$C_F = (1+1/|A_{CL}|)[(R_F+R_{IN})/R_F{}^2] \quad C_L R_0$$

where A_{CL} is the closed-loop gain.

By experimenting, it was found that the $1/A_{CL}$ term needed to be added to the equation for C_F. Just these two equations enables virtually any op-amp circuit to be compensated for virtually any capacitive load. A complete derivation performed at the PMI division accurately predicts the previous two equations, including the $1/A_{CL}$ term.

Though this method of compensation yields a stable circuit for any capacitive load, it reduces circuit-bandwidth drastically. The bandwidth is no longer determined by the op amp, but rather by the external components. C_F and R_F dominate, creating a closed-loop bandwidth of:

$$f_{-3 dB} = 1/2\pi C_F R_F$$

To show the limiting factors, substitute the equation for C_F into the previous equation and simplify:

$$f_{-3 dB} = 1/2\pi C_L R_0 (1 + 1/A_{CL})^2$$

This equation shows that the load capacitance (C_L) and the op amp's output impedance (R_0) need to be made as small as possible. Because R_0 is internal to the op amp, the only way to minimize it is to choose an op amp with low R_0. However, there is much more flexibility in controlling C_L. Consider all of the possible sources for C_L in the circuit and try to minimize them. For example, driving an unterminated coaxial cable can add significant amounts of load capacitance. It's important to back-terminate the cable to remove this capacitive load. A pc-board trace with a surrounding ground plane can also add a small amount of capacitance. To reduce its capacitive loading, keep the trace short and keep the ground plane away from it. Even if capacitive loads don't cause the circuit to oscillate, they should be minimized so as not to limit the closed-loop bandwidth.

Power-supply bypassing is often

dealt with by connecting a 10-μF tantalum capacitor in parallel with a 0.1-μF ceramic capacitor between the supply line and ground. Though this works in many cases, an understanding of what's actually happening helps prevent oscillations where bypassing is critical.

To start, an equivalent circuit of a typical power supply line with the bypass capacitor in place can be represented by an inductor in series with the supply line and a capacitor connected from the IC to ground. The line from the power supply is far from a perfect zero-impedance source, especially after it's routed through a wiring harness and pc-board trace. In addition, every supply line has parasitic inductance that reacts with the decoupling capacitance at some frequency. This causes the impedance, as seen by the IC, to become infinite and experience a rapid phase change. The op amp's phase margin degrades and the circuit may oscillate. To see why it may oscillate, calculate the equivalent parallel impedance of L and C as seen by the IC, Z_{eq}.

$Z_{eq} = sL(1/sC) / (sL + 1/sC)$
$\quad = (1/C)s / (s^2 + 1/LC)$

where: $s = \pm j(1/\sqrt{LC})$ the complex poles of the equation.

These complex poles cause the equivalent impedance to become infinite at a frequency:

$f = (1/2\pi)(1/\sqrt{LC})$

To show this, substitute the value for s into the original equivalent impedance equation:

$s = j\omega = j(1/\sqrt{LC})$

$Z_{eq} = (1/C)s / \{[j(1/\sqrt{LC})]^2 + 1/LC\}$

$Z_{eq} = (1/C)s / (-1/LC + 1/LC)$

The denominator then goes to zero, resulting in an expected infinite impedance. In reality, the impedance does not become infinite because of line losses—the small parasitic resistances that keep the denominator from going to zero. More importantly, the phase almost instantly changes by -180° at the pole frequency.

Like the supply line, the bypass ca-

pacitor also has a parasitic inductance, the equivalent series inductance (ESL). ESL creates another resonant frequency in combination with the bypass capacitor. But because they're in series, the capacitance and inductance form two zeros. These complex zeros cause the capacitor's impedance to go to zero and the phase to shift by +180°. A parasitic resistance, the equivalent series resistance (ESR) of the capacitor, dampens this response. Remember that ESR and ESL depend heavily upon the type of capacitor used, and thus should be considered.

A more complete equivalent bypass circuit along with a network analyzer gain-phase plot of an actual LC circuit illustrates the transfer function from the supply (V_p) to the IC's power supply pin (V_{IC}) *(Fig. 4)*. Notice the large gain peak, combined with -180° of phase shift, at the resonant frequency:

Freq. $= (1/2\pi)(1/\sqrt{L_pC_c}) = 1$ MHz

when $L_p = 250$ nH and $C_c = 0.1$ μF. The gain dips and the phase shifts by +180° at 16 MHz for $C_c = 0.1$ μF and $L_c = 1$nH.

What does all of this mean to the op amp attached to this supply line? To start, a power supply with high impedance means that any current drawn by the op amp causes significant voltage noise on the power supply line. Secondly, any phase shift in the power supply can also feed into the op amp and cause additional

phase shifts on its output. Remember that in a transistor-level analysis of an op amp, the power supplies are assumed to be an ac ground. This is true for most frequencies, but at the resonant frequency (with the bypass capacitor), this ac ground becomes a very high impedance with -180° of phase shift. These phase shifts can affect the output of the op amp, degrade the phase margin, and cause the op amp to oscillate. This effect is reduced somewhat by the power-supply rejection ratio (PSRR), which falls off at higher frequencies. Unfortunately, resonant peaks generally occur at high frequencies where most op amps are unable to reject it.

Wide-bandwidth op amps can easily have such a resonant frequency near their 0-dB (unity-gain) frequency, playing havoc with its gain and phase characteristics, and possibly again causing oscillation. For example, a network analyzer plot was done on the OP-42 with a supply line like that of figure 4. The plot clearly shows the effects on the op amp's output *(Fig. 5)*.

The first gain peak doesn't appear on the output but the gain dip does. This is a function of the drop in PSRR as the frequency rises. The OP-42's PSRR is high enough at 1 MHz, about 45 dB, to reject the first peak. But at 15 MHz, the PSRR has fallen to about 15 dB, allowing the gain dip to feed through to the output. There's a rapid change in both gain and phase at this frequency. In this
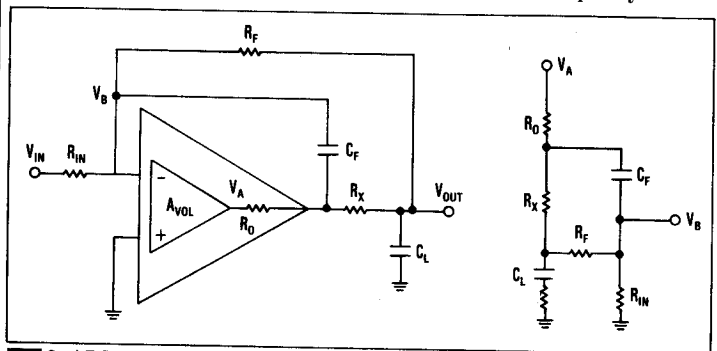
2. ADDING A RESISTOR (R_x) in series with the output and a capacitor (C_F) between the output and input of an op amp can reduce phase shift in the feedback loop to a value close to zero. This restores stability to an op amp which would oscillate when driving a capacitive load (C_L).

example, it happens that the gain dip is due to the complex zero and the phase jumps up, so the op amp maintains its phase margin.

However, if the complex pole had occurred at 15 MHz, the phase would have dipped drastically and could have resulted in –180° of phase shift, causing the op amp to oscillate. Clearly, what happens on its power supply line can severely degrade op-amp performance.

Because the supply line's inductance and the capacitor's ESL appear to be the main causes of circuit resonance, the inductance should be reduced. This is often easier said than done, and the inductance can never be completely eliminated. Furthermore, some inductance may actually be desirable to act as a filter. Consequently, liberal bypass capacitance is needed to move the resonance frequency lower to a point where the PSRR is high enough to reject the gain and phase changes. In addition, the bypass capacitor should be located as close to the IC as possible to minimize trace inductance between it and the IC.

Reducing the parasitic inductance within the capacitor is a matter of selecting the correct capacitor type for the job. Typically, a 10-μF tantalum in parallel with a 0.1-μF ceramic capacitor is specified for supply bypassing, and with good reason. The total bypass capacitance combined with the supply-line inductance sets the gain peak's position. To diminish its effect, the peak should be much lower in frequency than the amplifier's 0-dB frequency. As a result, a large capacitor is needed to move the peak lower in frequency to where the PSRR is high. A 10-μF tantalum fits this mold because large capacitance values are available in a reasonably sized component. In fact, in some applications where it's critical not only to maintain stability but also to ensure gain and phase-flatness out to the amplifier's 0-dB frequency, an even larger bypass capacitor is required to ensure rejection.

Unfortunately, tantalum capacitors aren't perfect because they have high ESR. On the other hand, ceramic capacitors have low ESR. Typical curves of impedance versus frequency for these two capacitors show that the ceramic capacitor has a much sharper dip in impedance (well below 1 Ω) at a much higher frequency due to its low ESR and ESL. However, the tantalum capacitor has much higher ESR, and th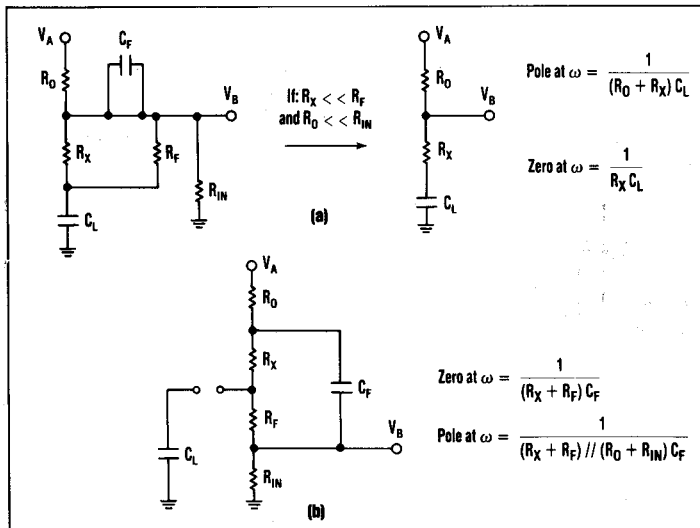us has a shallow dip down to the range of 1-10 Ω. If just the tantalum is used, the impedance of the bypass won't come close to an ideal ac ground at high frequency. Consequently, a lower-value ceramic capacitor is used, in parallel, to further reduce the high-frequency impedance of the supply bypass circuit. The tantalum capacitor reaches its ESR limit around 1 MHz. Above this frequency, the ceramic continues to lower the bypass impedance until its own ESL dominates around 10 MHz.

Typical curves of ceramic capacitors will usually include a few tenths of an inch of lead length. Most of the ESL that causes the impedance to rise sharply above 10 MHz actually comes from the leads. Shortening the leads reduces ESL. This illustrates the importance of placing bypass capacitors close to the IC. Chip capacitors can be valuable for high-speed circuits for this reason. Because they're surface mounted, chip capacitors have almost no lead length except the pc-board trace and the amplifier leads. Minimizing every source of lead length ensures clean supply bypassing at high frequencies.

The discussion so far dealt with only one amplifier connected to the supply, but usually many amplifiers share the same power source. When this is true, the supply line should be as short and wide as possible, and each IC should be bypassed individually. This reduces noise on the supply line, which arises from the op amps' rapidly changing supply-current demands.

Stray capacitance on the input of lower bandwidth op amps, such as the 741, can often be overlooked without significantly impacting circuit performance. However, when dealing with high-speed circuits, this capacitance becomes critical. Not only will the input capacitance cause the closed-loop bandwidth to drop, it can also cause the op amp to oscillate. This capacitance, which comes from both the op amp's input circuitry and the pc-board (or breadboard) layout, can be looked at as a capacitor to ground on the inverting input *(Fig. 6a)*.

To see how this capacitance causes

Pole at $\omega = \dfrac{1}{(R_0 + R_X) C_L}$

Zero at $\omega = \dfrac{1}{R_X C_L}$

If: $R_X << R_F$ and $R_0 << R_{IN}$

(a)

Zero at $\omega = \dfrac{1}{(R_X + R_F) C_F}$

Pole at $\omega = \dfrac{1}{(R_X + R_F) // (R_0 + R_{IN}) C_F}$

(b)

3. TO FIND THE POLE and zero locations caused by the load and feedback capacitors in an op-amp circuit, assume that C_F is a short circuit (a) and C_L is an open circuit (b).

instability, consider the feedback network that includes the amplifier's output impedance *(Fig. 6b)*. The capacitor's phase contribution to the feedback signal is determined by analyzing the circuit's transfer function from V_A to V_B. In other words, the signal is phase shifted by the amplifier's open-loop phase characteristic and then further shifted by the feedback network's phase response. The transfer function is easily determined to be:

$$V_B/V_A = R_1/[(R_1+R_2+R_0) + sC_1R_1(R_0+R_2)]$$

which produces a pole at:

$$fc = (R_1 + R_2 + R_0)/2\pi C_1 R_1(R_0 + R_2)$$
$$\approx (R_1 + R_2)/2\pi C_1 R_1 R_2$$
(Assuming $R_0 << R_1$ and R_2)

This pole causes a phase shift at the unity-gain frequency, f_U, of:

Phase Shift = $TAN^{-1}(f_U/f_C)$

If this phase shift is large enough, the amplifier may oscillate. As an example, consider the OP-42 with 5 pF of input capacitance and $R_1 = R_2 = 10$ kΩ. This creates a pole at 6.4 MHz, creating a phase shift of 51° at the unity-gain crossover frequency of 8 MHz. Because the OP-42 has a phase margin of 48°, a phase shift of 51° can start the amplifier oscillating.

Fortunately, a feedback capacitor can be added in parallel with the feedback resistor to compensate for the input capacitance. The optimum value for the feedback capacitor is easily calculated by determining the pole and zero locations of the feedback network and setting them equal to each other:

Pole = $1/2\pi(C_1 + C_2)R_1//R_2$

Zero = $1/2\pi C_2 R_2$

equating and solving these gives:
$C_2 \geq C_1 R_1 /R_2$
Using this value for C_2 provides for zero degrees of phase shift in the feedback network. A shift of 0° ensures stability (assuming the op amp itself is stable). An interesting note is that most resistors have about 1-2 pF of stray capacitance across them, which helps to stabilize the circuit. In the previous example, to compensate
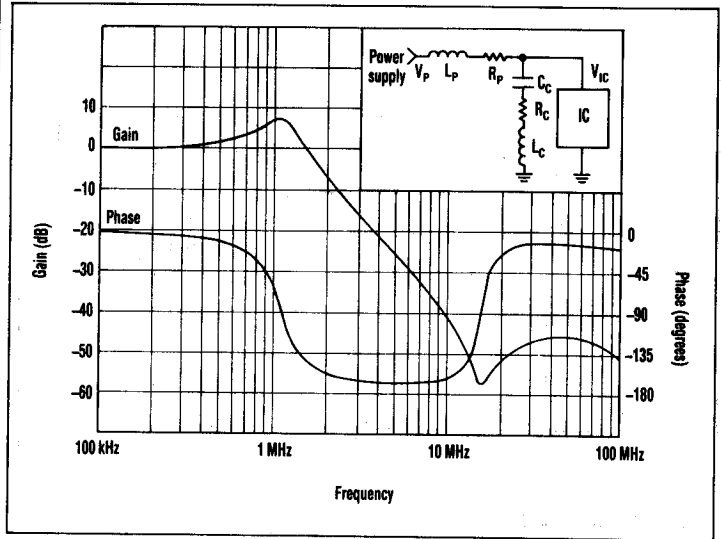
4. DUE TO RLC PARASITICS, the bypassed power supply line of an IC can resonate at several frequencies. In this instance, pronounced gain and phase changes occur at 1 and 16 MHz.

for the 5-pF input capacitance of the OP-42, C_2 also needs to be 5 pF.

The board layout can be a major source of stray input capacitance. This capacitance arises from the input traces to the summing junction of the op amp.

As a reference point, 0.025 in. of pc-board trace with a ground plane surrounding it, on the opposite side of the board, represents about 10 pF of capacitance per inch. Of course, this value varies depending upon the board thickness and the material its made of. But there can easily be enough input capacitance to cause an amplifier to oscillate.

The effects of the input capacitance can be reduced by moving the pole further out in frequency to reduce its effects near the 0-dB frequency. Most op amps have 3 to 5 pF of input capacitance—a combination of the differential-and common-mode capacitances.

For inverting applications, the two capacitances add. However, for non-inverting configurations, the differential capacitance is effectively zero, leaving about 1 to 3 pF of common-mode capacitance on each input. This capacitance is fixed for any given op

amp and can't be reduced.

On the other hand, some control of pc-board stray capacitance does exist. There are two key ways to reduce this capacitance. First, keep the input traces as short as possible. Put the feedback resistor and the input source very close to the op amp's input, minimizing pc-board trace length. Keep the analog section close together to further reduce trace lengths. Second, don't place the ground plane near the op amp except where it's needed for the circuit. Be especially careful to keep the ground plane away from the op amp's inputs. The obvious exception to this occurs when the noninverting pin is grounded. When ground really is needed, bring it in with a wide trace to ensure a low resistance ground. Don't locate the ground plane on the opposite side of the board from the analog section. Combining all of these measures will go a long way toward keeping the stray input capacitance to a minimum.

The best possible pc-board layout for high-speed analog circuits would pack the analog parts close together, attenuating trace length. Surface-mounted devices and chip capacitors

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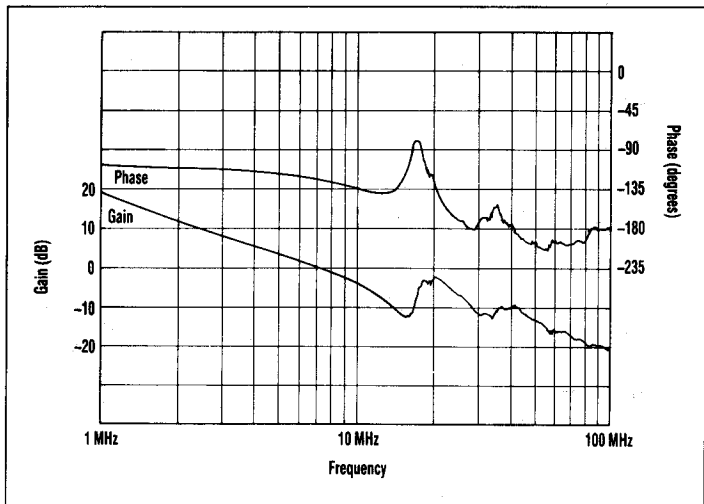
5. THE RESONANCES SEEN by the supply pins of an op amp translate into rapid changes in op-amp gain and phase with an attendant loss in phase margin and increased potential for oscillation. The effect is shown here at 16 MHz.

for power-supply bypassing can really help. The ground plane should be around the perimeter of the analog section and only come in through traces to make contact where ground is required. Try to avoid using sockets to mount the ICs on the board, because they can add another 1 to 3 pF of capacitance to the devices' input pins.

Referring back to the pole equation, it can be seen that minimizing the capacitance isn't the only way to reduce its effects. The parallel combination of the resistors, R_1 and R_2, should also be kept small. The op amp itself determines how small a feedback resistor can be used. Somewhere around 1-2 kΩ is best for most high-frequency amplifiers.

Lowering the resistors by a factor of 10 is the same as reducing the input capacitance by the same factor. However, the output circuit must be able to drive the feedback circuit and the load.

By compensating for the input capacitance with the feedback capacitor, C_2 can stabilize the circuit. However, it reduces bandwidth. Capacitor C_2 forms a pole with the feedback resistor, R_2, which limits the bandwidth to:

$$\text{Bandwidth} = 1/2\pi C_2 R_2$$

Clearly the best way to deal with input capacitance is to minimize both it and the feedback resistance. This reduces the possibility of the circuit oscillating and preserves maximum closed-loop bandwidth.

TRICK THOSE OP AMPS

Unfortunately, not all op amps are created stable—at least not at unity gain. Many high-speed op amps are stable only for gains greater than five or even ten. These broadband op amps sacrifice unity-gain stability to achieve a much higher gain-bandwidth product. What happens if a design calls for unity gain and you can't find a unity-gain-stable op amp that fits the application? It's not hopeless—by simply adding a capacitor and resistor across the inputs, almost any amplifier can be made stable at unity gain *(Fig. 7)*. This configuration reduces the feedback factor beta (β) at high frequencies, and the amplifier "thinks" it's running at a gain greater than unity.

To understand this compensation technique, first assume that the capacitor is a short at high frequencies, so all that remains is R_C and R_F. The

calculation for the value of R_C is based on the amplifier's minimum stable gain If the amplifier needs a gain of at least 5, make $R_C = R_F/4$ to get $\beta = 1/5$. Because the feedback is the equivalent of the minimum gain needed for stability, the amplifier thinks it's at a closed-loop gain of 5 and is therefore stable. However, the signal sees a closed-loop gain of unity, which can be shown by deriving the expression for the gain:

$$V_O = -A_{OL}(R_C/R_C + R_1)V_O + A_{OL}[V_{IN} - (R_1/R_C + R_1)V_{IN}]$$

where A_{OL} is the open-loop gain of the amplifier.

This expression simplifies to:

$$V_O/V_{IN} = A_{OL}\beta / (1 + A_L\beta)$$
$$= 1/(1/A_{OL}\beta + 1)$$

where

$$\beta = R_C/(R_C + R_1)$$

When the open-loop gain is large, $V_O/V_{IN} = 1$. Unity gain in the signal path is maintained even though the amplifier thinks it is at a closed-loop gain of five.

Next consider the value of the compensating capacitor, C_C. It must be large enough to ensure that the amplifier satisfies the β requirement at a low enough frequency to ensure stability. A minimum value for C_C should provide an impedance equal to that of R_C at a frequency at least a decade below the corner frequency for the amplifier's lowest stable gain:

$$C_C = 1/2\pi R_C(f_C/10)$$

For example, consider the OP-64, a high slew-rate op amp. Its lowest stable gain (5) yields a corner frequency at 16 MHz. A feedback resistor of 1000 Ω results in an R_C of 250 Ω and a C_C of 398 pF—the minimum value that should be considered for C_C.

This equation holds true for operation in a noninverting configuration. Now consider an inverting circuit, whose analysis is very similar. The closed-loop gain equation becomes:

$$V_O/V_{IN} = -1/(1 + 1/A_{OL}\beta)$$

where

$$\beta = (R_C//R_1) / (R_C//R_1 + R_2)$$

This expression is similar to the noninverting case except for the sign and the value of β. The expression for β indicates that the input resistor, R_1, is parallel with R_C at high frequencies. This parallel combination calculates the value of R_C for minimum stable gain. The capacitor's value is calculated the same as for the noninverting case.

WHAT'S THE CATCH?

An op amp's bandwidth and settling time can be affected by lead-lag compensation. Don't make the mistake of thinking that because the amplifier is in a unity-gain configuration that its signal bandwidth equals the amplifier's full gain-bandwidth product. Using lead-lag compensation doesn't increase the bandwidth above that at the minimum stable gain. For example, the OP-64 has a gain-bandwidth product of 80 MHz but it's stable only for closed-loop gains of five or more. Therefore, its bandwidth is 16 MHz for a gain of five. When compensated for unity-gain operation, its bandwidth is still 16 MHz, as is seen in the results of the circuit's Spice analysis (*Fig. 7, again*). To understand this effect, look at the closed loop gain expression for $\beta = 1/5$:

$$V_0/V_{IN} = 1/(5/A_{OL} + 1)$$

and compare it to a typical unity gain expression:
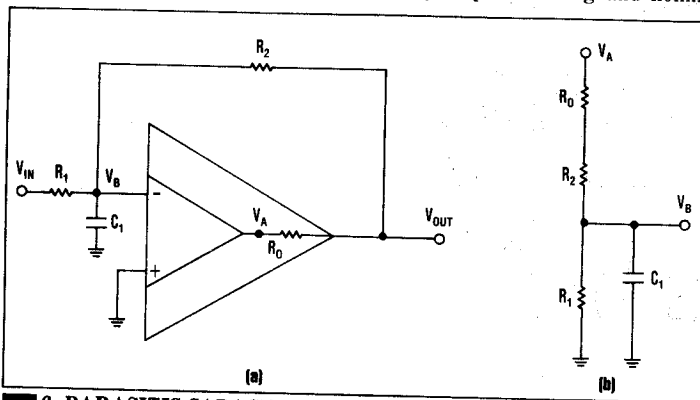
$$V_0/V_{IN} = 1/(1/A_{OL} + 1)$$

Due to β, the compensated amplifier's gain bandwidth is one-fifth that of the uncompensated OP-64.
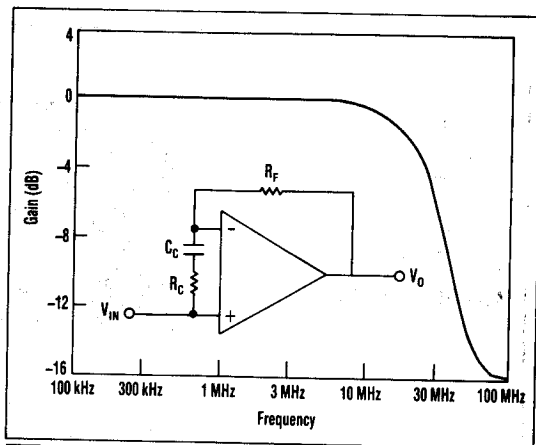
Lead-lag compensation can also affect an op amp's settling time. This can be illustrated by examining the transient response of the OP-64 (*Figs. 8a and 8b*). These tests were performed with $C_C = 470$ pF and $R_C = 250\ \Omega$. The circuit's settling time to 0.1% increases to 600 ns in contrast to the $A_v = 5$ settling time of 390 ns. However, this effect is easily overcome by increasing the value of C_C. Another test was performed with $C_C = 1\ \mu F$ and the results prove to be much better (*Fig. 8c*). The settling time in this instance drops to 310 ns—comparable to the $A_v = 5$ settling time. Using a smaller capacitor while ensuring stability still causes significant overshoot, resulting in a long settling time.

Changing the input voltage from -1 V to $+1$ V almost instantly creates a large differential voltage between the op amp's inverting and nonin-

7. LEAD-LAG COMPENSATION formed by capacitor C_C and resistor R_C can stabilize at unity gain. Typically, this op amp is stable only at a higher gain.
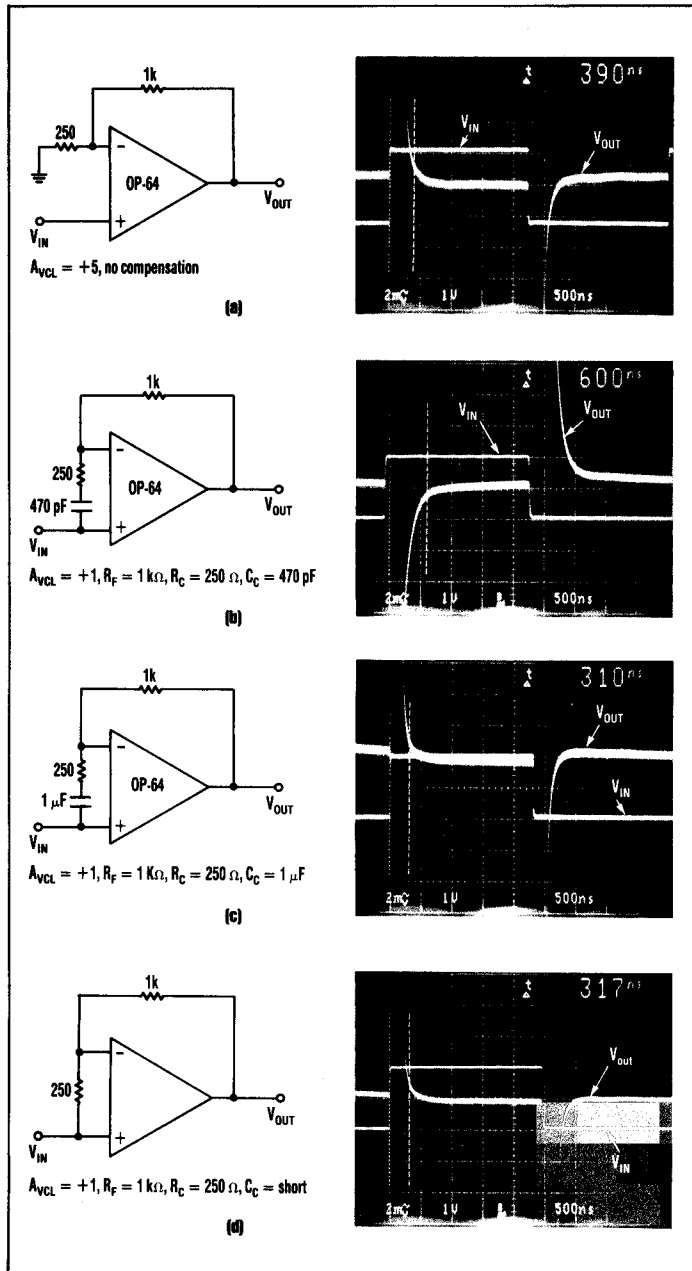
verting inputs. The smaller capacitor, combined with the compensating resistor, has a relatively small RC time constant. It charges quickly towards the full differential voltage. When the amplifier overshoots while trying to return to the final output voltage (the input voltage times the closed-loop gain), the capacitor is charged to enough differential voltage to continue forcing the output high. The long decay in the overshoot is caused by the slow discharge of the compensation capacitor. When the larger capacitor is used, the RC time constant becomes very large and the capacitor can only charge to a fraction of the differential voltage. Consequently, when the amplifier overshoots, the capacitor isn't charged to enough of the differential voltage to continue to force the output high. As a result, it quickly returns to the final voltage.

While overall settling time varies considerably, the slew rate (and thus the full power bandwidth) is constant. Regardless of the capacitor chosen, the slew rate is the same as that for a minimum-stable-gain condition. The amplifier's slew rate is a function of its internal structure—it's independent of the compensating resistor and capacitor.

This discussion may raise such questions as: "How big a capacitor

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6. PARASITIC CAPACITANCE on an op amp's input (C_1) reduces phase margin and can cause oscillation (a). Its effect can be analyzed by considering C_1 as part of the op amp's feedback network (b).

1k

250

OP-64

V_{OUT}

V_{IN}

$A_{VCL} = +5$, no compensation

(a)

390^{ns}

V_{IN} V_{OUT}

2m℧ 1 V 500ns

1k

250

470 pF

OP-64

V_{OUT}

V_{IN}

$A_{VCL} = +1, R_F = 1 k\Omega, R_C = 250 \Omega, C_C = 470 pF$

(b)

600^{ns}

V_{IN} V_{OUT}

2m℧ 1 V 500ns

1k

250

1 µF

OP-64

V_{OUT}

V_{IN}

$A_{VCL} = +1, R_F = 1 K\Omega, R_C = 250 \Omega, C_C = 1 µF$

(c)

310^{ns}

V_{OUT}

V_{IN}

2m℧ 1 V 500ns

1k

250

V_{OUT}

V_{IN}

$A_{VCL} = +1, R_F = 1 k\Omega, R_C = 250 \Omega, C_C = short$

(d)

317^{ns}

V_{out}

V_{IN}

2m℧ 1 V 500ns

8. WHEN AN OP AMP with a minimum stable gain of 5 is lead-lag compensated to run at a gain of one, its original settling time of about 400 ns (a) increases to about 600 ns (b). However, increasing the size of the compensation capacitor from 470 pF to 1 µF drops the settling time to about 300 ns (c). Shorting the capacitor shows similar results (d).

should be used? And if a bigger capacitor is better, then why use one at all?" To answer the first question experimentally, a capacitor that's roughly 1000 times the calculated value usually works to keep the overshoot down and the settling time to a minimum. The settling time with just the resistor in place was also measured *(Fig. 8d)*. It is 317 ns, almost the same as when using $C_C = 1 µF$. However, dc errors will creep in if the capacitor isn't used. With the capacitor missing, the dc noise gain of this circuit is now also five. Therefore, any dc errors, such as voltage offset, are increased by a factor of five at the output. Because high-speed amplifiers typically have relatively large offsets, dc errors can be significant and certainly need to be considered.

MORE NOISE GAIN

High-frequency or ac noise gain must also be considered. Because the amplifier's feedback is now equivalent to a gain of 5, its ac noise is boosted by a factor of five at the output. Voltage noise is typically modelled as a noise generator on the amplifier's inverting input. A Spice analysis was performed to measure the noise gain by placing the input source on the inverting input and measuring the amplitude of the output for two different compensation capacitors, 470 pF and 1 µF *(Fig. 9)*. At unity gain, the noise gain would usually be one, but as the plot shows, the lead-lag compensation increases it to five (14 dB). By looking at these two plots, it seems that using a 1-µF capacitor generates significantly more noise than the 470-pF capacitor. However, the difference isn't that great. The equation for total rms noise over a given bandwidth is:
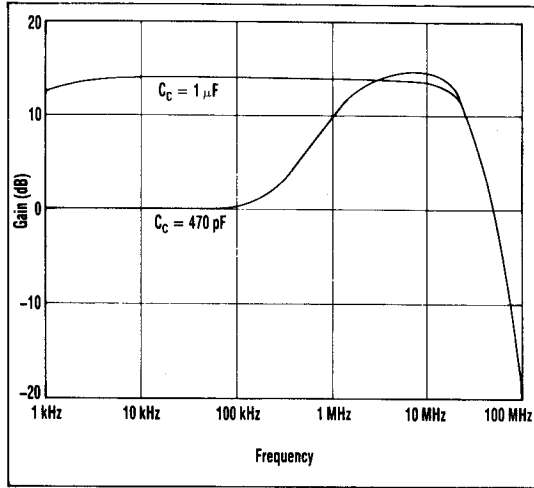
$$E_n = e_n \sqrt{(f_H - f_L)}$$

where:

e_n = the spectral voltage noise density

f_H = upper frequency limit

f_L = lower frequency imit

Examining the plot, both capacitors appear to have the same f_H—20

MHz—but the f_t is different. It's about 500 kHz for the 470-pF capacitor and about 500 Hz for the 1-μF capacitor. However, this only creates a difference of 1.3% for the total noise. Therefore, the noise trade-off with the 1-μF capacitor is minimal when compared to the difference in settling time resulting from the two capacitors. Lead-lag compensation is a valuable tool in dealing with high-frequency op amps. And, as the aforementioned discussion shows, it can offer stability for op amps that typically would be unstable at low gains. However, there are trade-offs, so care must be exercised when using this compensation scheme.□

Reference:
1. Precision Monolithics Inc., 1988 Analog Applications Seminar.

For a complete discussion of the op-amp stability criterion:

Gary, P., and Meyer, G. *Analog Integrated Circuits*. (New York: Wiley, 1984), pp. 527-70.

9. UPPING THE VALUE of a lead-lag compensation capacitor from 470 pF to 1 μF raises the low-frequency noise gain by about 10 dB. Over a given bandwidth, however, the total rms noise is only raised by a small percentage.

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